



**Memory Products**

1989/1990 Data Book

Advanced  
Micro  
Devices

**EPROM**

**memories**

**PROM**

**ExpressROM™**

**FIFO**

**CAM**

**FLASH**

**SRAM**

**E<sup>2</sup>PROM**







Advanced  
Micro  
Devices

# Memory Products Data Book

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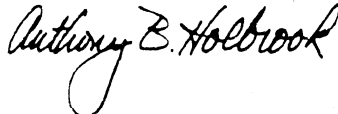
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As a market leader in non-volatile memories, Advanced Micro Devices provides the best of today's design and technology. The 1989/1990 Memory Products Data Book contains technical specifications on these important products:

- High-Performance 1-Megabit EPROMs in both x 8 and x 16 configurations
- a content-addressable memory device, offering more speed and flexibility in many applications — the Am99C10
- CMOS High-Performance PROMs
- EPROMs with speeds to 55 ns

Advanced information specifications on soon-to-be introduced products are included as well. This information covers 2-Megabit EPROMs, Flash memories, and ExpressROM™ devices.

More than one hundred memory products are detailed in this comprehensive volume. Over 50% of these data sheets cover CMOS products. We have highlighted these important CMOS products with blue paper.



Anthony B. Holbrook  
President and Chief Operating Officer

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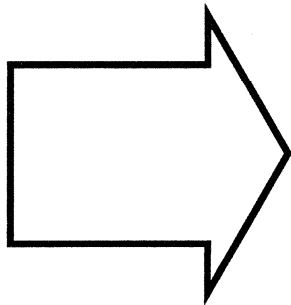
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Advanced  
Micro  
Devices



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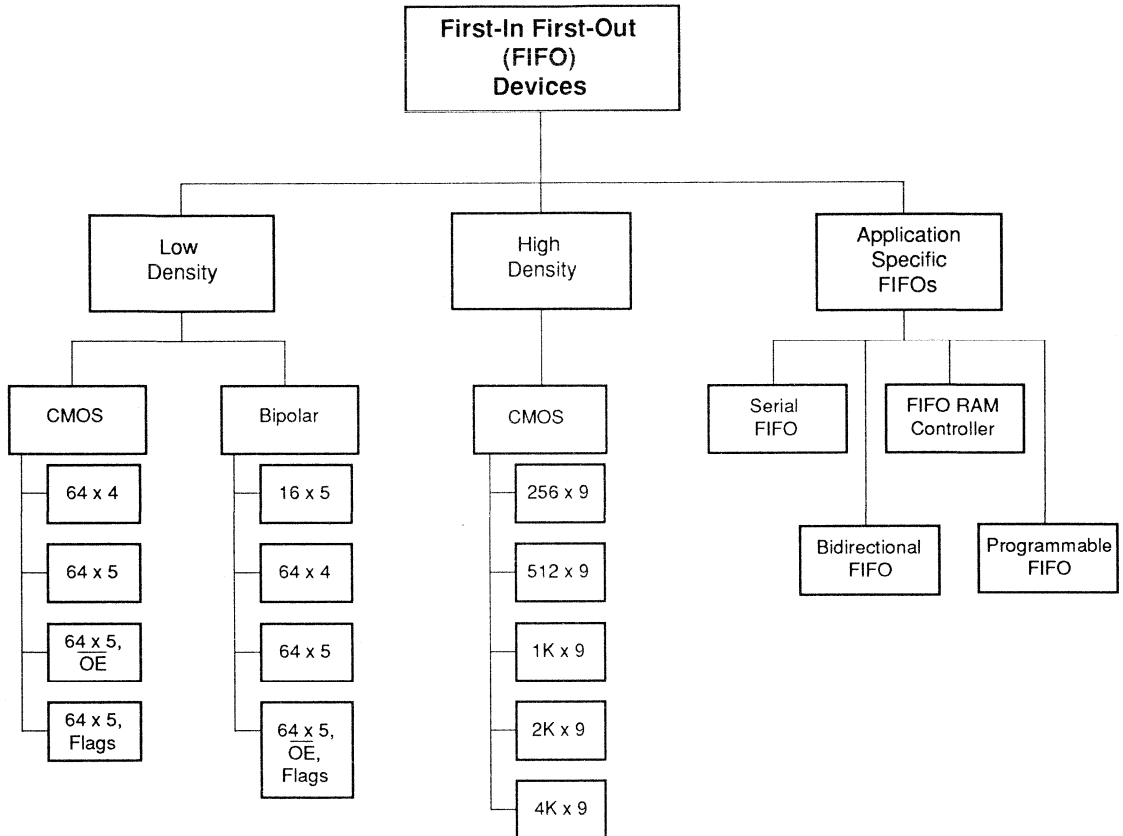
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# First-In First-Out Devices Selector Guide



1

## Features and Benefits

### Low Density CMOS FIFOs (64 x 4/5)

- Shift rates to 40 MHz
- Zero standby power consumption
- Ram based technology with fast access times
- Three state output and status flags
- Expandable in width and depth

### High Density CMOS FIFOs (1/4K, 1/2K, 1K, 2K, 4K x 9)

- Data Rates, 0 to 28.5 MHz
- Low power consumption – 70mA max
- Status flags — Half-full, Empty, Full
- Asynchronous and simultaneous read/write
- Expandable in width and depth

# First-in First-Out Devices Selector Guide

## Low Density FIFOS

Technology	Part Number	Organization	Type	Max Data Rate MHz	Max ICCmA	Package Type	Pin Count	Features
B	74S225	16 x 5	C	10	120	N, J	20	TSO
B	74S225A	16 x 5	C	20	120	N, J	20	TSO
B	C67401	64 x 4	C	10	160	N,J, NL	16, 20 (NL)	TPO
B	67401	64 x 4	S	10	160	N,J, NL	16, 20 (NL)	TPO
B	C67401A	64 x 4	C	15	170	N,J, NL	16, 20 (NL)	TPO
B	67401	64 x 4	S	15	170	N,J, NL	16, 20 (NL)	TPO
B	C67402	64 x 5	C	10	180	N,J, NL	16, 20 (NL)	TPO
B	67402	64 x 5	S	10	180	N,J, NL	16, 20 (NL)	TPO
B	C67402A	64 x 5	C	15	190	J	18	TPO
B	67402A	64 x 5	S	15	190	J	18	TPO
B	67413	64 x 4	S	25	240	J	20	TPO, Status Flags
B	67413A	64 x 4	S	35	240	J	20	TPO, Status Flags
C	67C401-10	64 x 4	C	10	35	N, J, NL	16	TPO Low Power, RAM Based
C	67C401-15	64 x 4	C	15	45	N, J, NL	16	TPO Low Power, RAM Based
C	67C4013-10	64 x 4	C	10	35	N, J, NL	16	TSO Low Power, RAM Based
C	67C4013-15	64 x 4	C	15	45	N, J, NL	16	TSO Low Power, RAM Based
C	67C402-10	64 x 5	C	10	35	N, J, NL	18	TPO Low Power, RAM Based
C	67C402-15	64 x 5	C	15	45	N, J, NL	18	TPO Low Power, RAM Based
C	67C4023-10	64 x 5	C	10	35	N, J, NL	18	TSO Low Power, RAM Based
C	67C4023-15	64 x 5	C	15	45	N, J, NL	18	TSO Low Power, RAM Based
C	67C4033-10	64 x 5	C	10	35	N, J, NL	20	TSO Low Power, RAM Based, Status Flags
C	67C4033-15	64 x 5	C	15	45	N, J, NL	20	TSO Low Power, RAM Based, Status Flags
C	67C401-25	64x4	C	25	60	N, J, NL	16	TPO Low Power, RAM Based
C	67C401-35	64x4	C	35	60	N, J, NL	16	TPO Low Power, RAM Based
C	67C4013-25	64x4	C	25	60	N, J, NL	16	TSO Low Power, RAM Based
C	67C4013-35	64x4	C	35	60	N, J, NL	16	TSO Low Power, RAM Based
C	67C402-25	64x5	C	25	60	N, J, NL	18	TPO Low Power, RAM Based
C	67C402-35	64x5	C	35	60	N, J, NL	18	TPO Low Power, RAM Based
C	67C4023-25	64x5	C	25	60	N, J, NL	18	TSO Low Power, RAM Based
C	67C4023-35	64x5	C	35	60	N, J, NL	18	TSO Low Power, RAM Based
C	67C413-40	64x5	S	40	60	N, J, NL	20	TPO Low Power, RAM Based, Status Flags

### Notes:

Technology:  
B – Bipolar  
C – CMOS

Type:  
C – Cascadable  
S – Standalone

Package Type:  
N – Plastic  
J – Ceramic  
NL – PLCC

Features:  
TSO – Three State Output  
TPO – Totem Pole Output

High Density FIFOS

Technology	Part Number	Organization	Type	Max Data Rate MHz	Max ICCmA	Package Type	Pin Count	Features
C	7200-80	256 x 9	C	10	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=80ns, Status Flags
C	7200-65	256 x 9	C	12	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=65ns, Status Flags
C	7200-50	256 x 9	C	15	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=50ns, Status Flags
C	7200-35	256 x 9	C	22	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=35ns, Status Flags
C	7200-25	256 x 9	C	28.5	70	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=25ns, Status Flags
C	7201-80	512 x 9	C	10	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=80ns, Status Flags
C	7201-65	512 x 9	C	12	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=65ns, Status Flags
C	7201-50	512 x 9	C	15	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=50ns, Status Flags
C	7201-35	512 x 9	C	22	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=35ns, Status Flags
C	7201-25	512 x 9	C	28.5	70	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=25ns, Status Flags
C	7202-80	1K x 9	C	10	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=80ns, Status Flags
C	7202-65	1K x 9	C	12	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=65ns, Status Flags
C	7202-50	1K x 9	C	15	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=50ns, Status Flags
C	7202-35	1K x 9	C	22	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=35ns, Status Flags
C	7202-25	1K x 9	C	28.5	70	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=25ns, Status Flags
C	7203-80	2K x 9	C	10	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=80ns, Status Flags
C	7203-65	2K x 9	C	12	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=65ns, Status Flags
C	7203-50	2K x 9	C	15	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=50ns, Status Flags
C	7203-35	2K x 9	C	22	60	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=35ns, Status Flags
C	7203-25*	2K x 9	C	28.5	70	PC, DC, JC, RC	28, 32 (JC)	TSO Access Time=25ns, Status Flags
C	7204-80*	4K x 9	C	10	60	PC, DC, JC	28, 32 (JC)	TSO Access Time=80ns, Status Flags
C	7204-65*	4K x 9	C	12	60	PC, DC, JC	28, 32 (JC)	TSO Access Time=65ns, Status Flags
C	7204-50*	4K x 9	C	15	60	PC, DC, JC	28, 32 (JC)	TSO Access Time=50ns, Status Flags
C	7204-35*	4K x 9	C	22	60	PC, DC, JC	28, 32 (JC)	TSO Access Time=35ns, Status Flags
C	7204-25*	4K x 9	C	28.5	70	PC, DC, JC	28, 32 (JC)	TSO Access Time=25ns, Status Flags



Application Specific FIFOS

Technology	Part Number	Organization	Type	Max Data Rate MHz	Max ICCmA	Package Type	Pin Count	Features
B	67417	64 x m/9/1	S	10 Par. 28 Ser.	350	J	24	TSO Parallel/Serial, Status Flags
B	674219	512-64K	S	10	350	J	40	TSO FIFO RAM Controller, 16-Bit SRAM Address, Status Flags
C	AM4701	2-512x9	S	17	100	PC	28	TSO Access Time=45ns, Programmable Flags
C	AM4601*	512x9	S	22	100	PC	28	TSO Access Time=35ns, Programmable Flags

Notes:

Technology:  
B – Bipolar  
C – CMOS

Type:  
C – Cascadable  
S – Standalone

Package Type:  
PC, RC, N – Plastic DIP  
DC, J – Ceramic DIP  
JC, NL – PLCC

Features:  
TSO – Three State Output

\* Consult Factory

# FIFO Competitive Cross Reference Guide



## CYPRESS

CY7C401-5PC  
 CY7C401-5DC  
 CY7C401-10PC  
 CY7C401-10DC  
 CY7C401-15PC  
 CY7C401-15DC  
 CY7C401-25PC  
 CY7C402-5PC  
 CY7C402-5DC  
 CY7C402-10PC  
 CY7C402-10DC  
 CY7C402-15PC  
 CY7C402-15DC  
 CY7C402-25PC  
 CY7C403-5PC  
 CY7C403-5DC  
 CY7C403-10PC  
 CY7C403-10DC  
 CY7C403-15PC  
 CY7C403-15DC  
 CY7C403-25PC  
 CY7C404-5PC  
 CY7C404-5DC  
 CY7C404-10PC  
 CY7C404-10DC  
 CY7C404-15PC  
 CY7C404-15DC  
 CY7C404-25PC  
 CY7C420-40DC  
 CY7C421-40JC  
 CY7C420-40PC  
 CY7C421-40PC  
 CY7C420-65DC  
 CY7C421-65JC  
 CY7C420-65PC  
 CY7C421-65PC  
 CY7C424-40DC  
 CY7C425-40JC  
 CY7C424-40PC  
 CY7C425-40PC  
 CY7C424-65DC  
 CY7C425-65JC  
 CY7C424-65PC  
 CY7C425-65PC  
 CY7C428-40DC  
 CY7C429-40JC  
 CY7C428-40PC  
 CY7C429-40PC  
 CY7C428-65DC  
 CY7C429-65JC  
 CY7C428-65PC  
 CY7C429-65PC

## DALLAS SEMICONDUCTOR

DS2009  
 DS2010

## AMD

67C401-10N  
 67C401-10J  
 67C401-10N  
 67C401-10J  
 67C401-15N  
 67C401-15J  
 67C401-25N  
 67C402-10N  
 67C402-10J  
 67C402-10N  
 67C402-10J  
 67C402-15N  
 67C402-15J  
 67C402-25N  
 67C4013-10N  
 67C4013-10J  
 67C4013-10N  
 67C4013-10J  
 67C4013-15N  
 67C4013-15J  
 67C4013-25N  
 67C4023-10N  
 67C4023-10J  
 67C4023-10N  
 67C4023-10J  
 67C4023-15N  
 67C4023-15J  
 67C4023-25N  
 AM7201-35DC  
 AM7201-35JC  
 AM7201-35PC  
 AM7201-35RC  
 AM7201-65DC  
 AM7201-65JC  
 AM7201-65PC  
 AM7201-65RC  
 AM7202-35DC  
 AM7202-35JC  
 AM7202-35PC  
 AM7202-35RC  
 AM7202-65DC  
 AM7202-65JC  
 AM7202-65PC  
 AM7202-65RC  
 AM7203-35DC  
 AM7203-35JC  
 AM7203-35PC  
 AM7203-35RC  
 AM7203-65DC  
 AM7203-65JC  
 AM7203-65PC  
 AM7203-65RC

## AMD

AM7201  
 AM7202

## IDT

IDT7200S/L-25P  
 IDT7200S/L-25D  
 IDT7200S/L-25J  
 IDT7200S/L-25TC  
 IDT7200S/L-25TP  
 IDT7200S/L-35P  
 IDT7200S/L-35D  
 IDT7200S/L-35J  
 IDT7200S/L-35TC  
 IDT7200S/L-35TP  
 IDT7200S/L-50P  
 IDT7200S/L-50D  
 IDT7200S/L-50J  
 IDT7200S/L-50TC  
 IDT7200S/L-50TP  
 IDT7200S/L-65P  
 IDT7200S/L-65D  
 IDT7200S/L-65J  
 IDT7200S/L-65TC  
 IDT7200S/L-65TP  
 IDT7200S/L-80P  
 IDT7200S/L-80D  
 IDT7200S/L-80J  
 IDT7200S/L-80TC  
 IDT7200S/L-80TP  
 IDT7200S/L-120P  
 IDT7200S/L-120D  
 IDT7200S/L-120J  
 IDT7200S/L-120TC  
 IDT7200S/L-120TP  
 IDT7201SA/LA-25P  
 IDT7201SA/LA-25D  
 IDT7201SA/LA-25J  
 IDT7201SA/LA-25TC  
 IDT7201SA/LA-25TP  
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 IDT7201SA/LA-35D  
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 IDT7201S/L/SA/LA-50TC  
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 IDT7201S/L/SA/LA-65J  
 IDT7201S/L/SA/LA-65TC  
 IDT7201S/L/SA/LA-65TP  
 IDT7201S/L/SA/LA-80P  
 IDT7201S/L/SA/LA-80D  
 IDT7201S/L/SA/LA-80J  
 IDT7201S/L/SA/LA-80TC  
 IDT7201S/L/SA/LA-80TP  
 IDT7201S/L/SA/LA-120P  
 IDT7201S/L/SA/LA-120D  
 IDT7201S/L/SA/LA-120J  
 IDT7201S/L/SA/LA-120TC  
 IDT7201S/L/SA/LA-120TP

## AMD

AM7200-25PC  
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 AM7201-80PC

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 IDT7202SA/LA-25J  
 IDT7202SA/LA-25TC  
 IDT7202SA/LA-25TP  
 IDT7202SA/LA-35P  
 IDT7202SA/LA-35D  
 IDT7202SA/LA-35J  
 IDT7202SA/LA-35TC  
 IDT7202SA/LA-35TP  
 IDT7202S/L/SA/LA-50P  
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 67C4023-15J  
 67C4023-15NL  
 67C4023-25N



# FIFO Competitive Cross Reference Guide

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IDT72403L-10P  
IDT72403L-10D  
IDT72403L-10J  
IDT72403L-15P  
IDT72403L-15D  
IDT72403L-15J  
IDT72403L-25P  
IDT72404L-10P  
IDT72404L-10D  
IDT72404L-10J

67C4013-10N  
67C4013-10J  
67C4013-10NL  
67C4013-15N  
67C4013-15J  
67C4013-15NL  
67C4013-25N  
67C4023-10N  
67C4023-10J  
67C4023-10NL

IDT72404L-15P  
IDT72404L-15D  
IDT72404L-15J  
IDT72404L-25P

## **MOSTEK**

MK4501-65N  
MK4501-80N  
MK4501-100N  
MK4501-120N

67C4023-15N  
67C4023-15J  
67C4023-15NL  
67C4023-25N

## **AMD**

AM7201-65PC  
AM7201-80PC  
AM7201-80PC  
AM7201-80PC

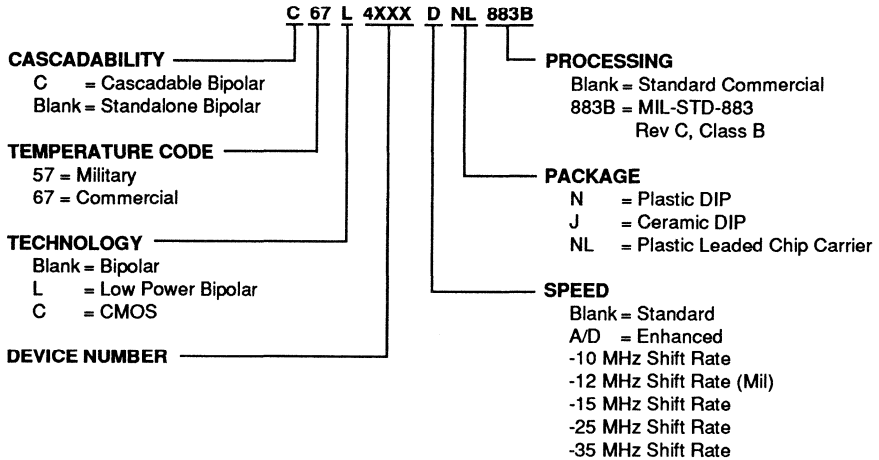
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SN74ALS236J  
SN74ALS235J  
SN74ACT7202N

## **AMD**

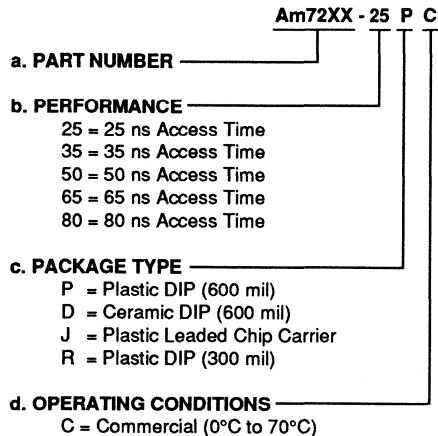
74S225N  
74S225J  
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67413AJ  
AM7202PC

# FIFO Ordering Information



## STANDARD PRODUCTS

AMD Standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

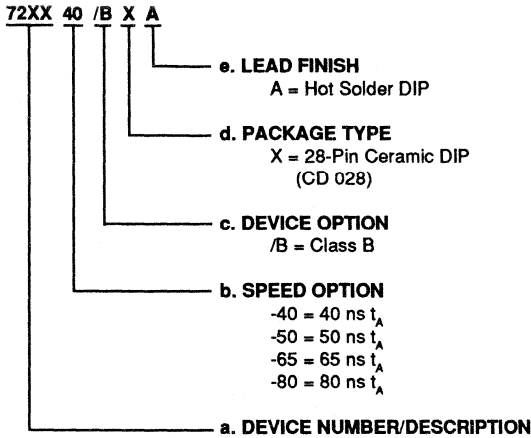


**MILITARY ORDERING INFORMATION**

**APL Products**

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

**Group A Tests**

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

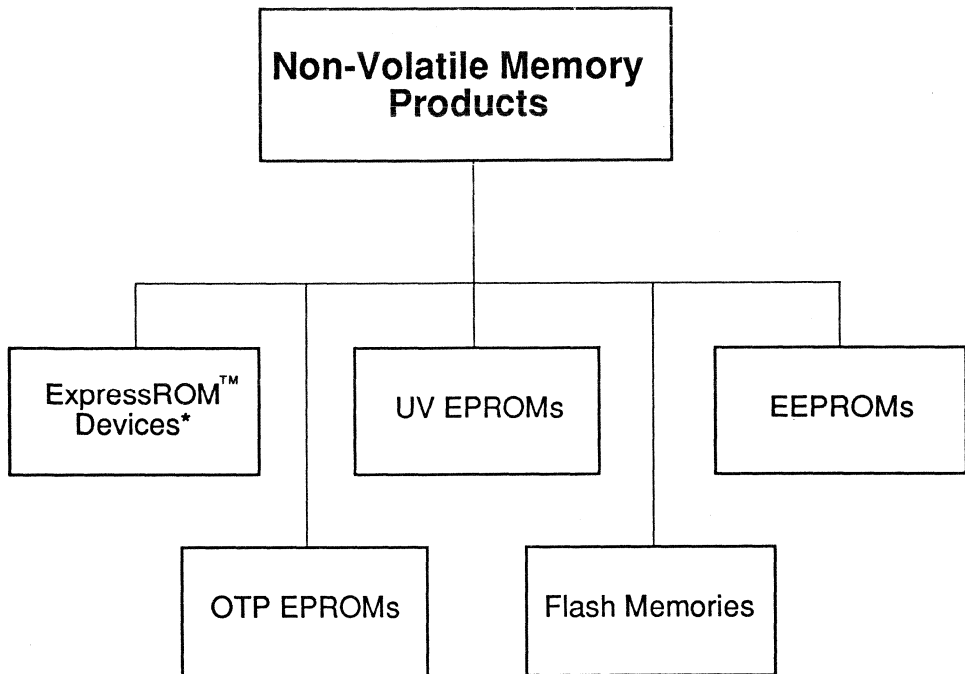
Valid Combinations	
AM72XX-40	/BXA
AM72XX-50	
AM72XX-65	
AM72XX-80	



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# Non-Volatile Memory Products Selector Guide



\* Consult the local AMD sales office to obtain more information on this product family.

## Introduction

The Non-Volatile Memory Division manufactures a broad range of high performance memory products. These products include traditional windowed EPROMs, plastic OTP EPROMs, ExpressROM™ devices, EEPROMs, and Flash Memories. They offer the system designer an extensive choice of economical alternatives for program storage.

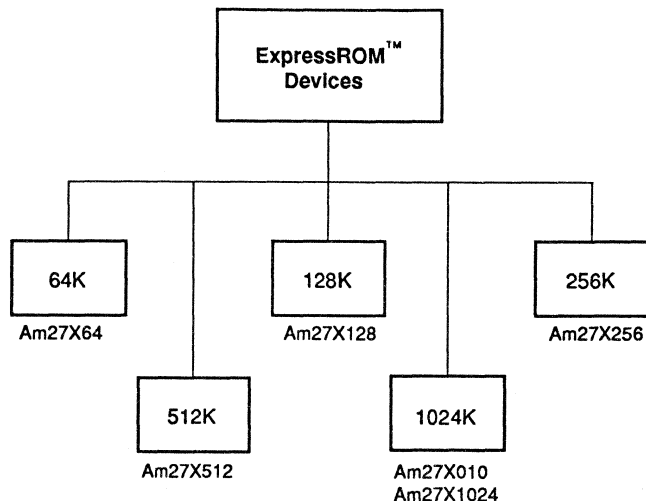
NVDs EPROM offerings are manufactured with a state-of-the-art CMOS process yielding access times as fast as 55ns. Products in production range from 64K to 1 Megabit. Also being announced this year are 2 megabit and 4 megabit devices. EPROMs are available in both windowed ceramic and One Time Programmable plastic packages.

A new concept from AMD is the ExpressROM™ device. These are quick turn ROMs produced from EPROM wafers. Lead times of these devices are typically half that of ROMs.

Flash memories will be the designer's choice for non-volatile memory in the 90s. AMD is introducing 2 families of high speed Flash devices with densities initially ranging from 256K to 1 Megabit. Offerings will be available in both EPROM and EEPROM compatible architectures.

AMD is committed to leadership in high performance CMOS non-volatile memories. These products offer industry leading speeds and densities that will contribute to the competitive advantages of your design.

# Non-Volatile Memory Products Selector Guide



## ExpressROM™ Devices\*

Part Number	Organization	Access Time(ns)	Temp Range <sup>1</sup>	Package Types <sup>2</sup>	Number of Pins DIP/PLCC	Operating Power Act/Stdby Max <sup>3</sup> (mW)	Supply Voltage
Am27X64-105	8K x 8	100	C	P, J	28/32	138/0.55	5V ± 5%
Am27X64-125	8K x 8	120	C	P, J	28/32	138/0.55	5V ± 5%
Am27X64-120	8K x 8	120	C	P, J	28/32	138/0.55	5V ± 10%
Am27X64-155	8K x 8	150	C	P, J	28/32	138/0.55	5V ± 5%
Am27X64-150	8K x 8	150	C	P, J	28/32	138/0.55	5V ± 10%
Am27X64-175	8K x 8	170	C	P, J	28/32	138/0.55	5V ± 5%
Am27X64-170	8K x 8	170	C	P, J	28/32	138/0.55	5V ± 10%
Am27X64-205	8K x 8	200	C	P, J	28/32	138/0.55	5V ± 5%
Am27X64-200	8K x 8	200	C	P, J	28/32	138/0.55	5V ± 10%
Am27X64-255	8K x 8	250	C	P, J	28/32	138/0.55	5V ± 5%
Am27X64-250	8K x 8	250	C	P, J	28/32	138/0.55	5V ± 10%
Am27X64-305	8K x 8	300	C	P, J	28/32	138/0.55	5V ± 5%
Am27X64-300	8K x 8	300	C	P, J	28/32	138/0.55	5V ± 10%
Am27X128-105	16K x 8	100	C	P, J	28/32	138/0.55	5V ± 5%
Am27X128-125	16K x 8	120	C	P, J	28/32	138/0.55	5V ± 5%
Am27X128-120	16K x 8	120	C	P, J	28/32	138/0.55	5V ± 10%
Am27X128-155	16K x 8	150	C	P, J	28/32	138/0.55	5V ± 5%
Am27X128-150	16K x 8	150	C	P, J	28/32	138/0.55	5V ± 10%
Am27X128-175	16K x 8	170	C	P, J	28/32	138/0.55	5V ± 5%
Am27X128-170	16K x 8	170	C	P, J	28/32	138/0.55	5V ± 10%
Am27X128-205	16K x 8	200	C	P, J	28/32	138/0.55	5V ± 5%
Am27X128-200	16K x 8	200	C	P, J	28/32	138/0.55	5V ± 10%
Am27X128-255	16K x 8	250	C	P, J	28/32	138/0.55	5V ± 5%
Am27X128-250	16K x 8	250	C	P, J	28/32	138/0.55	5V ± 10%
Am27X128-305	16K x 8	300	C	P, J	28/32	138/0.55	5V ± 5%
Am27X128-300	16K x 8	300	C	P, J	28/32	138/0.55	5V ± 10%
Am27X256-105	32K x 8	100	C	P, J	28/32	138/0.55	5V ± 5%
Am27X256-125	32K x 8	120	C	P, J	28/32	138/0.55	5V ± 5%
Am27X256-120	32K x 8	120	C	P, J	28/32	138/0.55	5V ± 10%
Am27X256-155	32K x 8	150	C	P, J	28/32	138/0.55	5V ± 5%
Am27X256-150	32K x 8	150	C	P, J	28/32	138/0.55	5V ± 10%
Am27X256-175	32K x 8	170	C	P, J	28/32	138/0.55	5V ± 5%
Am27X256-170	32K x 8	170	C	P, J	28/32	138/0.55	5V ± 10%
Am27X256-205	32K x 8	200	C	P, J	28/32	138/0.55	5V ± 5%

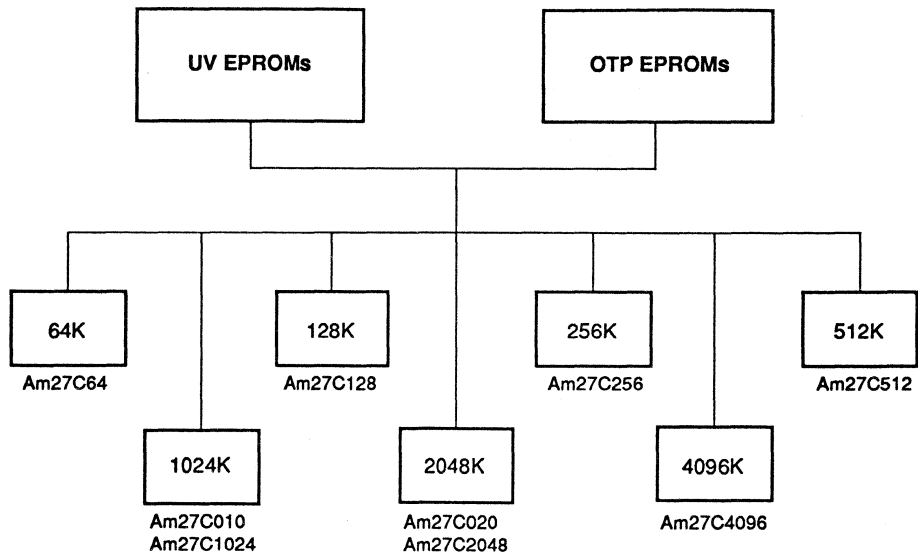
ExpressROM™ Devices (cont.)

Part Number	Organization	Access Time(ns)	Temp Range	Package Types	Number of Pins DIP/PLCC	Operating Power Act/Stdby Max (mW)	Supply Voltage
Am27X256-200	32K x 8	200	C	P, J	28/32	138/0.55	5V ± 10%
Am27X256-255	32K x 8	250	C	P, J	28/32	138/0.55	5V ± 5%
Am27X256-250	32K x 8	250	C	P, J	28/32	138/0.55	5V ± 10%
Am27X256-305	32K x 8	300	C	P, J	28/32	138/0.55	5V ± 5%
Am27X256-300	32K x 8	300	C	P, J	28/32	138/0.55	5V ± 10%
Am27X512-155	64K x 8	150	C	P, J	28/32	220/0.55	5V ± 5%
Am27X512-175	64K x 8	170	C	P, J	28/32	220/0.55	5V ± 5%
Am27X512-170	64K x 8	170	C	P, J	28/32	220/0.55	5V ± 10%
Am27X512-205	64K x 8	200	C	P, J	28/32	220/0.55	5V ± 5%
Am27X512-200	64K x 8	200	C	P, J	28/32	220/0.55	5V ± 10%
Am27X512-255	64K x 8	250	C	P, J	28/32	220/0.55	5V ± 5%
Am27X512-250	64K x 8	250	C	P, J	28/32	220/0.55	5V ± 10%
Am27X512-305	64K x 8	300	C	P, J	28/32	220/0.55	5V ± 5%
Am27X512-300	64K x 8	300	C	P, J	28/32	220/0.55	5V ± 10%
Am27X010-175	128K x 8	170	C	P, J	32/32	165/0.55	5V ± 5%
Am27X010-205	128K x 8	200	C	P, J	32/32	165/0.55	5V ± 5%
Am27X010-200	128K x 8	200	C	P, J	32/32	165/0.55	5V ± 10%
Am27X010-255	128K x 8	250	C	P, J	32/32	165/0.55	5V ± 5%
Am27X010-250	128K x 8	250	C	P, J	32/32	165/0.55	5V ± 10%
Am27X010-305	128K x 8	300	C	P, J	32/32	165/0.55	5V ± 5%
Am27X010-300	128K x 8	300	C	P, J	32/32	165/0.55	5V ± 10%
Am27X1024-175	64K x 16	170	C	P, J	40/44	275/1.1	5V ± 5%
Am27X1024-205	64K x 16	200	C	P, J	40/44	275/1.1	5V ± 5%
Am27X1024-200	64K x 16	200	C	P, J	40/44	275/1.1	5V ± 10%
Am27X1024-255	64K x 16	250	C	P, J	40/44	275/1.1	5V ± 5%
Am27X1024-250	64K x 16	250	C	P, J	40/44	275/1.1	5V ± 10%
Am27X1024-305	64K x 16	300	C	P, J	40/44	275/1.1	5V ± 5%
Am27X1024-300	64K x 16	300	C	P, J	40/44	275/1.1	5V ± 10%

\* Contact the local AMD sales office for the availability of this device family.



# Non-Volatile Memory Products Selector Guide



## UV Erasable PROMs

Part Number	Organization	Access Time(ns)	Temp Range <sup>1</sup>	Package Types <sup>2</sup>	Number of Pins DIP/LCC(PLCC)	Operating Power Act/Stdby Max <sup>3</sup> (mW)	Supply Voltage
Am27C64-55	8K x 8	55*	C	D, L	28/32	138/0.55	5V ± 5%
Am27C64-75	8K x 8	70	C	D, L	28/32	138/0.55	5V ± 5%
Am27C64-70	8K x 8	70	C	D, L	28/32	138/0.55	5V ± 10%
Am27C64-95	8K x 8	90	C, I	D, L	28/32	138/0.55	5V ± 5%
Am27C64-90	8K x 8	90	C, I, E	D, L	28/32	138/0.55	5V ± 10%
Am27C64-125	8K x 8	120	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C64-120	8K x 8	120	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C64-155	8K x 8	150	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C64-150	8K x 8	150	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C64-205	8K x 8	200	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C64-200	8K x 8	200	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C64-255	8K x 8	250	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C64-250	8K x 8	250	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C64-305	8K x 8	300	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C64-300	8K x 8	300	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C128-55	16K x 8	55*	C	D, L	28/32	138/0.55	5V ± 5%
Am27C128-75	16K x 8	70	C	D, L	28/32	138/0.55	5V ± 5%
Am27C128-70	16K x 8	70	C	D, L	28/32	138/0.55	5V ± 10%
Am27C128-95	16K x 8	90	C, I	D, L	28/32	138/0.55	5V ± 5%
Am27C128-90	16K x 8	90	C, I, E	D, L	28/32	138/0.55	5V ± 10%
Am27C128-125	16K x 8	120	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C128-120	16K x 8	120	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C128-155	16K x 8	150	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C128-150	16K x 8	150	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C128-205	16K x 8	200	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C128-200	16K x 8	200	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C128-255	16K x 8	250	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C128-250	16K x 8	250	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C128-305	16K x 8	300	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C128-300	16K x 8	300	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%



## Non-Volatile Memory Products Selector Guide

### Erasable PROMs (cont.)

Part Number	Organization	Access Time(ns)	Temp Range	Package Types	Number of Pins DIP/LCC(PLCC)	Operating Power Act/Stdby Max (mW)	Supply Voltage
Am27C256-55	32K x 8	55*	C	D, L	28/32	138/0.55	5V ± 5%
Am27C256-75	32K x 8	70	C	D, L	28/32	138/0.55	5V ± 5%
Am27C256-70	32K x 8	70	C	D, L	28/32	138/0.55	5V ± 10%
Am27C256-95	32K x 8	90	C, I	D, L	28/32	138/0.55	5V ± 5%
Am27C256-90	32K x 8	90	C, I, E	D, L	28/32	138/0.55	5V ± 10%
Am27C256-105	32K x 8	100	C, I	D, L	28/32	138/0.55	5V ± 5%
Am27C256-100	32K x 8	100	C, I, E	D, L	28/32	138/0.55	5V ± 10%
Am27C256-125	32K x 8	120	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C256-120	32K x 8	120	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C256-155	32K x 8	150	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C256-150	32K x 8	150	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C256-175	32K x 8	170	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C256-170	32K x 8	170	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C256-205	32K x 8	200	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C256-200	32K x 8	200	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C256-255	32K x 8	250	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C256-250	32K x 8	250	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C256-305	32K x 8	300	C, I	D, L, P, J	28/32	138/0.55	5V ± 5%
Am27C256-300	32K x 8	300	C, I, E	D, L, P, J	28/32	138/0.55	5V ± 10%
Am27C512-95	64K x 8	90*	C	D, L	28/32	220/0.55	5V ± 5%
Am27C512-90	64K x 8	90	C	D, L	28/32	220/0.55	5V ± 10%
Am27C512-125	64K x 8	120	C, I	D, L	28/32	220/0.55	5V ± 5%
Am27C512-120	64K x 8	120	C, I, E	D, L	28/32	220/0.55	5V ± 10%
Am27C512-155	64K x 8	150	C, I	D, L, P, J	28/32	220/0.55	5V ± 5%
Am27C512-150	64K x 8	150	C, I, E	D, L, P, J	28/32	220/0.55	5V ± 10%
Am27C512-175	64K x 8	170	C, I	D, L, P, J	28/32	220/0.55	5V ± 5%
Am27C512-170	64K x 8	170	C, I, E	D, L, P, J	28/32	220/0.55	5V ± 10%
Am27C512-205	64K x 8	200	C, I	D, L, P, J	28/32	220/0.55	5V ± 5%
Am27C512-200	64K x 8	200	C, I, E	D, L, P, J	28/32	220/0.55	5V ± 10%
Am27C512-255	64K x 8	250	C, I	D, L, P, J	28/32	220/0.55	5V ± 5%
Am27C512-250	64K x 8	250	C, I, E	D, L, P, J	28/32	220/0.55	5V ± 10%
Am27C512-305	64K x 8	300	C, I	D, L, P, J	28/32	220/0.55	5V ± 5%
Am27C512-300	64K x 8	300	C, I, E	D, L, P, J	28/32	220/0.55	5V ± 10%
Am27C010-105	128K x 8	100*	C	D, L	32/32	165/0.55	5V ± 5%
Am27C010-100	128K x 8	100	C	D, L	32/32	165/0.55	5V ± 10%
Am27C010-125	128K x 8	120	C, I	D, L	32/32	165/0.55	5V ± 5%
Am27C010-120	128K x 8	120	C, I	D, L	32/32	165/0.55	5V ± 10%
Am27C010-155	128K x 8	150	C, I	D, L	32/32	165/0.55	5V ± 5%
Am27C010-150	128K x 8	150	C, I	D, L	32/32	165/0.55	5V ± 10%
Am27C010-175	128K x 8	170	C, I	D, L, P, J	32/32	165/0.55	5V ± 5%
Am27C010-170	128K x 8	170	C, I, E	D, L, P, J	32/32	165/0.55	5V ± 10%
Am27C010-205	128K x 8	200	C, I	D, L, P, J	32/32	165/0.55	5V ± 5%
Am27C010-200	128K x 8	200	C, I, E	D, L, P, J	32/32	165/0.55	5V ± 10%
Am27C010-255	128K x 8	250	C, I	D, L, P, J	32/32	165/0.55	5V ± 5%
Am27C010-250	128K x 8	250	C, I, E	D, L, P, J	32/32	165/0.55	5V ± 10%
Am27C010-305	128K x 8	300	C, I	D, L, P, J	32/32	165/0.55	5V ± 5%
Am27C010-300	128K x 8	300	C, I, E	D, L, P, J	32/32	165/0.55	5V ± 10%
Am27C1024-105	64K x 16	100*	C	D, L	40/44	275/1.1	5V ± 5%
Am27C1024-100	64K x 16	100	C	D, L	40/44	275/1.1	5V ± 10%
Am27C1024-125	64K x 16	120	C, I	D, L	40/44	275/1.1	5V ± 5%
Am27C1024-120	64K x 16	120	C, I	D, L	40/44	275/1.1	5V ± 10%
Am27C1024-155	64K x 16	150	C, I	D, L	40/44	275/1.1	5V ± 5%
Am27C1024-150	64K x 16	150	C, I	D, L	40/44	275/1.1	5V ± 10%
Am27C1024-175	64K x 16	170	C, I	D, L, P, J	40/44	275/1.1	5V ± 5%
Am27C1024-170	64K x 16	170	C, I, E	D, L, P, J	40/44	275/1.1	5V ± 10%
Am27C1024-205	64K x 16	200	C, I	D, L, P, J	40/44	275/1.1	5V ± 5%
Am27C1024-200	64K x 16	200	C, I, E	D, L, P, J	40/44	275/1.1	5V ± 10%
Am27C1024-255	64K x 16	250	C, I	D, L, P, J	40/44	275/1.1	5V ± 5%



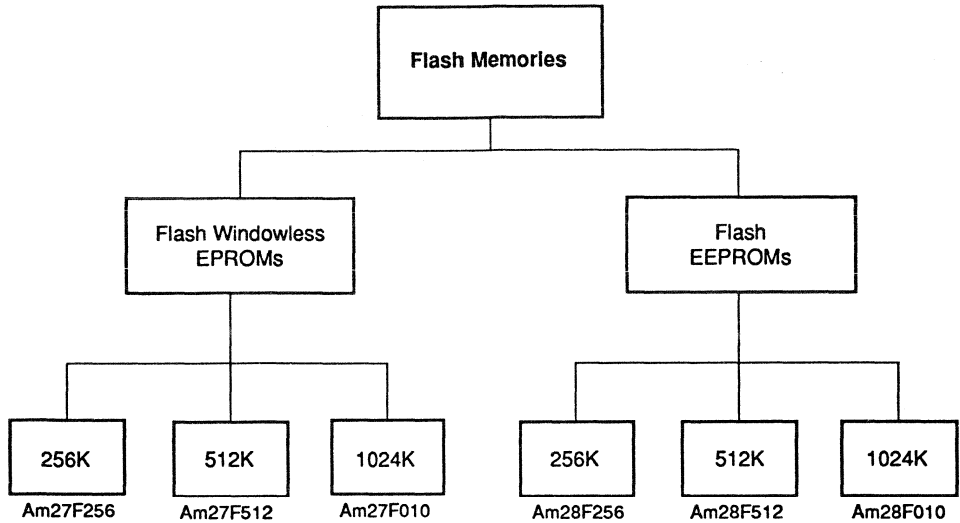
## Non-Volatile Memory Products Selector Guide

### Erasable PROMs (cont.)

Part Number	Organization	Access Time(ns)	Temp Range	Package Types	Number of Pins DIP/LCC(PLCC)	Operating Power Act/Stdby Max (mW)	Supply Voltage
Am27C1024-250	64K x 16	250	C, I, E	D, L, P, J	40/44	275/1.1	5V ± 10%
Am27C1024-305	64K x 16	300	C, I	D, L, P, J	40/44	275/1.1	5V ± 5%
Am27C1024-300	64K x 16	300	C, I, E	D, L, P, J	40/44	275/1.1	5V ± 10%
Am27C020-105**	256K x 8	100	C	D, L	32/32	165/0.55	5V ± 5%
Am27C020-100	256K x 8	100	C	D, L	32/32	165/0.55	5V ± 10%
Am27C020-125	256K x 8	120	C, I	D, L	32/32	165/0.55	5V ± 5%
Am27C020-120	256K x 8	120	C, I	D, L	32/32	165/0.55	5V ± 10%
Am27C020-155	256K x 8	150	C, I	D, L	32/32	165/0.55	5V ± 5%
Am27C020-150	256K x 8	150	C, I, E	D, L	32/32	165/0.55	5V ± 10%
Am27C020-175	256K x 8	170	C, I	D, L, P, J	32/32	165/0.55	5V ± 5%
Am27C020-170	256K x 8	170	C, I, E	D, L, P, J	32/32	165/0.55	5V ± 10%
Am27C020-205	256K x 8	200	C, I	D, L, P, J	32/32	165/0.55	5V ± 5%
Am27C020-200	256K x 8	200	C, I, E	D, L, P, J	32/32	165/0.55	5V ± 10%
Am27C2048-105**	128K x 16	100	C	D, L	40/44	165/0.55	5V ± 5%
Am27C2048-100	128K x 16	100	C	D, L	40/44	165/0.55	5V ± 10%
Am27C2048-125	128K x 16	120	C, I	D, L	40/44	165/0.55	5V ± 5%
Am27C2048-120	128K x 16	120	C, I	D, L	40/44	165/0.55	5V ± 10%
Am27C2048-155	128K x 16	150	C, I	D, L	40/44	165/0.55	5V ± 5%
Am27C2048-150	128K x 16	150	C, I, E	D, L	40/44	165/0.55	5V ± 10%
Am27C2048-175	128K x 16	170	C, I	D, L, P, J	40/44	165/0.55	5V ± 5%
Am27C2048-170	128K x 16	170	C, I, E	D, L, P, J	40/44	165/0.55	5V ± 10%
Am27C2048-205	128K x 16	200	C, I	D, L, P, J	40/44	165/0.55	5V ± 5%
Am27C2048-200	128K x 16	200	C, I, E	D, L, P, J	40/44	165/0.55	5V ± 10%
Am27C4096-125**	256K x 16	120	C	D, L	40/44	275/0.55	5V ± 5%
Am27C4096-120	256K x 16	120	C	D, L	40/44	275/0.55	5V ± 10%
Am27C4096-155	256K x 16	150	C, I	D, L	40/44	275/0.55	5V ± 5%
Am27C4096-150	256K x 16	150	C, I	D, L	40/44	275/0.55	5V ± 10%
Am27C4096-175	256K x 16	170	C, I	D, L, P, J	40/44	275/0.55	5V ± 5%
Am27C4096-170	256K x 16	170	C, I, E	D, L, P, J	40/44	275/0.55	5V ± 10%
Am27C4096-205	256K x 16	200	C, I	D, L, P, J	40/44	275/0.55	5V ± 5%
Am27C4096-200	256K x 16	200	C, I, E	D, L, P, J	40/44	275/0.55	5V ± 10%

\* Contact the local AMD sales office for the availability of this speed grade.

\*\* Contact the local AMD sales office for the availability of this device family.



Flash Windowless EPROMs\*

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Part Number	Organization	Access Time(ns)	Temp Range <sup>1</sup>	Package Types <sup>2</sup>	Number of Pins DIP/LCC(PLCC)	Operating Power Act/Stdby Max <sup>3</sup> (mW)	Supply Voltage
Am27F256-95	32K x 8	90	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F256-90	32K x 8	90	C, I	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F256-125	32K x 8	120	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F256-120	32K x 8	120	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F256-155	32K x 8	150	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F256-150	32K x 8	150	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F256-175	32K x 8	170	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F256-170	32K x 8	170	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F256-205	32K x 8	200	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F256-200	32K x 8	200	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F256-255	32K x 8	250	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F256-250	32K x 8	250	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F512-105	64K x 8	100	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F512-100	64K x 8	100	C, I	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F512-125	64K x 8	120	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F512-120	64K x 8	120	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F512-155	64K x 8	150	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F512-150	64K x 8	150	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F512-175	64K x 8	170	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F512-170	64K x 8	170	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F512-205	64K x 8	200	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F512-200	64K x 8	200	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F512-255	64K x 8	250	C, I	D, L, P, J	28/32	155/0.6	5V ± 5%
Am27F512-250	64K x 8	250	C, I, E	D, L, P, J	28/32	155/0.6	5V ± 10%
Am27F010-125	128K x 8	120	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am27F010-120	128K x 8	120	C, I	D, L, P, J	32/32	155/0.6	5V ± 10%
Am27F010-155	128K x 8	150	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am27F010-150	128K x 8	150	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am27F010-175	128K x 8	170	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%

\* Contact the local AMD sales office for the availability of this device family.  
Operating power specifications are preliminary.

## Non-Volatile Memory Products Selector Guide

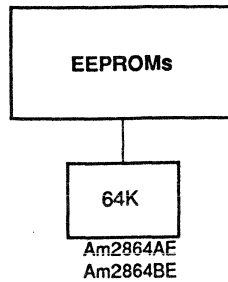
### Flash Windowless EPROMs\* (cont.)

Part Number	Organization	Access Time(ns)	Temp Range	Package Types	Number of Pins DIP/LCC(PLCC)	Operating Power Act/Stdby Max (mW)	Supply Voltage
Am27F010-170	128K x 8	170	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am27F010-205	128K x 8	200	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am27F010-200	128K x 8	200	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am27F010-255	128K x 8	250	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am27F010-250	128K x 8	250	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am27F010-305	128K x 8	300	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am27F010-300	128K x 8	300	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%

### Flash EEPROMs\*

Part Number	Organization	Access Time(ns)	Temp Range <sup>1</sup>	Package Types <sup>2</sup>	Number of Pins DIP/LCC(PLCC)	Operating Power Act/Stdby Max <sup>3</sup> (mW)	Supply Voltage
Am28F256-95	32K x 8	90	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F256-90	32K x 8	90	C, I	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F256-105	32K x 8	100	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F256-100	32K x 8	100	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F256-125	32K x 8	120	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F256-120	32K x 8	120	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F256-155	32K x 8	150	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F256-150	32K x 8	150	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F256-175	32K x 8	170	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F256-170	32K x 8	170	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F256-205	32K x 8	200	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F256-200	32K x 8	200	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F256-255	32K x 8	250	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F256-250	32K x 8	250	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F512-105	64K x 8	100	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F512-100	64K x 8	100	C, I	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F512-125	64K x 8	120	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F512-120	64K x 8	120	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F512-155	64K x 8	150	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F512-150	64K x 8	150	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F512-175	64K x 8	170	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F512-170	64K x 8	170	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F512-205	64K x 8	200	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F512-200	64K x 8	200	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F512-255	64K x 8	250	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F512-250	64K x 8	250	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F010-125	128K x 8	120	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F010-120	128K x 8	120	C, I	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F010-155	128K x 8	150	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F010-150	128K x 8	150	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F010-175	128K x 8	170	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F010-170	128K x 8	170	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F010-205	128K x 8	200	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F010-200	128K x 8	200	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F010-255	128K x 8	250	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F010-250	128K x 8	250	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%
Am28F010-305	128K x 8	300	C, I	D, L, P, J	32/32	155/0.6	5V ± 5%
Am28F010-300	128K x 8	300	C, I, E	D, L, P, J	32/32	155/0.6	5V ± 10%

\* Contact the local AMD sales office for the availability of this device family.  
Operating power specifications are preliminary.



## Electrically Erasable PROMs

Part Number	Organization	Access Time(ns)	Temp Range <sup>1</sup>	Package Types <sup>2</sup>	Number of Pins DIP/LCC(PLCC)	Operating Power Act/Stdby Max <sup>3</sup> (mW)	Supply Voltage
Am2864AE-205*	8K x 8	200	C, I	D, L, P, J	28/32	770/390	5V ± 5%
Am2864AE-200	8K x 8	200	C, I, E	D, L, P, J	28/32	770/390	5V ± 10%
Am2864AE-255	8K x 8	250	C, I	D, L, P, J	28/32	770/390	5V ± 5%
Am2864AE-250	8K x 8	250	C, I, E	D, L, P, J	28/32	770/390	5V ± 10%
Am2864AE-305	8K x 8	300	C, I	D, L, P, J	28/32	770/390	5V ± 5%
Am2864AE-300	8K x 8	300	C, I, E	D, L, P, J	28/32	770/390	5V ± 10%
Am2864AE-355	8K x 8	350	C, I	D, L, P, J	28/32	770/390	5V ± 5%
Am2864AE-350	8K x 8	350	C, I, E	D, L, P, J	28/32	770/390	5V ± 10%
Am2864BE-205*	8K x 8	200	C, I	D, L, P, J	28/32	770/390	5V ± 5%
Am2864BE-200	8K x 8	200	C, I, E	D, L, P, J	28/32	770/390	5V ± 10%
Am2864BE-255	8K x 8	250	C, I	D, L, P, J	28/32	770/390	5V ± 5%
Am2864BE-250	8K x 8	250	C, I, E	D, L, P, J	28/32	770/390	5V ± 10%
Am2864BE-305	8K x 8	300	C, I	D, L, P, J	28/32	770/390	5V ± 5%
Am2864BE-300	8K x 8	300	C, I, E	D, L, P, J	28/32	770/390	5V ± 10%
Am2864BE-355	8K x 8	350	C, I	D, L, P, J	28/32	770/390	5V ± 5%
Am2864BE-350	8K x 8	350	C, I, E	D, L, P, J	28/32	770/390	5V ± 10%

\* AE fully compliant to industry standard part with Pin 1 No Connect; BE version has Pin 1 as a Ready/Busy output.

### Notes:

#### <sup>1</sup> Temperature Range

- C = Commercial (0° to 70°C)
- I = Industrial (-40° to +85°)
- E = Extended (-55° to +125°C also available in DESC.)

#### <sup>2</sup> Package Types

- C = Ceramic DIP
- L = Rectangular Ceramic Leadless Chip Carrier
- P = Plastic DIP
- J = Rectangular Plastic Leaded Chip Carrier

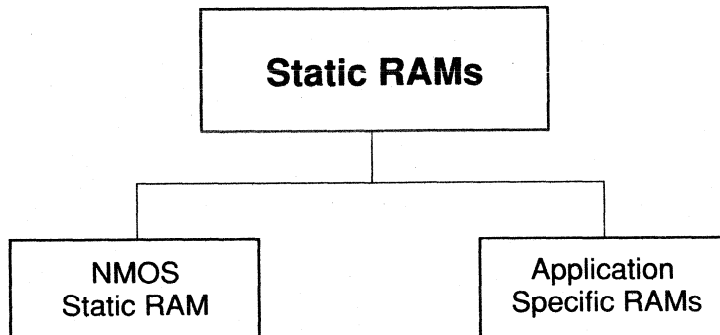
#### <sup>3</sup> Operating Power

CMOS inputs at 0 to 70°C.

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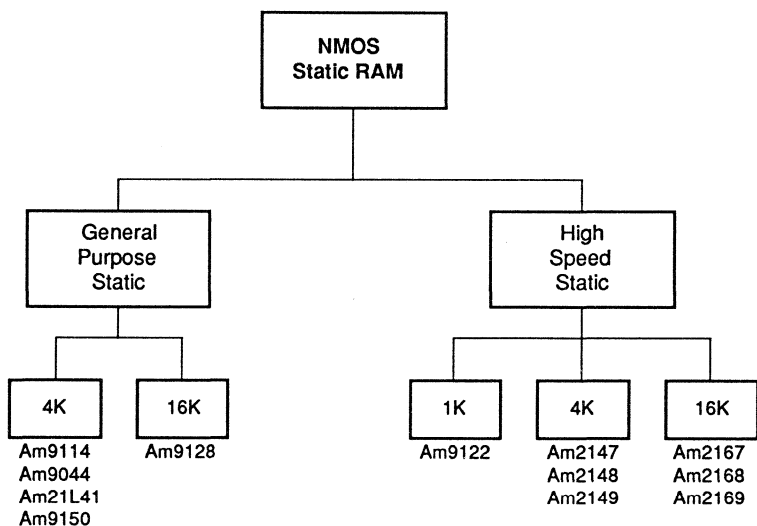
## Introduction

AMD's current product offerings in NMOS range from 1K to 16K densities.

Future offerings in ASIC RAMs include Am99C134, a 4K x 8 high speed CMOS Dual Port RAM with 35-nsec access time. Other offerings include master/slave CMOS Dual Ports with busy and interrupt features (Am99C1341/1441).

Another ASIC RAM product currently in production is Am99C10, a proprietary high performance CMOS Content Addressable Memory (CAM) with a capacity of 256 words and 48 bits per word. Am99C10 is optimized for address decoding in Local Area Networks (LAN) and bridging applications.

## Static RAMs Selector Guide



## NMOS Static RAM

### 1K Static RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation ( $\mu$ W)		Pins	Supply Voltage	Temp Range	Package
			Standby	Active				
Am9122-25	256 x 4	25	–	660	22	5	C	D, P
Am9122-35	256 x 4	35	–	660	22	5	C, M	D, P
Am91L22-25	256 x 4	35	–	440	22	5	C	D, P
Am91L22-45	256 x 4	45	–	440	22	5	C, M	D, P

### 4K Static RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation (mW)		Pins	Supply Voltage	Temp Range	Package
			Standby	Active				
Am21L41-12	4096 x 1	120	25	200	18	5	C	D, P
Am21L41-15	4096 x 1	150	25	200	18	5	C	D, P
Am21L41-20	4096 x 1	200	25	200	18	5	C	D, P
Am21L41-25	4096 x 1	250	25	250	18	5	C	D, P
Am9044B	4096 x 1	450	–	350	18	5	C, M	D, P
Am90L44B	4096 x 1	450	–	250	18	5	C, M	D, P
Am9044C	4096 x 1	300	–	350	18	5	C, M	D, P
Am90L44C	4096 x 1	300	–	250	18	5	C, M	D, P
Am9044D	4096 x 1	250	–	350	18	5	C, M	D, P
Am90L44D	4096 x 1	250	–	250	18	5	C, M	D, P
Am9044E	4096 x 1	200	–	350	18	5	C	D, P
Am90L44E	4096 x 1	200	–	250	18	5	C	D, P



4K Static RAMs (cont.)

Part Number	Organization	Access Time (ns)	Power Dissipation ( $\mu$ W)		Pins	Supply Voltage	Temp Range	Package
			Standby	Active				
Am9114B	1024 x 4	450	—	350	18	5	C, M	D, P
Am91L14B	1024 x 4	450	—	250	18	5	C, M	D, P
Am9114C	1024 x 4	300	—	350	18	5	C, M	D, P
Am91L14C	1024 x 4	300	—	250	18	5	C, M	D, P
Am9114E	1024 x 4	200	—	350	18	5	C, M	D, P
Am91L14E	1024 x 4	200	—	250	18	5	C	D, P
Am2147-35	4096 x 1	35	165	990	18	5	C	D, L, P
Am2147-45	4096 x 1	45	165	990	18	5	M	D, L, F, P
Am2147-55	4096 x 1	55	165	990	18	5	C, M	D, L, F, P
Am2147-70	4096 x 1	70	110	880	18	5	C, M	D, L, F, P
Am21L47-45	4096 x 1	45	83	688	18	5	C	D, L, P
Am21L47-55	4096 x 1	55	83	688	18	5	C	D, L, P
Am21L47-70	4096 x 1	70	83	688	18	5	C	D, L, P
Am2148-35	1024 x 4	35	165	990	18	5	C	D, L, P
Am2148-45	1024 x 4	45	165	990	18	5	C, M	D, L, P
Am2148-55	1024 x 4	55	165	990	18	5	C, M	D, L, P
Am2148-70	1024 x 4	70	165	990	18	5	C, M	D, L, P
Am21L48-45	1024 x 4	45	110	688	18	5	C	D, L, P
Am21L48-55	1024 x 4	55	110	688	18	5	C	D, L, P
Am21L48-70	1024 x 4	70	110	688	18	5	C	D, L, P
Am2149-35	1024 x 4	35	N/A	990	18	5	C	D, L, P
Am2149-45	1024 x 4	45	N/A	990	18	5	C, M	D, L, P
Am2149-55	1024 x 4	55	N/A	990	18	5	C, M	D, L, P
Am2149-70	1024 x 4	70	N/A	990	18	5	C, M	D, L, P
Am21L49-45	1024 x 4	45	N/A	688	18	5	C	D, L, P
Am21L49-55	1024 x 4	55	N/A	688	18	5	C	D, L, P
Am21L49-70	1024 x 4	70	N/A	688	18	5	C	D, L, P



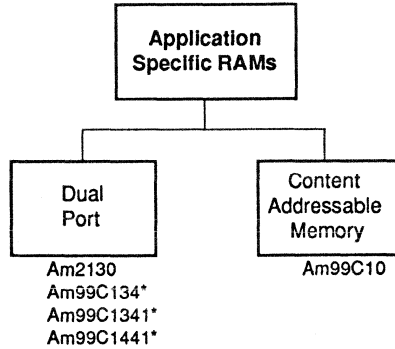
Application Specific RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation ( $\mu$ W)		Pins	Supply Voltage	Temp Range	Package
			Standby	Active				
Am9150-20	1024 x 4	20	N/A	990	24	5	C	D, L, P
Am9150-25	1024 x 4	25	N/A	990	24	5	C, M	D, L, P
Am9150-35	1024 x 4	35	N/A	990	24	5	C, M	D, L, P
Am9150-45	1024 x 4	45	N/A	990	24	5	C, M	D, L, P
Am91L50-20	1024 x 4	20	N/A	1200	24	5	C	D, P
Am91L50-25	1024 x 4	25	N/A	1200	24	5	C	D, P
Am91L50-35	1024 x 4	35	N/A	1200	24	5	C	D, P
Am91L50-45	1024 x 4	45	N/A	1200	24	5	C	D, P

## Static RAMs Selector Guide

### 16K Static RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation ( $\mu$ W)		Pins	Supply Voltage	Temp Range	Package
			Standby	Active				
Am9128-10	2048 x 8	100	83	660	24	5	C	D, P
Am9128-12	2048 x 8	120	165	825	24	5	M	D
Am9128-15	2048 x 8	150	83	550	24	5	C, M	D, P
Am9128-20	2048 x 8	200	165	660	24	5	C, M	D, P
Am9128-70	2048 x 8	70	165	770	24	5	C, M	D, P
Am9128-90	2048 x 8	90	165	990	24	5	M	D
Am2167-35	16384 x 1	35	165	660	20	5	C	D, P, L
Am2167-45	16384 x 1	45	165	660	20	5	C, M	D, P, L
Am2167-55	16384 x 1	35	165	660	20	5	C, M	D, P, L
Am2167-70	16384 x 1	70	165	660	20	5	C, M	D, P, L
Am2168-35	4096 x 4	35	165	660	20	5	C	D, P
Am2168-45	4096 x 4	45	165	550	20	5	C, M	D, P, L
Am2168-55	4096 x 4	55	165	550	20	5	C, M	D, P, L
Am2168-70	4096 x 4	70	165	550	20	5	C, M	D, P, L
Am2169-35	4096 x 4	35	N/A	550	20	5	C	D, P
Am2169-40	4096 x 4	40	N/A	550	20	5	C	D, P
Am2169-50	4096 x 4	50	N/A	550	20	5	C, M	D, P, L
Am2169-70	4096 x 4	70	N/A	550	20	5	C, M	D, P, L



## Application Specific RAMs

### Dual Port RAM

Part Number	Organization	Access Time (ns)	Power Dissipation (μW)		Pins	Supply Voltage	Temp Range	Package
			Standby	Active				
Am2130 Am2140	1024 x 8 1024 x 8	55/70/100/120 11	605/220 605/220	935 935	48 48	5 5	C, M C, M	D, P, J D, P, J
Am99C134* Am99C1341* Am99C1441* (Slave)	4096 x 8 4096 x 8 4096 x 8	35 35 35	2.5 2.5 2.5	900 900 900	48/52 52 52	5 5 5	C C C	P, J J J

\* Future Products

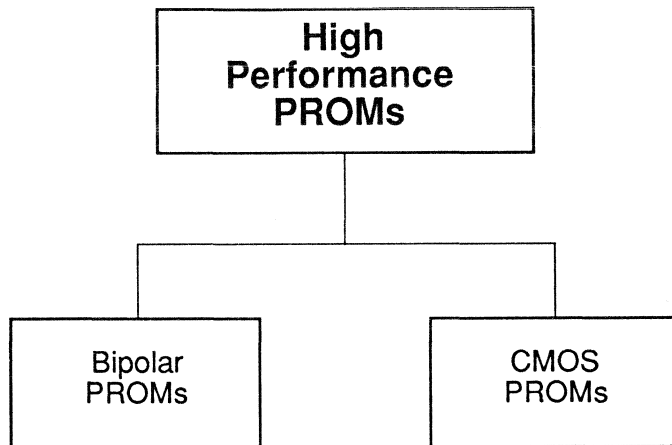


### Content Addressable Memory (CAM)

Part Number	Organization	Access Time (ns)	Power Dissipation (μW)		Pins	Supply Voltage	Temp Range	Package
			Standby	Active				
Am99C10	256 x 48	100	55	715	28	5	C	D

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## Advantages of AMD PROM Devices

- Broadest BIPOLAR/CMOS PROM product line in the industry
- AMD's IMOX™ process produces the industry's fastest bipolar PROMs
- AMD's Dual-Metal EPROM technology produces the industry's fastest CMOS PROMs
- Highly reliable, ultra-fast programming platinum-silicide fuses guarantees extremely high (>98%) programming yields for Am27Sxxx Series
- Commercial 16K, 64K, and 128K CMOS PROMs in production are pin and speed compatible with their Bipolar counterparts
- Future plans for CMOS PROMs include 16K registered and 32K densities

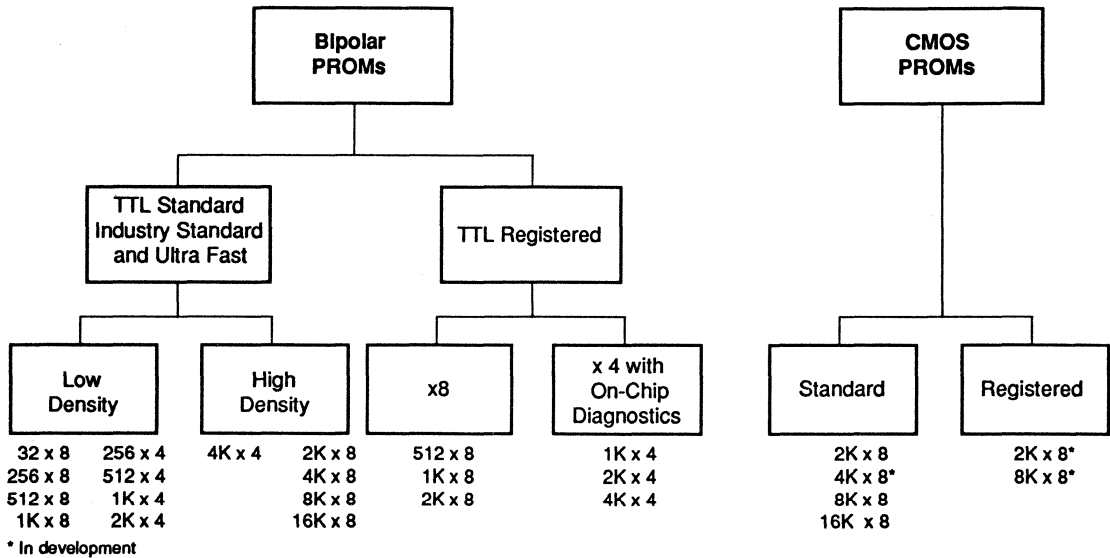
## Features/Benefits

- Low Voltage generic programming
- PNP inputs for low input current
- Three state outputs
- Registered outputs options
- Many are offered in 300-mil SKINNYDIP® package
- Some are offered in power-switched version

## Typical applications include:

- Microprogramming controls
- State machines
- Mapping functions
- Code conversion
- Character generator
- Next address generation
- Look-up table
- Logic Replacement

# High Performance PROMs Selector Guide



## Standard PROMs

AMD Part Number	Size	Organization	Output	Number of Pins	Access Times T <sub>AA</sub> C/M <sup>(1)</sup> Max	Packages
Am27LS19	256	32 x 8	TS	16	55/70	D, P, F, L, J
Am27S19	256	32 x 8	TS	16	40/50	D, P, F, L, J
Am27S19A	256	32 x 8	TS	16	25/35	D, P, F, L, J
AM27S19SA	256	32 x 8	TS	16	15/20	D, P, F, L, J
Am27S21	1024	256 x 4	TS	16	45/60	D, P, F, L, J
Am27S21A	1024	256 x 4	TS	16	30/40	D, P, F, L, J
53/63S281	2048	256 x 8	TS	20	45/50	N, NL, W, L, J
53/63S281A	2048	256 x 8	TS	20	28/40	N, NL, W, L, J
Am27S13	2048	512 x 4	TS	16	50/60	D, P, F, L, J
Am27S13A	2048	512 x 4	TS	16	30/40	D, P, F, L, J
Am27S29	4096	512 x 8	TS	20	55/70	D, P, F, L, J
Am27S29A	4096	512 x 8	TS	20	40/50	D, P, F, L, J
Am27S29SA	4096	512 x 8	TS	20	30/40	D, P, F, L, J
Am27S31	4096	512 x 8	TS	24	55/70	D, P, F, L, J
Am27S31A	4096	512 x 8	TS	24	40/50	D, P, F, L, J
Am27S33	4096	1024 x 4	TS	18	55/70	D, P, F, L, J

Notes: 1. Commercial = 0 to 75°C, V<sub>cc</sub> = 5V ±5%.  
Military = -55 to 125°C, V<sub>cc</sub> = 5V ±10%.

### Packages:

#### Am27SXXX Series

D – Ceramic DIP  
F – Flat Pack  
L – Leadless Chip Carrier  
J – Plastic Leaded Chip Carrier  
P – Plastic DIP

#### 53/63SXXX Series

J – Ceramic DIP  
JS – 300 mil Ceramic DIP  
L – Leadless Chip Carrier  
NL – Plastic Leaded Chip Carrier  
N – Plastic DIP  
NS – 300 mil Plastic DIP  
W – Ceramic Flat Pack

Standard PROMs (cont.)

AMD Part Number	Size	Organization	Output	Number of Pins	Access Times T <sub>AA</sub> C/M <sup>(1)</sup> Max	Packages
Am27S33A	4096	1024 x 4	TS	18	35/45	D, P, F, L, J
Am27S181	8192	1024 x 8	TS	24	60/80	D, P, F, L, J
Am27S181A	8192	1024 x 8	TS	24	35/50	D, P, F, L, J
Am27S281 <sup>(2)</sup>	8192	1024 x 8	TS	24	60/80	D, P
Am27S281A <sup>(2)</sup>	8192	1024 x 8	TS	24	35/50	D, P
53/63S881	8192	1024 x 8	TS	24	45/55	N,NL,NS,W,L,J,JS
53/63S881A	8192	1024 x 8	TS	24	30/45	N,NL,NS,W,L,J,JS
Am27S185	8192	2048 x 4	TS	18	50/55	D, P, F, L, J
Am27S185A	8192	2048 x 4	TS	18	35/45	D, P, F, L, J
Am27S191	16384	2048 x 8	TS	24	50/65	D, P, F, L, J
Am27S191A	16384	2048 x 8	TS	24	35/50	D, P, F, L, J
Am27PS191	16384	2048 x 8	TS	24	65/75	D, P, F, L, J
Am27PS191A	16384	2048 x 8	TS	24	50/65	D, P, F, L, J
Am27S191SA	16384	2048 x 8	TS	24	25/30	D, P, F, L, J
Am27S291 <sup>(2)</sup>	16384	2048 x 8	TS	24	50/65	D, P
Am27S291A <sup>(2)</sup>	16384	2048 x 8	TS	24	35/50	D, P
Am27S291SA <sup>(2)</sup>	16384	2048 x 8	TS	24	25/30	D, P
Am27PS291 <sup>(2)</sup>	16384	2048 x 8	TS	24	65/75	D, P
Am27PS291A <sup>(2)</sup>	16384	2048 x 8	TS	24	50/65	D, P
Am27S41	16384	4096 x 4	TS	20	50/65	D, P
Am27S41A	16384	4096 x 4	TS	20	35/50	D, P
Am27PS41	16384	4096 x 4	TS	20	-/65	D, P
Am27S43	32768	4096 x 8	TS	24	55/65	D, P, F, L
Am27S43A	32768	4096 x 8	TS	24	40/55	D, P, F, L
53/63S3281	32768	4096 x 8	TS	24	45/60	NL, N, W, L, J
53/63S3281A	32768	4096 x 8	TS	24	35/50	NL, N, W, L, J
53S3281B	32768	4096 x 8	TS	24	-/40	W, L, J
Am27S49	65536	8192 x 8	TS	24	55/65	D, F, L, P <sup>(3)</sup>
Am27S49A-45	65536	8192 x 8	TS	24	45/-	D, F, L, P <sup>(3)</sup>
Am27S49A	65536	8192 x 8	TS	24	40/55	D, F, L, P <sup>(3)</sup>
Am27S49SA	65536	8192 x 8	TS	24	25/30	D, F, L, P <sup>(3)</sup>
Am27S49-T <sup>(2)</sup>	65536	8192 x 8	TS	24	55/65	D, P <sup>(3)</sup>
Am27S49A-T <sup>(2)</sup>	65536	8192 x 8	TS	24	40/55	D, P <sup>(3)</sup>
Am27S49SA-T <sup>(2)</sup>	65536	8192 x 8	TS	24	25/30	D, P <sup>(3)</sup>
Am27S51	131072	16384 x 8	TS	28	55/65	D
Am27S51A	131072	16384 x 8	TS	28	35/45	D

Notes: 1. Commercial = 0 to 75°C, V<sub>cc</sub> = 5V ±5%. 2. SKINNYDIP® 24-pin package—300 mil lateral centers. 3. In development.  
Military = -55 to 125°C, V<sub>cc</sub> = 5V ±10%.

**Packages:**

**Am27SXXX Series**

- D — Ceramic DIP
- F — Flat Pack
- L — Leadless Chip Carrier
- J — Plastic Leaded Chip Carrier
- P — Plastic DIP

**53/63SXXX Series**

- J — Ceramic DIP
- JS — 300 mil Ceramic DIP
- L — Leadless Chip Carrier
- NL — Plastic Leaded Chip Carrier
- N — Plastic DIP
- NS — 300 mil Plastic DIP
- W — Ceramic Flat Pack



# High Performance PROMs Selector Guide

## Registered PROMs

AMD Part Number	Size	Organization	Output	Number of Pins	Set-Up Times C/M <sup>(1)</sup> Max	Clock To Output Times C/M <sup>(1)</sup> Max	Packages
Am27S25 <sup>(2)</sup>	4096	512 x 8	TS	24	50/55	27/30	D, P, F, L, J
Am27S25A <sup>(2)</sup>	4096	512 x 8	TS	24	30/35	20/25	D, P, F, L, J
Am27S25SA <sup>(2)</sup>	4096	512 x 8	TS	24	25/30	12/15	D, P, F, L, J
Am27S27	4096	512 x 8	TS	22	55/65	27/30	D, P, F
Am27S27A	4096	512 x 8	TS	22	30/35	15/20	D, P, F
Am27S35 <sup>(2)</sup>	8192	1024 x 8	TS	24	40/45	25/30	D, P, F, L, J
Am27S35A <sup>(2)</sup>	8192	1024 x 8	TS	24	35/40	20/25	D, P, F, L, J
Am27S37 <sup>(2)</sup>	8192	1024 x 8	TS	24	40/45	25/30	D, P, F, L, J
Am27S37A <sup>(2)</sup>	8192	1024 x 8	TS	24	35/40	20/25	D, P, F, L, J
53/63RS881	8192	1024 x 8	TS	24	35/45	20/25	N, NL, NS, W, L, J, JS
53/63RS881A	8192	1024 x 8	TS	24	30/40	15/20	N, NL, NS, W, L, J, JS
Am27S45 <sup>(2)</sup>	16384	2048 x 8	TS	24	45/50	25/30	D, P, F, L, J
Am27S45A <sup>(2)</sup>	16384	2048 x 8	TS	24	40/45	20/25	D, P, F, L, J
Am27S45SA <sup>(2)</sup>	16384	2048 x 8	TS	24	25/28	10/12	D, P, F, L, J
Am27S47 <sup>(2)</sup>	16384	2048 x 8	TS	24	45/50	25/30	D, P, F, L, J
Am27S47A <sup>(2)</sup>	16384	2048 x 8	TS	24	40/45	20/25	D, P, F, L, J
Am27S47SA <sup>(2)</sup>	16384	2048 x 8	TS	24	25/28	10/12	D, P, F, L, J
53/63RA1681	16384	2048 x 8	TS	24	40/45	20/25	NL, NS, W, L, JS
53/63RA1681A	16384	2048 x 8	TS	24	35/40	15/20	NL, NS, W, L, JS
53/63RS1681	16384	2048 x 8	TS	24	40/45	20/25	NL, NS, W, L, JS
53/63RS1681A	16384	2048 x 8	TS	24	35/40	15/20	NL, NS, W, L, JS

## Registered PROMs with On-Chip Diagnostics

AMD Part Number	Size	Organization	Output	Number of Pins	Set-Up Times C/M <sup>(1)</sup> Max	Clock To Output Times C/M <sup>(1)</sup> Max	Packages
Am27S85 <sup>(2)</sup>	16384	4096 x 4	TS	24	35/40	15/20	D, P, F, L, J
Am27S85A <sup>(2)</sup>	16384	4096 x 4	TS	24	27/30	12/17	D, P, F, L, J

Notes: 1. Commercial = 0 to 75°C, V<sub>cc</sub> = 5V ±5%.  
 Military = -55 to 125°C, V<sub>cc</sub> = 5V ±10%.

### Packages:

#### Am27SXXX Series

D – Ceramic DIP  
 F – Flat Pack  
 L – Leadless Chip Carrier  
 J – Plastic Leaded Chip Carrier  
 P – Plastic DIP

#### 53/63SXXX Series

J – Ceramic DIP  
 JS – 300 mil Ceramic DIP  
 L – Leadless Chip Carrier  
 NL – Plastic Leaded Chip Carrier  
 N – Plastic DIP  
 NS – 300 mil Plastic DIP  
 W – Ceramic Flat Pack



## CMOS PROMs

Part Number	Size	Organization	Output	Number of Pins	Access Times $T_{AA}/C/M^{(1)}$ Max	Packages
Am27C49-35	64K	8K x 8	TS	24	35/-	D
Am27C49-45	64K	8K x 8	TS	24	45/45 <sup>(3)</sup>	D
Am27C49-55	64K	8K x 8	TS	24	55/55 <sup>(3)</sup>	D
Am27C191-25	16K	2K x 8	TS	24	25/-	D
Am27C191-35	16K	2K x 8	TS	24	35/35 <sup>(3)</sup>	D
Am27C191-45	16K	2K x 8	TS	24	45/45 <sup>(3)</sup>	D
Am27C291-25 <sup>(2)</sup>	16K	2K x 8	TS	24	255/-	D
Am27C291-35 <sup>(2)</sup>	16K	2K x 8	TS	24	35/35 <sup>(3)</sup>	D
Am27C291-45 <sup>(2)</sup>	16K	2K x 8	TS	24	45/45 <sup>(3)</sup>	D
Am27C51-45 <sup>(3)</sup>	128K	16K x 8	TS	28	45/-	D
Am27C51-55 <sup>(3)</sup>	128K	16K x 8	TS	28	55/55	D
Am27C51-65 <sup>(3)</sup>	128K	16K x 8	TS	28	65/65	D
Am27C45-20 <sup>(3)</sup>	16K Reg.	2K x 8	TS	24	20/-	D
Am27C45-25 <sup>(3)</sup>	16K Reg.	2K x 8	TS	24	25/25	D
Am27C45-35 <sup>(3)</sup>	16K Reg.	2K x 8	TS	24	35/35	D
Am27C43-35 <sup>(3)</sup>	32K	4K x 8	TS	24	35/35	D
Am27C43-45 <sup>(3)</sup>	32K	4K x 8	TS	24	45/45	D

- Notes: 1. Commercial = 0 to 75°C,  $V_{CC} = 5V \pm 5\%$ .  
 Military = -55 to 125°C,  $V_{CC} = 5V \pm 10\%$ .  
 2. SKINNYDIP 24-pin package—300 mil lateral centers.  
 3. In development.

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### Packages:

#### Am27SXXX Series

- D — Ceramic DIP  
 F — Flat Pack  
 L — Leadless Chip Carrier  
 J — Plastic Leaded Chip Carrier  
 P — Plastic DIP

#### 53/63SXXX Series

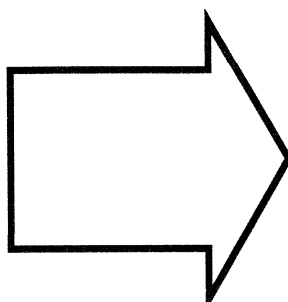
- J — Ceramic DIP  
 JS — 300 mil Ceramic DIP  
 L — Leadless Chip Carrier  
 NL — Plastic Leaded Chip Carrier  
 N — Plastic DIP  
 NS — 300 mil Plastic DIP  
 W — Ceramic Flat Pack

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Advanced  
Micro  
Devices



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# Am7200-25/35/50/65/80

CMOS First-in First-out (FIFO) 256x9-Bit Buffer

## DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 256x9 organization
- Cycle times of 35/45/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption
  - 60 mA max, -35/50/65/80
  - 70 mA max, -25
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for XI - CMOS threshold
- Functional and pin compatible with industry standard devices

## GENERAL DESCRIPTION

The Am7200 is a RAM-based CMOS FIFO that is 256 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7200 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7200 useful in communication, image processing, mass storage, DSP, and printing systems.

2

## BLOCK DIAGRAM

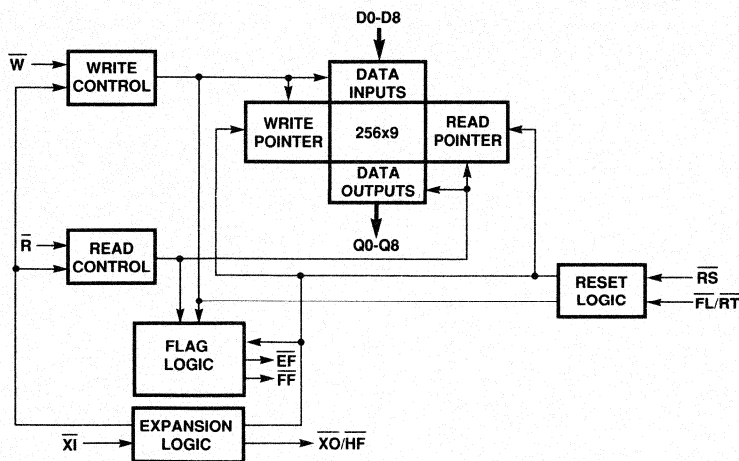
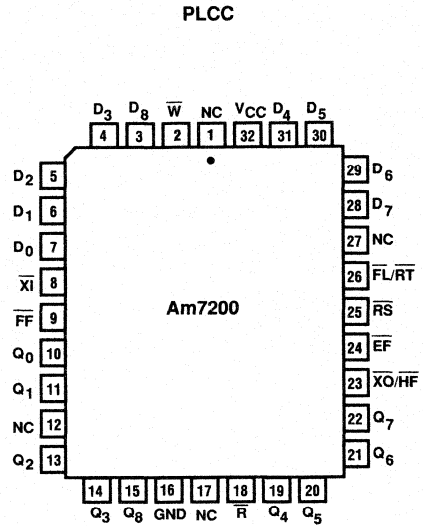
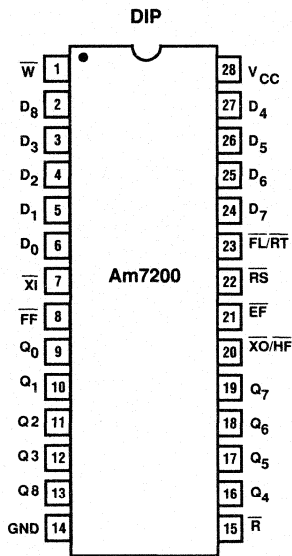


Figure 1.

## CONNECTION DIAGRAMS



Note: Pin 1 is marked for orientation.

**Pin Designations:**  $\overline{W}$  = Write  
 $\overline{R}$  = Read  
 $\overline{RS}$  = Reset  
 $\overline{FL/RT}$  = First Load/Retransmit  
 $D_x$  = Data In  
 $Q_x$  = Data Out  
 $\overline{XI}$  = Expansion In  
 $\overline{XO/HF}$  = Expansion Out/Half-Full Flag  
 $\overline{FF}$  = Full Flag  
 $\overline{EF}$  = Empty Flag  
 $V_{CC}$  = Supply Voltage  
 $GND$  = Ground  
 $NC$  = No Connect

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

- Part Number
- Performance
- Package Type
- Operating Conditions

NOTE: AMD has changed the part numbers on the high-density FIFOs. The following part numbers are equivalent devices with the same DC and AC electrical characteristics.

New P/N	Old P/N
Am7200	67C4500
Am7201	67C4501
Am7202	67C4502
Am7203	67C4503
Am7204	—

### Am7200 - 25 P C

**a. PART NUMBER**

**b. PERFORMANCE**  
**ACCESS TIME**

25 = 25 ns  
 35 = 35 ns  
 50 = 50 ns  
 65 = 65 ns  
 80 = 80 ns

**c. PACKAGE TYPE**

P = Plastic DIP (600 mil) - PD 028  
 D = Ceramic DIP (600 mil) - CD 028  
 J = Plastic Leaded Chip Carrier - PL 032  
 R = Plastic DIP (300 mil) - PD 3028

**d. OPERATING CONDITIONS**

C = Commercial (0°C to 70°C)



## ABSOLUTE MAXIMUM RATINGS

Supply voltage,  $V_{CC}$  ..... -0.5 V to + 7.0 V  
 Input voltage ..... -0.5 V to  $V_{CC} + 0.5$  V  
 Operating temperature ..... 0°C to + 70°C  
 Storage temperature ..... -55°C to + 150°C  
 Power dissipation ..... 1.0 W  
 DC output current ..... 50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## DC CHARACTERISTICS Commercial: $V_{CC} = 5 \text{ V} \pm 10\%$ , $T_A = 0^\circ\text{C}$ to + 70°C

Parameter Symbol	Parameter Description	Am7200-25 $t_A = 25 \text{ ns}$		Am7200-35 $t_A = 35 \text{ ns}$		Am7200-50 $t_A = 50 \text{ ns}$		Am7200-65 $t_A = 65 \text{ ns}$		Am7200-80 $t_A = 80 \text{ ns}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$I_{IL}$	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	-1	1	$\mu\text{A}$
$I_{IO}$	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$V_{IH}$	Input High Voltage (all inputs except $\overline{XI}$ ) (Note 3)	2.0	-	2.0	-	2.0	-	2.0	-	2.0	-	V
$V_{IL}$	Input Low Voltage (all inputs except $\overline{XI}$ ) (Note 3)	-	0.8	-	0.8	-	0.8	-	0.8	-	0.8	V
$V_{IHxI}$	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	-	3.5	-	3.5	-	3.5	-	3.5	-	V
$V_{ILxI}$	Input Low Voltage, $\overline{XI}$ (Note 3)	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	V
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2 \text{ mA}$	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	V
$V_{OL}$	Output Logic "0" voltage $I_{OL} = 8 \text{ mA}$	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V
$I_{CC1}$	Average $V_{CC}$ Power Supply Current (Note 4)	-	70	-	60	-	60	-	60	-	60	mA
$I_{CC2}$	Average Standby Current ( $R = W = \overline{RS} = \overline{FL}/RT = V_{IH}$ ) (Note 4)	-	20	-	20	-	20	-	20	-	20	mA
$I_{CC3}$	Power Down Current (all inputs = $V_{CC} - 0.2 \text{ V}$ ) (Note 4)	-	5	-	5	-	5	-	5	-	5	mA

Notes: 1. Measurements with  $GND \leq V_{IN} \leq V_{CC}$ .

2.  $R \geq V_{IH}$ ,  $GND \leq V_{OUT} \leq V_{CC}$ .

3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

4.  $I_{CC}$  measurements are made with outputs open.

2

**AC CHARACTERISTICS**  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ 

Parameter Symbol	Parameter Description	Figures	Am7200-25 Min. Max.	Am7200-35 Min. Max.	Am7200-50 Min. Max.	Am7200-65 Min. Max.	Am7200-80 Min. Max.	Unit
<b>Write and Flag Timing</b>								
$t_{WC}$	Write Cycle Time	3	35	45	65	80	100	ns
$t_{WPW}$	Write Pulse Width	3	25	35	50	65	80	ns
$t_{WR}$	Write Recovery Time	3	10	10	15	15	20	ns
$t_{DS}$	Data Setup Time	3,9	15	18	30	30	40	ns
$t_{DH}$	Data Hold Time	3,9	0	0	5	10	10	ns
$t_{WFF}$	Write LOW to Full Flag LOW	6,9	25	30	45	60	60	ns
$t_{WHF}$	Write LOW to Half-Full Flag LOW	5	35	45	65	80	100	ns
$t_{WEF}$	Write HIGH to Empty Flag HIGH	4,8	25	30	45	60	60	ns
$t_{WLZ}$	Write pulse HIGH to data bus at LOW Z (Note 1)	8	5	10	15	15	20	ns
<b>Read and Flag Timing</b>								
$t_{RC}$	Read Cycle Time	3	35	45	65	80	100	ns
$t_A$	Access Time	3,4,8,9	25	35	50	65	80	ns
$t_{RR}$	Read Recovery Time	3	10	10	15	15	20	ns
$t_{RPW}$	Read Pulse Width	3	25	35	50	65	80	ns
$t_{RLZ}$	Read pulse LOW to data bus at LOW Z (Note 1)	3	5	5	10	10	10	ns
$t_{DV}$	Data Valid from read pulse HIGH	3	5	5	5	5	5	ns
$t_{RHZ}$	Read pulse HIGH to data bus at HIGH Z (Note 1)	3	18	20	30	30	30	ns
$t_{RFF}$	Read HIGH to Full Flag HIGH	6,9	25	30	45	60	60	ns
$t_{RHF}$	Read HIGH to Half-Full-Flag HIGH	5	35	45	65	80	100	ns
$t_{REF}$	Read LOW to Empty Flag LOW	4,8	25	30	45	60	60	ns
<b>Reset Timing</b>								
$t_{RSC}$	Reset Cycle Time	2	35	45	65	80	100	ns
$t_{RS}$	Reset Pulse Width	2	25	35	50	65	80	ns
$t_{RSS}$	Reset Setup Time	2	25	35	50	65	80	ns
$t_{RSR}$	Reset Recovery Time	2	10	10	15	15	20	ns
$t_{EFL}$	Reset to Empty Flag LOW	2	35	45	65	80	100	ns
$t_{HFH}$	Reset to Half-Full Flag High	2	35	45	65	80	100	ns
$t_{FFH}$	Reset to Full Flag HIGH	2	35	45	65	80	100	ns
<b>Retransmit Timing</b>								
$t_{RTC}$	Retransmit Cycle Time	7	35	45	65	80	100	ns
$t_{RT}$	Retransmit Pulse Width	7	25	35	50	65	80	ns
$t_{RTR}$	Retransmit Recovery Time	7	10	10	15	15	20	ns

Note: 1. Characterized parameters.

## FUNCTIONAL DESCRIPTION

The Am7200 CMOS FIFO is designed around a 256x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 255. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7200. The write, read, data-in and data-out lines of the Am7200 are connected in parallel, and the Expansion-Out (XO) and the Expansion-In (XI) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between XO and XI.

## OPERATIONAL DESCRIPTION

### Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of XI and FL are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read (R) and Write (W) signals must be HIGH  $t_{RSS}$  prior to and  $t_{RSR}$  after the rising edge of Reset (RS). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag (EF) being LOW, active, and both the Half-Full (HF) and Full Flag (FF) being HIGH, inactive.

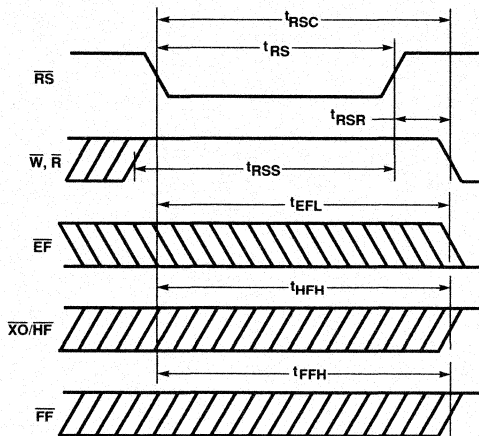


Figure 2. Reset Timing

### Writing Data To The FIFO

The HIGH state of the Full Flag ( $\overline{FF}$ ) indicates that the FIFO is capable of accepting data. The falling edge of Write (W) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8  $t_{DS}$  prior to and  $t_{DH}$  after the rising edge of W will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ( $\overline{EF}$ ) occurs  $t_{WEF}$  after the rising edge of W during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag /HF) will go LOW  $t_{WHF}$  after the falling edge of W during the write operation which creates the half-full condition. (See Figure 5.) HF will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 128 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ( $\overline{FF}$ ) goes LOW  $t_{WFF}$  after the falling edge of W during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 256 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

### Reading Data From The FIFO

The HIGH state of the Empty Flag ( $\overline{EF}$ ) indicates that the FIFO is ready to output data. The falling edge of Read (R) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8  $t_{x}$  after the falling edge of R, and remains until  $t_{QV}$  after the rising edge of R. Q0-Q8 return to a high-impedance state when a valid read is not in progress.

The Full Flag ( $\overline{FF}$ ) will go HIGH  $t_{RFF}$  after the rising edge of R during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag (HF) will go HIGH  $t_{RHF}$  after the rising edge of R during the read operation, which eliminates the half-full condition. (See Figure 5.) HF will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 127 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of EF occurs  $t_{REF}$  after the falling edge of R during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

### Half-Full Flag

The Half-Full ( $\overline{HF}$ ) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 128 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 128 words, and Read and Write pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

HF will always settle to the correct state after the appropriate delay,  $t_{WHF}$  or  $t_{RHF}$ . This property of the Half-Full Flag is clearly a function of the dynamic relation between W and R. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

### RESET AND RETRANSMIT TRUTH TABLE Single-Device Configuration/Width-Expansion Mode

Mode	Input			Internal Status		Outputs		
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF	HF
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

- Notes: 1. Flags will change to show correct state according to write pointer.  
 2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

### RESET AND FIRST LOAD TRUTH TABLE Depth-Expansion/Compound-Expansion Mode

Mode	Input			Internal Status		Outputs	
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF
Reset—first device	0	0	$\overline{X0}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{X0}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{X0}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

- Notes: 1.  $\overline{X1}$  is connected to  $\overline{X0}$  of previous device. See Figure 12.  
 2. Same as during Reset Cycle.  
 3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

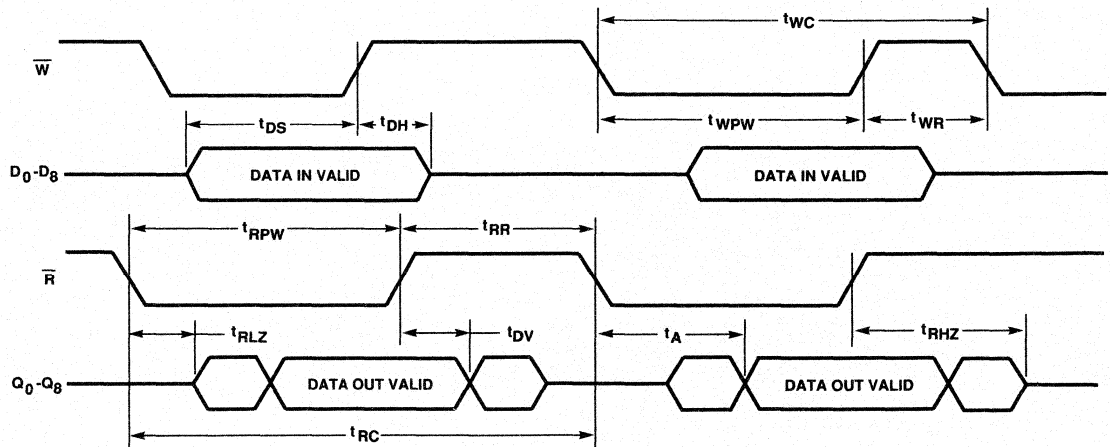


Figure 3. Asynchronous Write and Read Timing

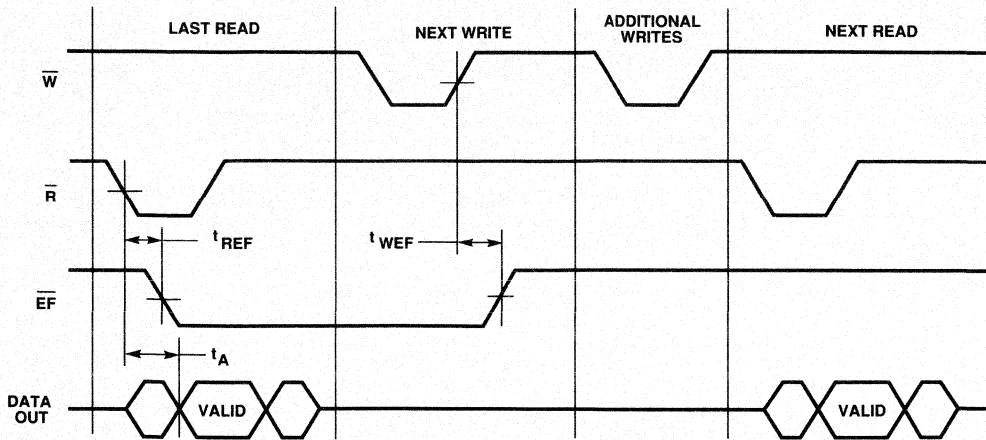
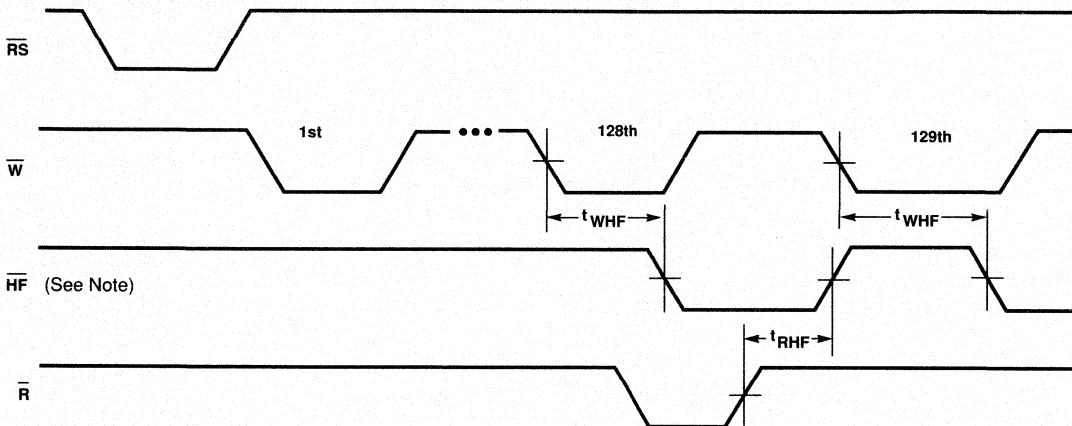


Figure 4. Empty Flag Timing



2

Note: Depending on the precise phase of  $\bar{W}$  and  $\bar{R}$ , the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when  $\bar{W}$  and  $\bar{R}$  are operating asynchronously near half full.

Figure 5. Half-Full Flag Timing

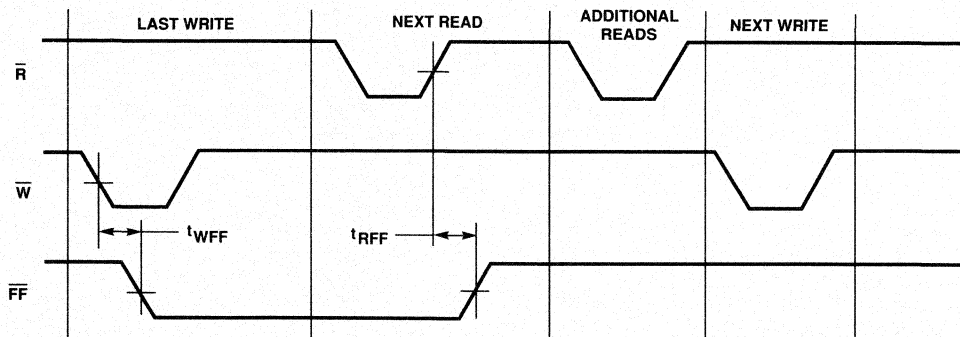


Figure 6. Full Flag Timing

## Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 256 or less writes between reset cycles.

The  $\overline{\text{FL}}/\overline{\text{RT}}$  is used as the Retransmit ( $\overline{\text{RT}}$ ) input in Single-Device Mode.  $\overline{\text{RT}}$ , an active LOW-going pulse of at least  $t_{\text{RT}}$  in duration, returns the internal read pointer to address zero and leaves the write pointer unaffected.  $\overline{\text{W}}$  and  $\overline{\text{R}}$  must both be HIGH during the retransmit cycle. The first write or read cycle should not start until  $t_{\text{RTR}}$  after the rising edge of  $\overline{\text{RT}}$ . The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO  $t_{\text{RTC}}$  after the falling edge of  $\overline{\text{RT}}$ . (See Figure 7 and Table 1).

## Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ( $\overline{\text{XI}}$ ) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7200 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag.

These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time ( $t_{\text{WFF}}$ ,  $t_{\text{WHF}}$ ,  $t_{\text{WFF}}$ ,  $t_{\text{REF}}$ ,  $t_{\text{RHF}}$ , and  $t_{\text{WFF}}$ ) for each flag has elapsed.

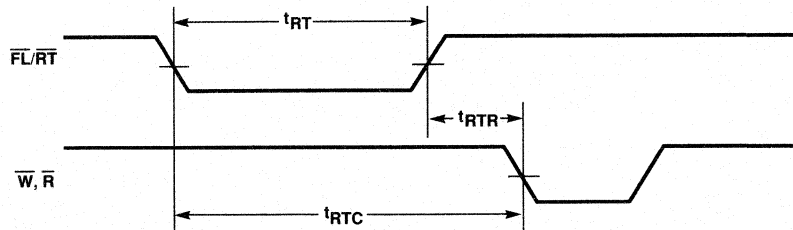
## Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ( $\overline{\text{XO}}$ ) of one device must be connected to Expansion In ( $\overline{\text{XI}}$ ) of the next device, with  $\overline{\text{XO}}$  of the last device being connected to  $\overline{\text{XI}}$  of the first device. The device that is to receive data first has its First Load ( $\overline{\text{FL}}$ ) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using  $\overline{\text{XO}}$  and  $\overline{\text{XI}}$ . A LOW-going pulse on  $\overline{\text{XO}}$  occurs when the last physical location of an active device, address 255, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the FF outputs together. Likewise, a composite Empty Flag is created by OR-ing all the EF outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

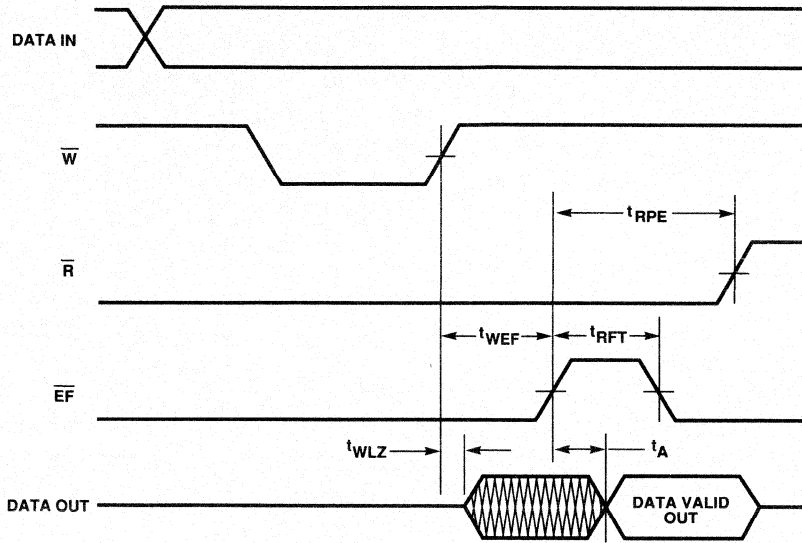
## Compound Expansion

FIFOs of greater width and depth than the Am7200 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)



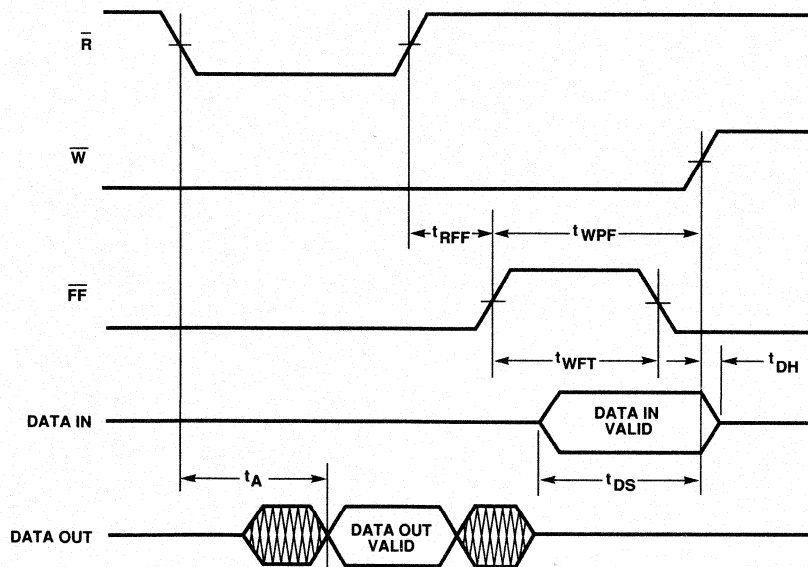
Note:  $\overline{\text{EF}}$ ,  $\overline{\text{HF}}$  and  $\overline{\text{FF}}$  may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at  $t_{\text{RTC}}$ .

Figure 7. Retransmit Timing



Note: ( $t_{RPE} = t_{RPW}$ ,  $t_{RFT} = t_{REF}$ )

Figure 8. Read Data Flow-Through Mode



Note: ( $t_{WPF} = t_{WPW}$ ,  $t_{WFT} = t_{WFF}$ )

Figure 9. Write Data Flow-Through Mode

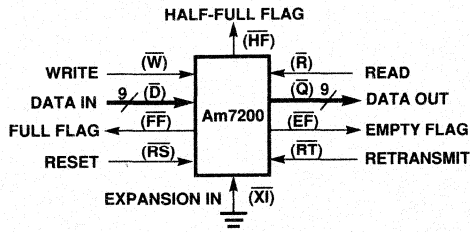


Figure 10. Single FIFO Configuration

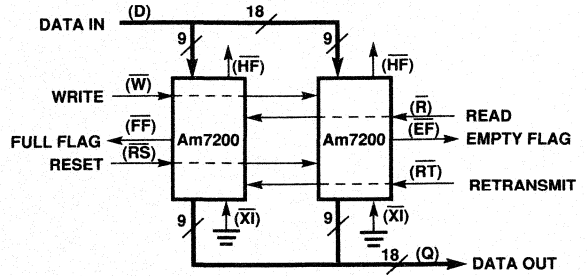


Figure 11. Width-Expansion to Form a 256x18 FIFO

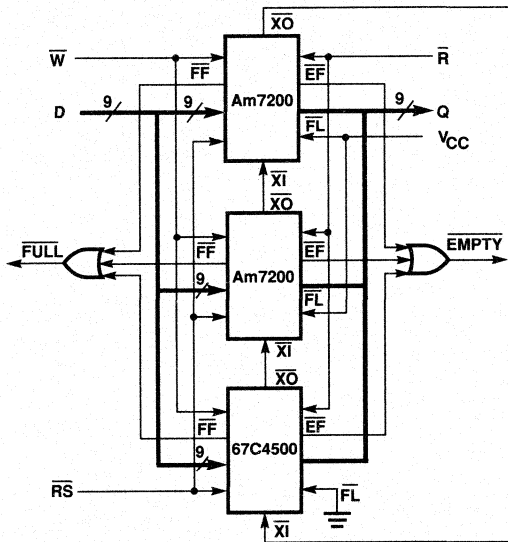


Figure 12. Depth-Expansion to Form a 768x9 FIFO

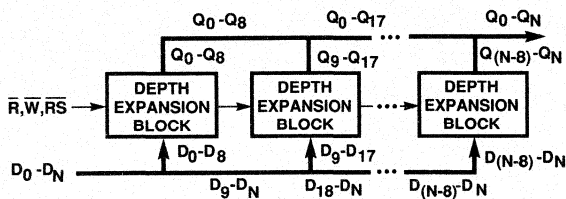


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

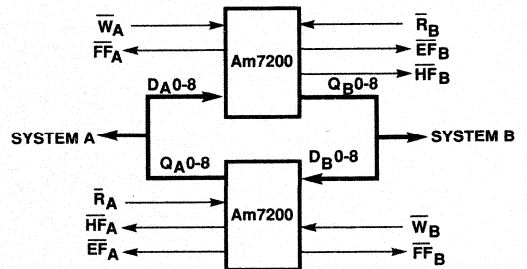
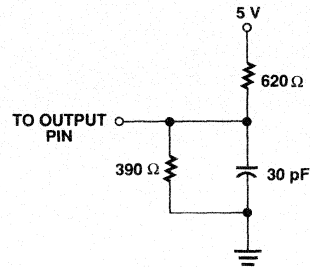


Figure 14. Bidirectional FIFO Mode



## AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



\* Includes jig and scope capacitances.

Figure 15. A.C. Test Load

## CAPACITANCE ( $T_A = + 25^\circ\text{C}$ , $f = 1.0\text{ MHz}$ )

Symbol	Parameter (Note 1)	Conditions	Typ.	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$	5	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$	7	pF

Note: 1. For reference only.



# Am7201-25/35/50/65/80

CMOS First-In First Out (FIFO) 512x9-Bit Buffer

## DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 512x9 organization
- Cycle times of 35/45/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption
  - 60 mA max, -35/50/65/80
  - 70 mA max, -25
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for  $\overline{X1}$  - CMOS threshold
- Functional and pin compatible with industry standard devices

## GENERAL DESCRIPTION

The Am7201 is a RAM-based CMOS FIFO that is 512 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7201 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7201 useful in communication, image processing, mass storage, DSP, and printing systems.

## BLOCK DIAGRAM

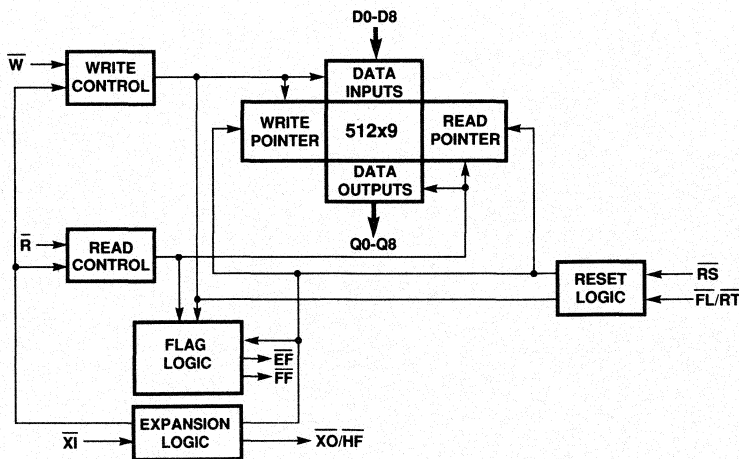
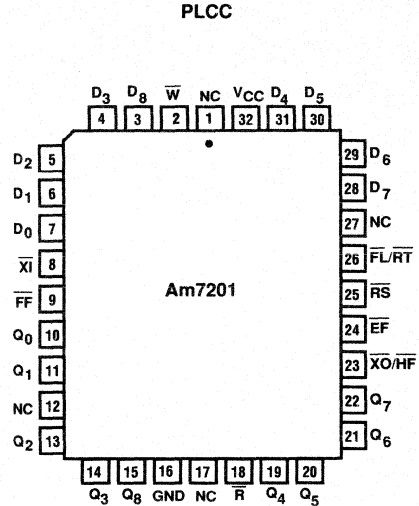
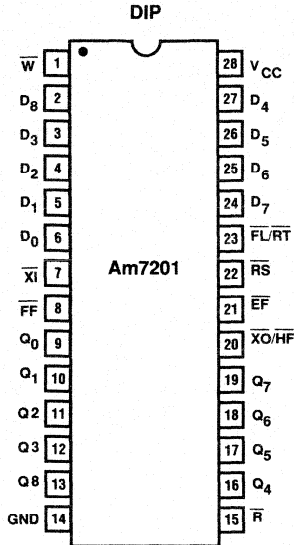


Figure 1.

## CONNECTION DIAGRAMS



Note: Pin 1 is marked for orientation.

**Pin Designations:**

- $\bar{W}$  = Write
- $\bar{R}$  = Read
- RS = Reset
- FL/RT = First Load/Retransmit
- $D_x$  = Data In
- $Q_x$  = Data Out
- $\bar{X}I$  = Expansion In
- $\bar{X}O/HF$  = Expansion Out/Half-Full Flag
- FF = Full Flag
- EF = Empty Flag
- $V_{CC}$  = Supply Voltage
- GND = Ground
- NC = No Connect

2

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

- a. Part Number
- b. Performance
- c. Package Type
- d. Operating Conditions

NOTE: AMD has changed the part numbers on the high-density FIFOs. The following part numbers are equivalent devices with the same DC and AC electrical characteristics.

New P/N	Old P/N
Am7200	67C4500
Am7201	67C4501
Am7202	67C4502
Am7203	67C4503
Am7204	—

### Am7201 - 25 P C

- a. PART NUMBER
- b. PERFORMANCE  
ACCESS TIME  
25 = 25 ns  
35 = 35 ns  
50 = 50 ns  
65 = 65 ns  
80 = 80 ns
- c. PACKAGE TYPE  
P = Plastic DIP (600 mil) - PD 028  
D = Ceramic DIP (600 mil) - CD 028  
J = Plastic Leaded Chip Carrier - PL 032  
R = Plastic DIP (300 mil) - PD 3028
- d. OPERATING CONDITIONS  
C = Commercial (0°C to 70°C)

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to + 7.0 V
Input voltage .....	-0.5 V to $V_{CC} + 0.5$ V
Operating temperature .....	0°C to + 70°C
Storage temperature .....	-55°C to + 150°C
Power dissipation .....	1.0 W
DC output current .....	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## DC CHARACTERISTICS Commercial: $V_{CC} = 5\text{ V} \pm 10\%$ , $T_A = 0^\circ\text{C}$ to + 70°C

Parameter Symbol	Parameter Description	Am7201-25 $t_A = 25\text{ ns}$		Am7201-35 $t_A = 35\text{ ns}$		Am7201-50 $t_A = 50\text{ ns}$		Am7201-65 $t_A = 65\text{ ns}$		Am7201-80 $t_A = 80\text{ ns}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$I_{IL}$	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	-1	1	$\mu\text{A}$
$I_{IO}$	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$V_{IH}$	Input High Voltage (all inputs except $\overline{XI}$ ) (Note 3)	2.0	-	2.0	-	2.0	-	2.0	-	2.0	-	V
$V_{IL}$	Input Low Voltage (all inputs except $\overline{XI}$ ) (Note 3)	-	0.8	-	0.8	-	0.8	-	0.8	-	0.8	V
$V_{IH(XI)}$	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	-	3.5	-	3.5	-	3.5	-	3.5	-	V
$V_{IL(XI)}$	Input Low Voltage, $\overline{XI}$ (Note 3)	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	V
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2\text{ mA}$	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	V
$V_{OL}$	Output Logic "0" voltage $I_{OL} = 8\text{ mA}$	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V
$I_{CC1}$	Average $V_{CC}$ Power Supply Current (Note 4)	-	70	-	60	-	60	-	60	-	60	mA
$I_{CC2}$	Average Standby Current ( $\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/RT = V_{IH}$ ) (Note 4)	-	20	-	20	-	20	-	20	-	20	mA
$I_{CC3}$	Power Down Current (all inputs = $V_{CC} - 0.2\text{ V}$ ) (Note 4)	-	5	-	5	-	5	-	5	-	5	mA

- Notes:
1. Measurements with  $GND \leq V_{IN} \leq V_{CC}$ .
  2.  $\overline{R} \geq V_{IH}$ ,  $GND \leq V_{OUT} \leq V_{CC}$ .
  3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
  4.  $I_{CC}$  measurements are made with outputs open.

## AC CHARACTERISTICS $V_{CC} = 5 V \pm 10\%$ , $T_A = 0^\circ C$ to $+70^\circ C$

Parameter Symbol	Parameter Description	Figures	Am7201-25	Am7201-35	Am7201-50	Am7201-65	Am7201-80	Unit
			Min.	Max.	Min.	Max.	Min.	
<b>Write and Flag Timing</b>								
$t_{WC}$	Write Cycle Time	3	35	45	65	80	100	ns
$t_{WPW}$	Write Pulse Width	3	25	35	50	65	80	ns
$t_{WR}$	Write Recovery Time	3	10	10	15	15	20	ns
$t_{DS}$	Data Setup Time	3,9	15	18	30	30	40	ns
$t_{DH}$	Data Hold Time	3,9	0	0	5	10	10	ns
$t_{WFF}$	Write LOW to Full Flag LOW	6,9	25	30	45	60	60	ns
$t_{WHF}$	Write LOW to Half-Full Flag LOW	5	35	45	65	80	100	ns
$t_{WEF}$	Write HIGH to Empty Flag HIGH	4,8	25	30	45	60	60	ns
$t_{WLZ}$	Write pulse HIGH to data bus at LOW Z (Note 1)	8	5	10	15	15	20	ns
<b>Read and Flag Timing</b>								
$t_{RC}$	Read Cycle Time	3	35	45	65	80	100	ns
$t_A$	Access Time	3,4,8,9	25	35	50	65	80	ns
$t_{RR}$	Read Recovery Time	3	10	10	15	15	20	ns
$t_{RPW}$	Read Pulse Width	3	25	35	50	65	80	ns
$t_{RLZ}$	Read pulse LOW to data bus at LOW Z (Note 1)	3	5	5	10	10	10	ns
$t_{DV}$	Data Valid from read pulse HIGH	3	5	5	5	5	5	ns
$t_{RHZ}$	Read pulse HIGH to data bus at HIGH Z (Note 1)	3	18	20	30	30	30	ns
$t_{RFF}$	Read HIGH to Full Flag HIGH	6,9	25	30	45	60	60	ns
$t_{RHF}$	Read HIGH to Half Full-Flag HIGH	5	35	45	65	80	100	ns
$t_{REF}$	Read LOW to Empty Flag LOW	4,8	25	30	45	60	60	ns
<b>Reset Timing</b>								
$t_{HSC}$	Reset Cycle Time	2	35	45	65	80	100	ns
$t_{HS}$	Reset Pulse Width	2	25	35	50	65	80	ns
$t_{RSS}$	Reset Setup Time	2	25	35	50	65	80	ns
$t_{RSR}$	Reset Recovery Time	2	10	10	15	15	20	ns
$t_{EFL}$	Reset to Empty Flag LOW	2	35	45	65	80	100	ns
$t_{HFH}$	Reset to Half-Full Flag High	2	35	45	65	80	100	ns
$t_{FFH}$	Reset to Full Flag HIGH	2	35	45	65	80	100	ns
<b>Retransmit Timing</b>								
$t_{RTC}$	Retransmit Cycle Time	7	35	45	65	80	100	ns
$t_{RT}$	Retransmit Pulse Width	7	25	35	50	65	80	ns
$t_{RTR}$	Retransmit Recovery Time	7	10	10	15	15	20	ns

Note: 1. Characterized parameters.

2

## FUNCTIONAL DESCRIPTION

The Am7201 CMOS FIFO is designed around a 512x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 511. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7201. The write, read, data-in and data-out lines of the Am7201 are connected in parallel, and the Expansion-Out (XO) and the Expansion-In (XI) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between  $\overline{XO}$  and  $\overline{XI}$ .

## OPERATIONAL DESCRIPTION

### Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of XI and FL are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ( $\overline{R}$ ) and Write ( $\overline{W}$ ) signals must be HIGH  $t_{RSS}$  prior to and  $t_{RSR}$  after the rising edge of Reset ( $\overline{RS}$ ). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ( $\overline{EF}$ ) being LOW, active, and both the Half-Full (HF) and Full Flag (FF) being HIGH, inactive.

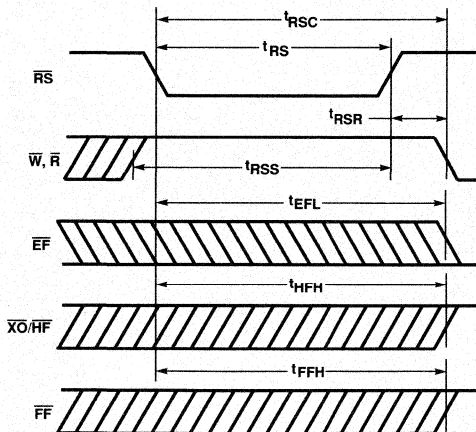


Figure 2. Reset Timing

### Writing Data To The FIFO

The HIGH state of the Full Flag ( $\overline{FF}$ ) indicates that the FIFO is capable of accepting data. The falling edge of Write ( $\overline{W}$ ) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8  $t_{DS}$  prior to and  $t_{DH}$  after the rising edge of  $\overline{W}$  will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ( $\overline{EF}$ ) occurs  $t_{WEF}$  after the rising edge of  $\overline{W}$  during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag (HF) will go LOW  $t_{WHF}$  after the falling edge of  $\overline{W}$  during the write operation which creates the half-full condition. (See Figure 5.)  $\overline{HF}$  will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 256 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ( $\overline{FF}$ ) goes LOW  $t_{WFF}$  after the falling edge of  $\overline{W}$  during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 512 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

### Reading Data From The FIFO

The HIGH state of the Empty Flag ( $\overline{EF}$ ) indicates that the FIFO is ready to output data. The falling edge of Read ( $\overline{R}$ ) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8  $t_A$  after the falling edge of  $\overline{R}$ , and remains until  $t_{DV}$  after the rising edge of  $\overline{R}$ . Q0-Q8 return to a high-impedance state when  $\overline{R}$  is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ( $\overline{FF}$ ) will go HIGH  $t_{RFF}$  after the rising edge of  $\overline{R}$  during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag (HF) will go HIGH  $t_{RHF}$  after the rising edge of  $\overline{R}$  during the read operation, which eliminates the half-full condition. (See Figure 5.)  $\overline{HF}$  will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 256 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of  $\overline{EF}$  occurs  $t_{REF}$  after the falling edge of  $\overline{R}$  during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

### Half-Full Flag

The Half-Full ( $\overline{HF}$ ) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 256 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 256 words, and Read and Write pulses are applied simultaneously, the  $\overline{HF}$  flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$  will always settle to the correct state after the appropriate delay,  $t_{WHF}$  or  $t_{RHF}$ . This property of the Half-Full Flag is clearly a function of the dynamic relation between  $\overline{W}$  and  $\overline{R}$ . Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

## RESET AND RETRANSMIT TRUTH TABLE Single-Device Configuration/Width-Expansion Mode

Mode	Input			Internal Status		Outputs		
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF	HF
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

- Notes: 1. Flags will change to show correct state according to write pointer.  
 2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

## RESET AND FIRST LOAD TRUTH TABLE Depth-Expansion/Compound-Expansion Mode

Mode	Input			Internal Status		Outputs	
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF
Reset—first device	0	0	$\overline{X0}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{X0}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{X0}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

- Notes: 1. XI is connected to  $\overline{X0}$  of previous device. See Figure 12.  
 2. Same as during Reset Cycle.  
 3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

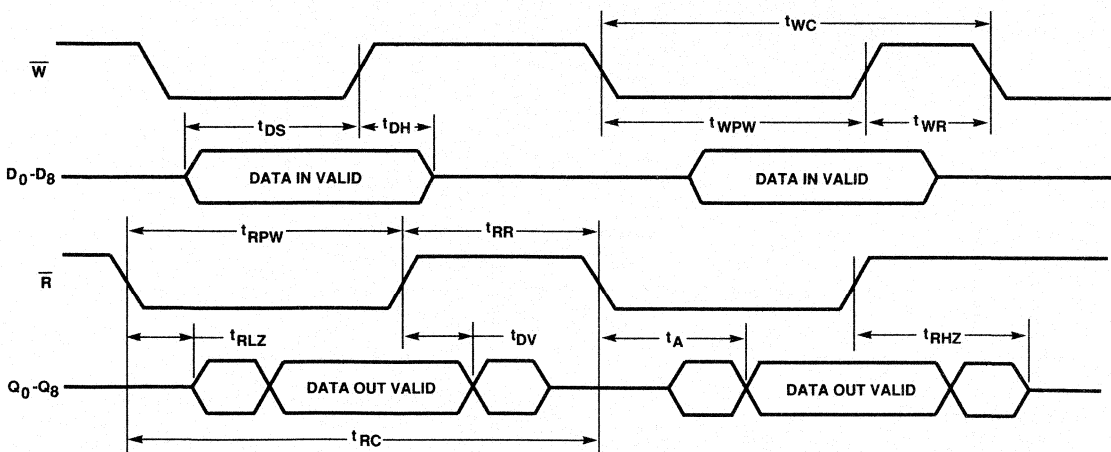


Figure 3. Asynchronous Write and Read Timing

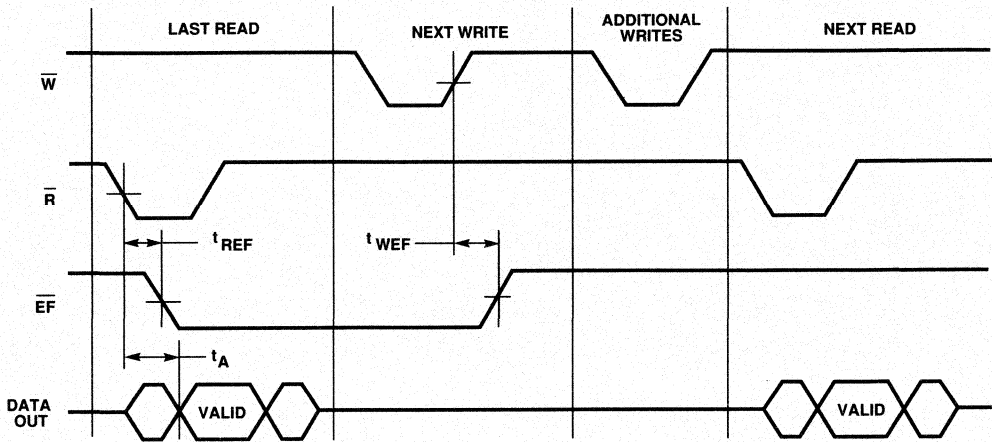
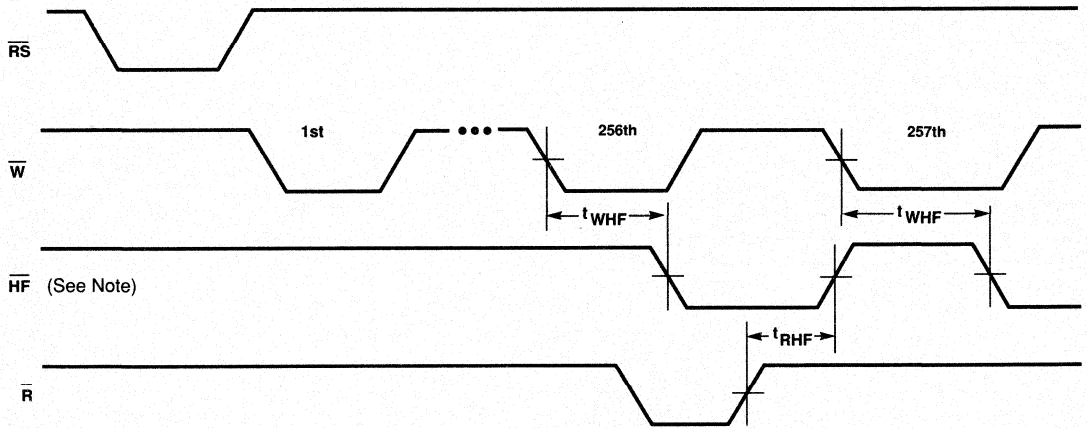


Figure 4. Empty Flag Timing



Note: Depending on the precise phase of  $\bar{W}$  and  $\bar{R}$ , the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when  $\bar{W}$  and  $\bar{R}$  are operating asynchronously near half full.

Figure 5. Half-Full Flag Timing

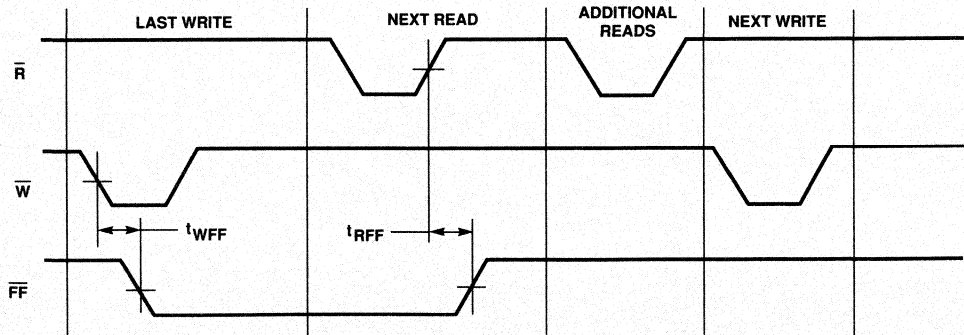


Figure 6. Full Flag Timing



## Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 512 or less writes between reset cycles.

The  $\overline{FL/RT}$  is used as the Retransmit ( $\overline{RT}$ ) input in Single-Device Mode. The retransmit capability is intended for use when there are 512 or less writes between reset cycles.  $\overline{RT}$ , an active LOW-going pulse of at least  $t_{RT}$  in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected.  $\overline{W}$  and  $\overline{R}$  must both be HIGH during the retransmit cycle. The first write or read cycle should not start until  $t_{RTR}$  after the rising edge of  $\overline{RT}$ . The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO  $t_{RTC}$  after the falling edge of  $\overline{RT}$ . (See Figure 7 and Table 1).

## Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ( $\overline{XI}$ ) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7201 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-

to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time ( $t_{WEF}$ ,  $t_{WHF}$ ,  $t_{WFF}$ ,  $t_{REF}$ ,  $t_{RHF}$ , and  $t_{RFF}$ ) for each flag has elapsed.

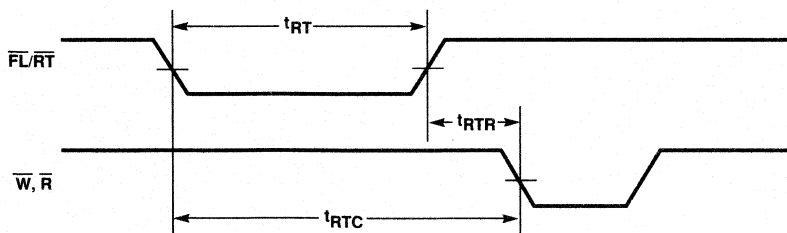
## Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ( $\overline{XO}$ ) of one device must be connected to Expansion In ( $\overline{XI}$ ) of the next device, with  $\overline{XO}$  of the last device being connected to  $\overline{XI}$  of the first device. The device that is to receive data first has its First Load ( $\overline{FL}$ ) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using  $\overline{XO}$  and  $\overline{XI}$ . A LOW-going pulse on  $\overline{XO}$  occurs when the last physical location of an active device, address 511, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the  $\overline{FF}$  outputs together. Likewise, a composite Empty Flag is created by OR-ing all the  $\overline{EF}$  outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

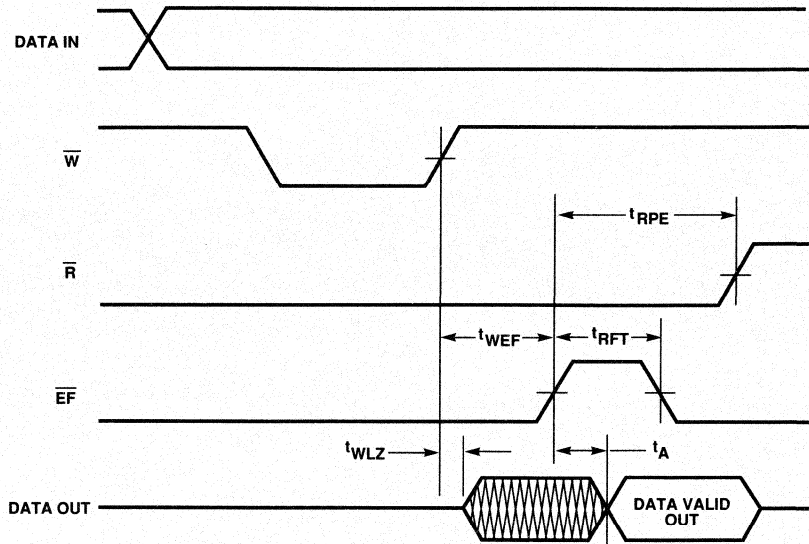
## Compound Expansion

FIFOs of greater width and depth than the Am7201 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)



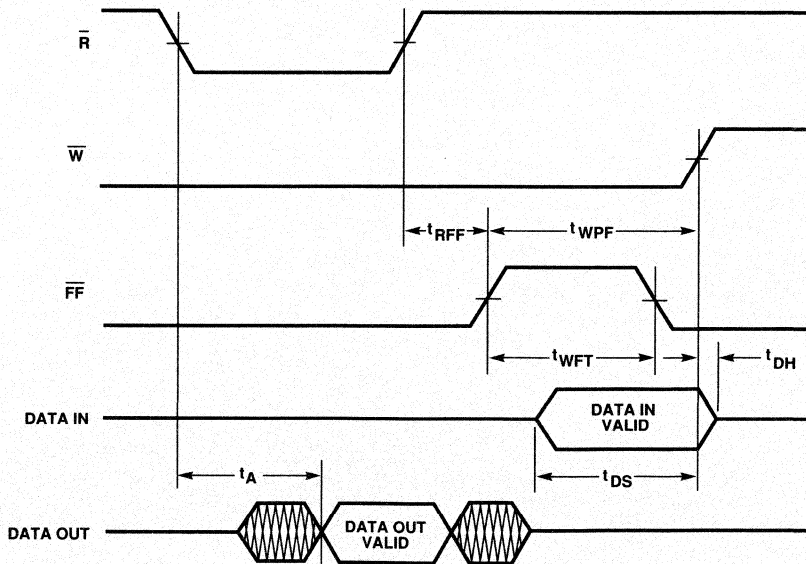
Note:  $\overline{EF}$ ,  $\overline{HF}$  and  $\overline{FF}$  may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at  $t_{RTC}$ .

Figure 7. Retransmit Timing



Note: ( $t_{RPE} = t_{RPW}$ ,  $t_{RFT} = t_{REF}$ )

Figure 8. Read Data Flow-Through Mode



Note: ( $t_{WPF} = t_{WPW}$ ,  $t_{WFT} = t_{WFF}$ )

Figure 9. Write Data Flow-Through Mode

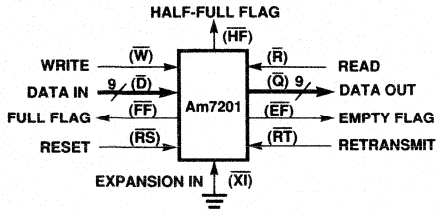


Figure 10. Single FIFO Configuration

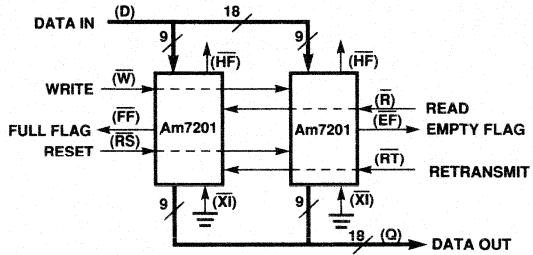


Figure 11. Width-Expansion to Form a 512x18 FIFO

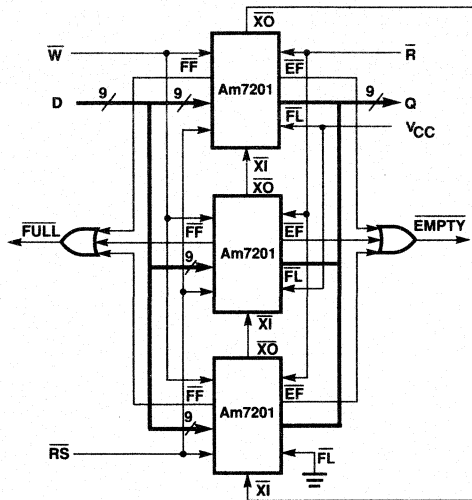


Figure 12. Depth-Expansion to Form a 1536x9 FIFO

2

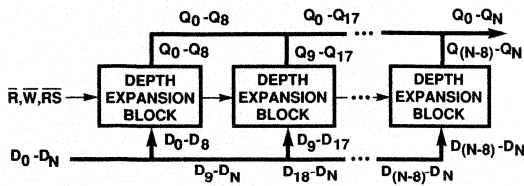


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

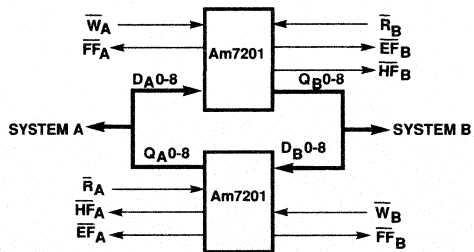
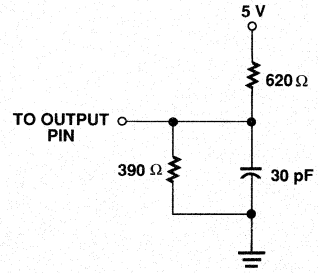


Figure 14. Bidirectional FIFO Mode

## AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



\* Includes jig and scope capacitances.

Figure 15. A.C. Test Load

## CAPACITANCE ( $T_A = +25^\circ\text{C}$ , $f = 1.0\text{ MHz}$ )

Symbol	Parameter (Note 1)	Conditions	Typ.	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$	5	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$	7	pF

Note: 1. For reference only.



# Am7202-25/35/50/65/80

## CMOS First-In First Out (FIFO) 1024x9-Bit Buffer

### DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 1024x9 organization
- Cycle times of 35/45/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption
  - 60 mA max, -35/50/65/80
  - 70 mA max, -25
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for XI - CMOS threshold
- Functional and pin compatible with industry standard devices

### GENERAL DESCRIPTION

The Am7202 is a RAM-based CMOS FIFO that is 1024 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7202 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7202 useful in communication, image processing, mass storage, DSP, and printing systems.

2

### BLOCK DIAGRAM

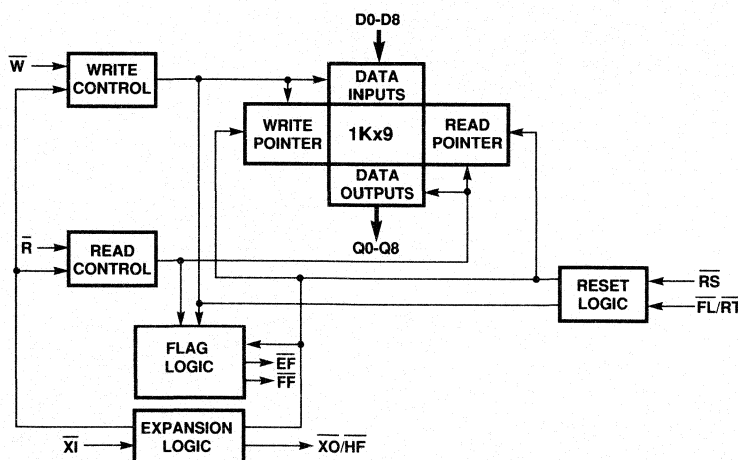
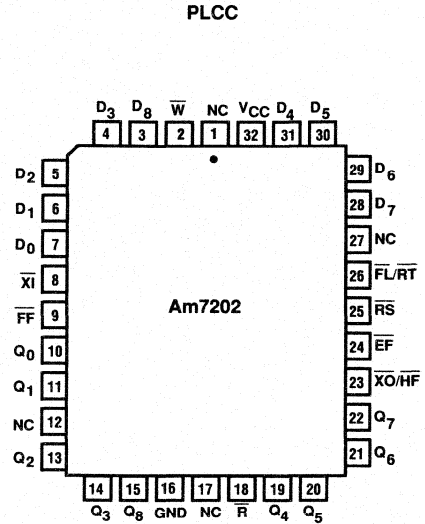
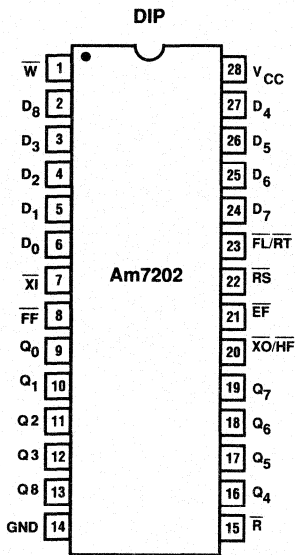


Figure 1.

## CONNECTION DIAGRAMS



- Pin Designations:**
- $\bar{W}$  = Write
  - $\bar{R}$  = Read
  - RS = Reset
  - FL/RT = First Load/Retransmit
  - $D_x$  = Data In
  - $Q_x$  = Data Out
  - $\bar{X}I$  = Expansion In
  - XO/HF = Expansion Out/Half-Full Flag
  - FF = Full Flag
  - EF = Empty Flag
  - $V_{CC}$  = Supply Voltage
  - GND = Ground
  - NC = No Connect

Note: Pin 1 is marked for orientation.

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

- a. Part Number
- b. Performance
- c. Package Type
- d. Operating Conditions

NOTE: AMD has changed the part numbers on the high-density FIFOs. The following part numbers are equivalent devices with the same DC and AC electrical characteristics.

New P/N	Old P/N
Am7200	67C4500
Am7201	67C4501
Am7202	67C4502
Am7203	67C4503
Am7204	—

Am7202 - 25 P C

- a. PART NUMBER
- b. PERFORMANCE  
ACCESS TIME
  - 25 = 25 ns
  - 35 = 35 ns
  - 50 = 50 ns
  - 65 = 65 ns
  - 80 = 80 ns
- c. PACKAGE TYPE
  - P = Plastic DIP (600 mil) - PD 028
  - D = Ceramic DIP (600 mil) - CD 028
  - J = Plastic Leaded Chip Carrier - PL 032
  - R = Plastic DIP (300 mil) - PD 3028
- d. OPERATING CONDITIONS
  - C = Commercial (0°C to 70°C)

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to + 7.0 V
Input voltage .....	-0.5 V to $V_{CC} + 0.5$ V
Operating temperature .....	0°C to + 70°C
Storage temperature .....	-55°C to + 150°C
Power dissipation .....	1.0 W
DC output current .....	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## DC CHARACTERISTICS Commercial: $V_{CC} = 5\text{ V} \pm 10\%$ , $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Parameter Symbol	Parameter Description	Am7202-25 $t_A = 25\text{ ns}$		Am7202-35 $t_A = 35\text{ ns}$		Am7202-50 $t_A = 50\text{ ns}$		Am7202-65 $t_A = 65\text{ ns}$		Am7202-80 $t_A = 80\text{ ns}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$I_{IL}$	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	-1	1	$\mu\text{A}$
$I_{IO}$	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$V_{IH}$	Input High Voltage (all inputs except $\overline{XI}$ ) (Note 3)	2.0	-	2.0	-	2.0	-	2.0	-	2.0	-	V
$V_{IL}$	Input Low Voltage (all inputs except $\overline{XI}$ ) (Note 3)	-	0.8	-	0.8	-	0.8	-	0.8	-	0.8	V
$V_{IH\overline{XI}}$	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	-	3.5	-	3.5	-	3.5	-	3.5	-	V
$V_{IL\overline{XI}}$	Input Low Voltage, $\overline{XI}$ (Note 3)	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	V
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2\text{ mA}$	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	V
$V_{OL}$	Output Logic "0" voltage $I_{OL} = 8\text{ mA}$	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V
$I_{CC1}$	Average $V_{CC}$ Power Supply Current (Note 4)	-	70	-	60	-	60	-	60	-	60	mA
$I_{CC2}$	Average Standby Current ( $\overline{R} = W = RS = FL/RT = V_{IH}$ ) (Note 4)	-	20	-	20	-	20	-	20	-	20	mA
$I_{CC3}$	Power Down Current (all inputs = $V_{CC} - 0.2\text{ V}$ ) (Note 4)	-	5	-	5	-	5	-	5	-	5	mA

- Notes:
1. Measurements with  $GND \leq V_{IN} \leq V_{CC}$ .
  2.  $\overline{R} \geq V_{IH}$ ,  $GND \leq V_{OUT} \leq V_{CC}$ .
  3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
  4.  $I_{CC}$  measurements are made with outputs open.

2

**AC CHARACTERISTICS**  $V_{CC} = 5 V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+ 70^\circ C$ 

Parameter Symbol	Parameter Description	Figures	Am7202-25		Am7202-35		Am7202-50		Am7202-65		Am7202-80		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write and Flag Timing</b>													
$t_{WC}$	Write Cycle Time	3	35	45	65	80	100						ns
$t_{WPW}$	Write Pulse Width	3	25	35	50	65	80						ns
$t_{WR}$	Write Recovery Time	3	10	10	15	15	20						ns
$t_{DS}$	Data Setup Time	3,9	15	18	30	30	40						ns
$t_{DH}$	Data Hold Time	3,9	0	0	5	10	10						ns
$t_{WFF}$	Write LOW to Full Flag LOW	6,9	25	30	45	60	60						ns
$t_{WHF}$	Write LOW to Half-Full Flag LOW	5	35	45	65	80	100						ns
$t_{WEF}$	Write HIGH to Empty Flag HIGH	4,8	25	30	45	60	60						ns
$t_{WLZ}$	Write pulse HIGH to data bus at LOW Z (Note 1)	8	5	10	15	15	20						ns
<b>Read and Flag Timing</b>													
$t_{RC}$	Read Cycle Time	3	35	45	65	80	100						ns
$t_A$	Access Time	3,4,8,9	25	35	50	65	80						ns
$t_{RH}$	Read Recovery Time	3	10	10	15	15	20						ns
$t_{RPW}$	Read Pulse Width	3	25	35	50	65	80						ns
$t_{RLZ}$	Read pulse LOW to data bus at LOW Z (Note 1)	3	5	5	10	10	10						ns
$t_{DV}$	Data Valid from read pulse HIGH	3	5	5	5	5	5						ns
$t_{RHZ}$	Read pulse HIGH to data bus at HIGH Z (Note 1)	3	18	20	30	30	30						ns
$t_{RFF}$	Read HIGH to Full Flag HIGH	6,9	25	30	45	60	60						ns
$t_{RHF}$	Read HIGH to Half Full-Flag HIGH	5	35	45	65	80	100						ns
$t_{REF}$	Read LOW to Empty Flag LOW	4,8	25	30	45	60	60						ns
<b>Reset Timing</b>													
$t_{RSC}$	Reset Cycle Time	2	35	45	65	80	100						ns
$t_{RS}$	Reset Pulse Width	2	25	35	50	65	80						ns
$t_{RSS}$	Reset Setup Time	2	25	35	50	65	80						ns
$t_{RSR}$	Reset Recovery Time	2	10	10	15	15	20						ns
$t_{EFL}$	Reset to Empty Flag LOW	2	35	45	65	80	100						ns
$t_{HFH}$	Reset to Half-Full Flag High	2	35	45	65	80	100						ns
$t_{FFH}$	Reset to Full Flag HIGH	2	35	45	65	80	100						ns
<b>Retransmit Timing</b>													
$t_{RTC}$	Retransmit Cycle Time	7	35	45	65	80	100						ns
$t_{RT}$	Retransmit Pulse Width	7	25	35	50	65	80						ns
$t_{RTR}$	Retransmit Recovery Time	7	10	10	15	15	20						ns

Note: 1. Characterized parameters.



## FUNCTIONAL DESCRIPTION

The Am7202 CMOS FIFO is designed around a 1024x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 1023. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7202. The write, read, data-in and data-out lines of the Am7202 are connected in parallel, and the Expansion-Out (XO) and the Expansion-In (XI) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between XO and XI.

## OPERATIONAL DESCRIPTION

### Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of XI and FL are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ( $\bar{R}$ ) and Write ( $\bar{W}$ ) signals must be HIGH  $t_{RSS}$  prior to and  $t_{RSR}$  after the rising edge of Reset ( $\bar{RS}$ ). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ( $\bar{EF}$ ) being LOW, active, and both the Half-Full (HF) and Full Flag (FF) being HIGH, inactive.

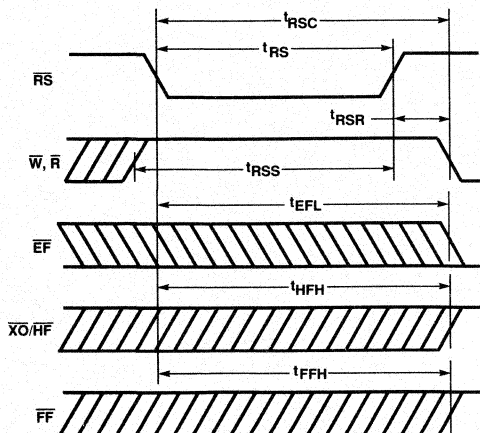


Figure 2. Reset Timing

### Writing Data To The FIFO

The HIGH state of the Full Flag ( $\bar{FF}$ ) indicates that the FIFO is capable of accepting data. The falling edge of Write ( $\bar{W}$ ) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8  $t_{DS}$  prior to and  $t_{DH}$  after the rising edge of  $\bar{W}$  will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ( $\bar{EF}$ ) occurs  $t_{WEF}$  after the rising edge of  $\bar{W}$  during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag /HF) will go LOW  $t_{WHF}$  after the falling edge of  $\bar{W}$  during the write operation which creates the half-full condition. (See Figure 5.)  $\bar{HF}$  will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 512 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag (FF) goes LOW  $t_{WFF}$  after the falling edge of  $\bar{W}$  during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 1024 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

### Reading Data From The FIFO

The HIGH state of the Empty Flag ( $\bar{EF}$ ) indicates that the FIFO is ready to output data. The falling edge of Read ( $\bar{R}$ ) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8  $t_A$  after the falling edge of  $\bar{R}$ , and remains until  $t_{DV}$  after the rising edge of  $\bar{R}$ . Q0-Q8 return to a high-impedance state when a valid read is not in progress.

The Full Flag ( $\bar{FF}$ ) will go HIGH  $t_{REF}$  after the rising edge of  $\bar{R}$  during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag (HF) will go HIGH  $t_{RHF}$  after the rising edge of  $\bar{R}$  during the read operation, which eliminates the half-full condition. (See Figure 5.)  $\bar{HF}$  will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 511 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of EF occurs  $t_{REF}$  after the falling edge of  $\bar{R}$  during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

### Half-Full Flag

The Half-Full ( $\bar{HF}$ ) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 512 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 512 words, and Read and Write pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\bar{HF}$  will always settle to the correct state after the appropriate delay,  $t_{WHF}$  or  $t_{RHF}$ . This property of the Half-Full Flag is clearly a function of the dynamic relation between  $\bar{W}$  and  $\bar{R}$ . Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

2

## RESET AND RETRANSMIT TRUTH TABLE Single-Device Configuration/Width-Expansion Mode

Mode	Input			Internal Status		Outputs		
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF	HF
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes: 1. Flags will change to show correct state according to write pointer.  
 2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

## RESET AND FIRST LOAD TRUTH TABLE Depth-Expansion/Compound-Expansion Mode

Mode	Input			Internal Status		Outputs	
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF
Reset-first device	0	0	X0 (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	X0 (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	X0 (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes: 1. XI is connected to X0 of previous device. See Figure 12.  
 2. Same as during Reset Cycle.  
 3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

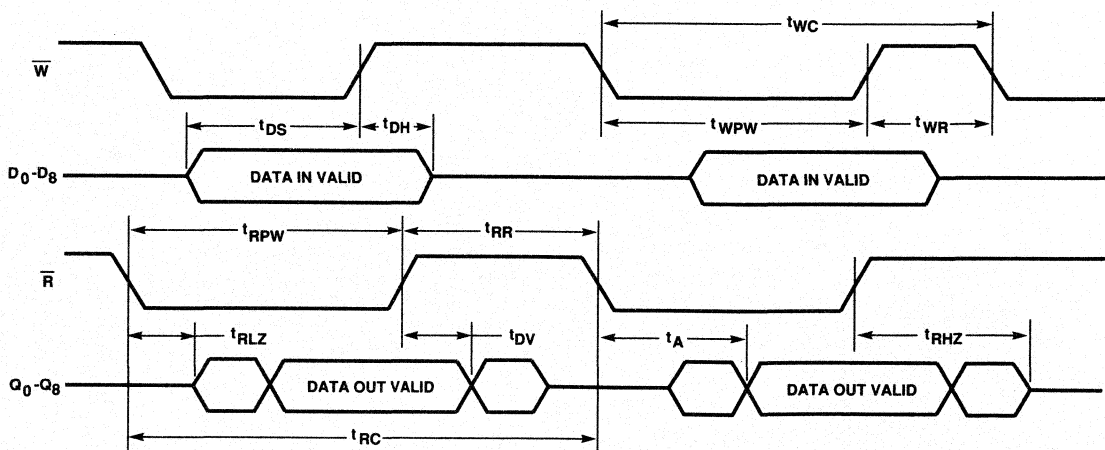


Figure 3. Asynchronous Write and Read Timing

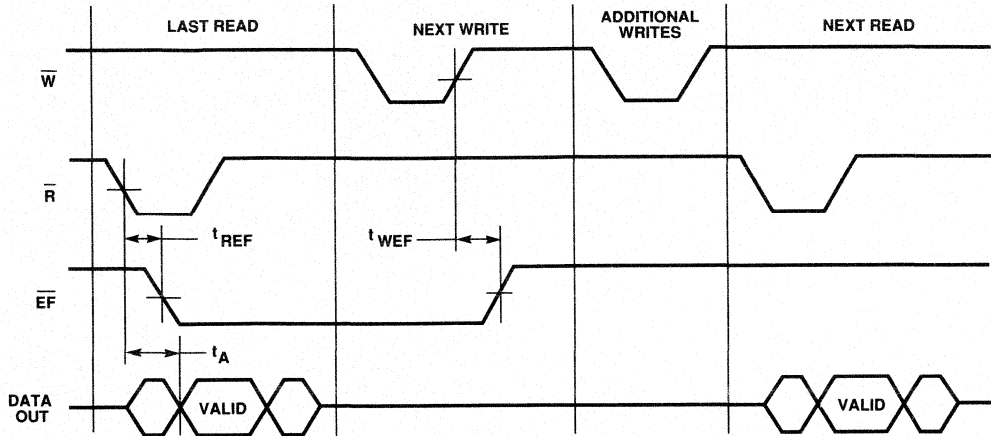
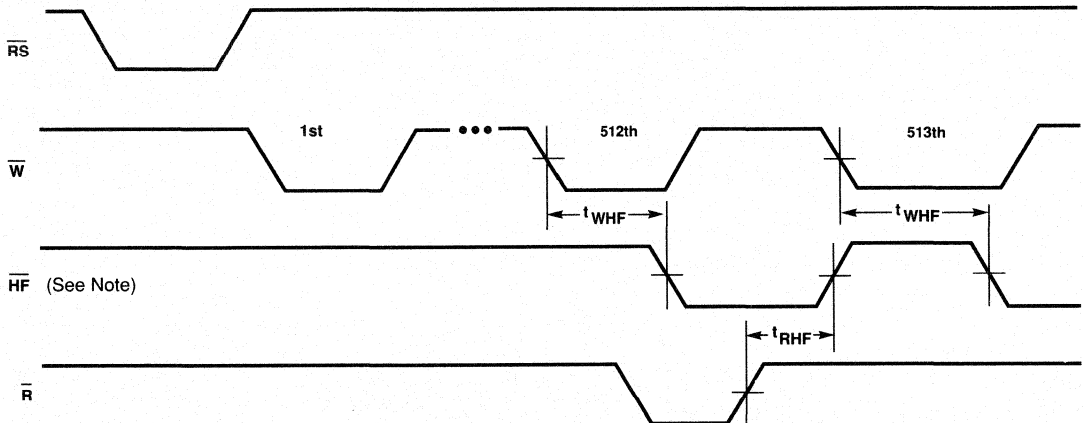


Figure 4. Empty Flag Timing



Note: Depending on the precise phase of  $\overline{W}$  and  $\overline{R}$ , the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when  $\overline{W}$  and  $\overline{R}$  are operating asynchronously near half full.

Figure 5. Half-Full Flag Timing

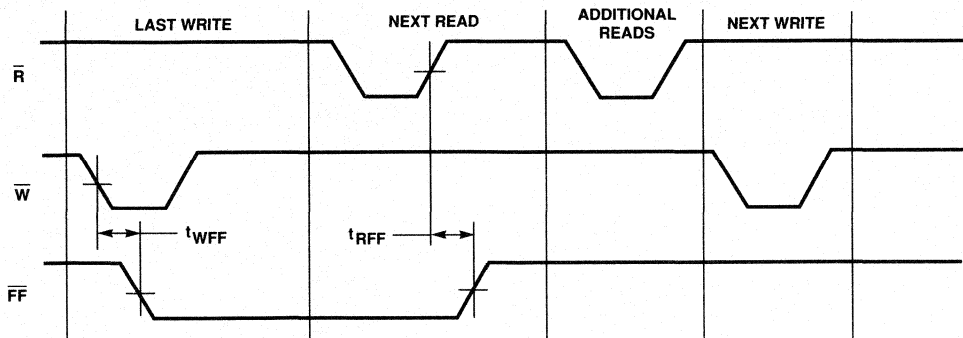


Figure 6. Full Flag Timing

## Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 1024 or less writes between reset cycles.

The  $\overline{FL/RT}$  is used as the Retransmit ( $\overline{RT}$ ) input in Single-Device Mode.  $\overline{RT}$ , an active LOW-going pulse of at least  $t_{RT}$  in duration, returns the internal read pointer to address zero and leaves the write pointer unaffected.  $\overline{W}$  and  $\overline{R}$  must both be HIGH during the retransmit cycle. The first write or read cycle should not start until  $t_{RTR}$  after the rising edge of  $\overline{RT}$ . The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO  $t_{RTC}$  after the falling edge of  $\overline{RT}$ . (See Figure 7 and Table 1).

## Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ( $\overline{XI}$ ) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7202 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag.

These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time ( $t_{WEP}$ ,  $t_{WHF}$ ,  $t_{WFF}$ ,  $t_{REF}$ ,  $t_{RHF}$ , and  $t_{WFE}$ ) for each flag has elapsed.

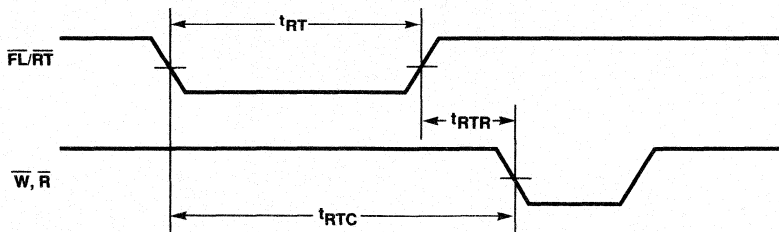
## Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ( $\overline{XO}$ ) of one device must be connected to Expansion In ( $\overline{XI}$ ) of the next device, with  $\overline{XO}$  of the last device being connected to  $\overline{XI}$  of the first device. The device that is to receive data first has its First Load ( $\overline{FL}$ ) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using  $\overline{XO}$  and  $\overline{XI}$ . A LOW-going pulse on  $\overline{XO}$  occurs when the last physical location of an active device, address 1023, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the FF outputs together. Likewise, a composite Empty Flag is created by OR-ing all the EF outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

## Compound Expansion

FIFOs of greater width and depth than the Am7202 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)



Note:  $\overline{EF}$ ,  $\overline{HF}$  and  $\overline{FF}$  may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at  $t_{RTC}$ .

Figure 7. Retransmit Timing

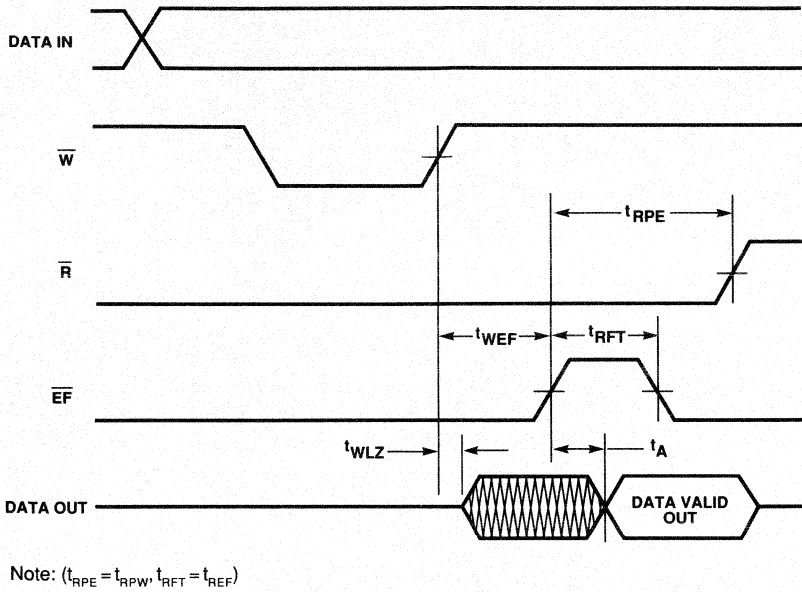


Figure 8. Read Data Flow-Through Mode

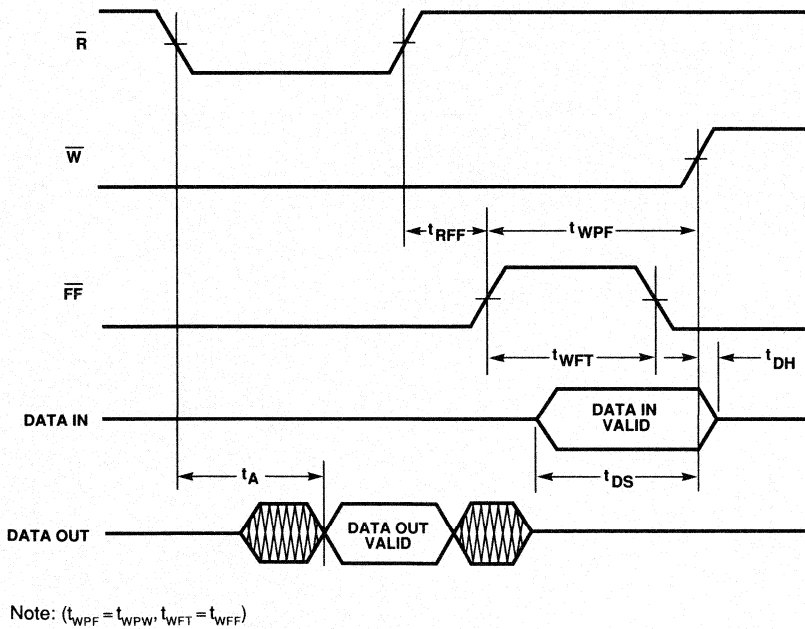


Figure 9. Write Data Flow-Through Mode

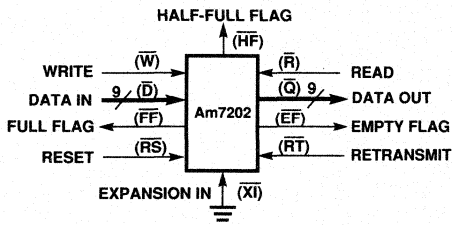


Figure 10. Single FIFO Configuration

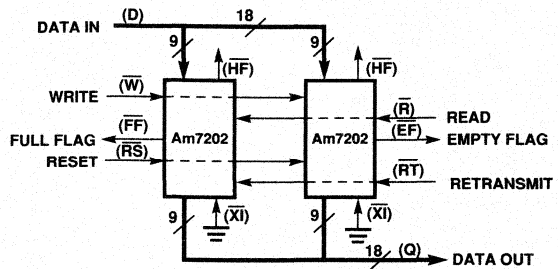


Figure 11. Width-Expansion to Form a 512x18 FIFO

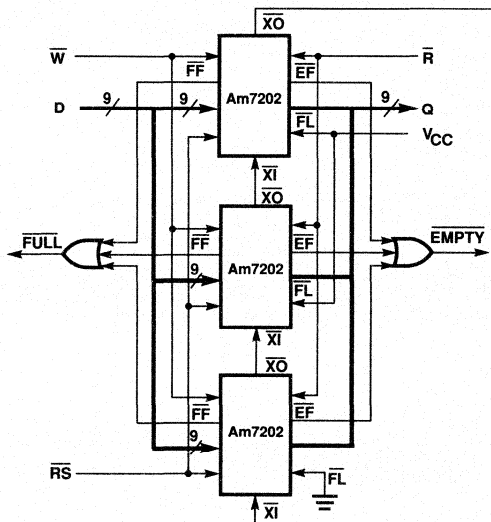


Figure 12. Depth-Expansion to Form a 1536x9 FIFO

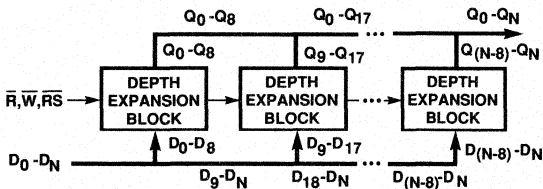


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

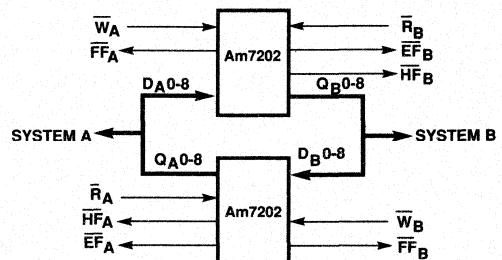
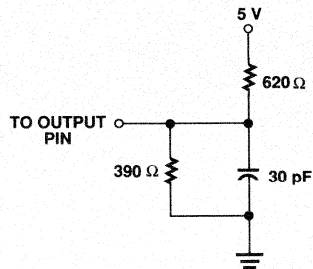


Figure 14. Bidirectional FIFO Mode

## AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



\* Includes jig and scope capacitances.

Figure 15. A.C. Test Load

## CAPACITANCE ( $T_A = +25^\circ\text{C}$ , $f = 1.0\text{ MHz}$ )

Symbol	Parameter (Note 1)	Conditions	Typ.	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$	5	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$	7	pF

Note: 1. For reference only.



# Am7203-25/35/50/65/80

CMOS First-in First-out (FIFO) 2048x9-Bit Buffer

## DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 2048x9 organization
- Cycle times of 35/45/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption
  - 60 mA max, -35/50/65/80
  - 70 mA max, -25
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for  $\overline{XI}$  - CMOS threshold
- Functional and pin compatible with industry standard devices

## GENERAL DESCRIPTION

The Am7203 is a RAM-based CMOS FIFO that is 2048 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7203 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7203 useful in communication, image processing, mass storage, DSP, and printing systems.

## BLOCK DIAGRAM

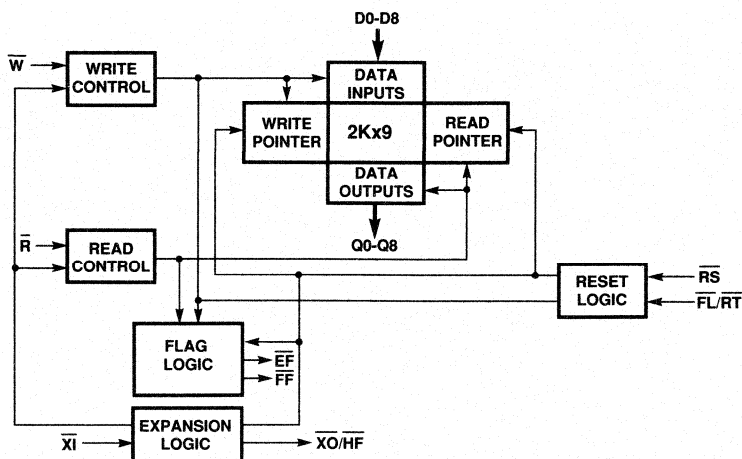
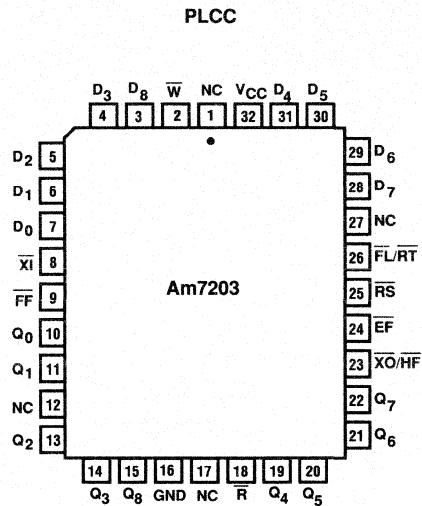
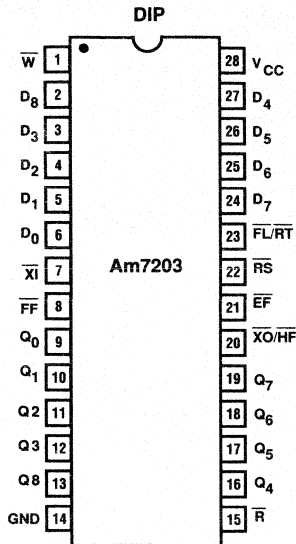


Figure 1.



## CONNECTION DIAGRAMS



- Pin Designations:**
- $\bar{W}$  = Write
  - $\bar{R}$  = Read
  - $\bar{RS}$  = Reset
  - $\bar{FL}/\bar{RT}$  = First Load/Retransmit
  - $D_x$  = Data In
  - $Q_x$  = Data Out
  - $\bar{XI}$  = Expansion In
  - $\bar{XO}/\bar{HF}$  = Expansion Out/Half-Full Flag
  - $\bar{FF}$  = Full Flag
  - $\bar{EF}$  = Empty Flag
  - $V_{CC}$  = Supply Voltage
  - $GND$  = Ground
  - $NC$  = No Connect

Note: Pin 1 is marked for orientation.

2

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

- a. Part Number
- b. Performance
- c. Package Type
- d. Operating Conditions

NOTE: AMD has changed the part numbers on the high-density FIFOs. The following part numbers are equivalent devices with the same DC and AC electrical characteristics.

New P/N	Old P/N
Am7200	67C4500
Am7201	67C4501
Am7202	67C4502
Am7203	67C4503
Am7204	—

- Am7203- 25 P C**
- a. PART NUMBER
  - b. PERFORMANCE  
ACCESS TIME  
25 = 25 ns\*  
35 = 35 ns  
50 = 50 ns  
65 = 65 ns  
80 = 80 ns
  - c. PACKAGE TYPE  
P = Plastic DIP (600 mil) - PD 028  
D = Ceramic DIP (600 mil)\* - CD 028  
J = Plastic Leaded Chip Carrier\* - PL 032  
R = Plastic DIP (300 mil) - PD 3028
  - d. OPERATING CONDITIONS  
C = Commercial (0°C to 70°C)

Note: \* Consult factory.

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$	-0.5 V to + 7.0 V
Input voltage	-0.5 V to $V_{CC} + 0.5$ V
Operating temperature	0°C to + 70°C
Storage temperature	-55°C to + 150°C
Power dissipation	1.0 W
DC output current	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## DC CHARACTERISTICS Commercial: $V_{CC} = 5\text{ V} \pm 10\%$ , $T_A = 0^\circ\text{C to } +70^\circ\text{C}$

Parameter Symbol	Parameter Description	Am7203-25 $t_A = 25\text{ ns}$		Am7203-35 $t_A = 35\text{ ns}$		Am7203-50 $t_A = 50\text{ ns}$		Am7203-65 $t_A = 65\text{ ns}$		Am7203-80 $t_A = 80\text{ ns}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$I_{IL}$	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	-1	1	$\mu\text{A}$
$I_{IO}$	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$V_{IH}$	Input High Voltage (all inputs except $\overline{XI}$ ) (Note 3)	2.0	-	2.0	-	2.0	-	2.0	-	2.0	-	V
$V_{IL}$	Input Low Voltage (all inputs except $\overline{XI}$ ) (Note 3)	-	0.8	-	0.8	-	0.8	-	0.8	-	0.8	V
$V_{IHXI}$	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	-	3.5	-	3.5	-	3.5	-	3.5	-	V
$V_{ILXI}$	Input Low Voltage, $\overline{XI}$ (Note 3)	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	V
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2\text{ mA}$	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	V
$V_{OL}$	Output Logic "0" voltage $I_{OL} = 8\text{ mA}$	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V
$I_{CC1}$	Average $V_{CC}$ Power Supply Current (Note 4)	-	70	-	60	-	60	-	60	-	60	mA
$I_{CC2}$	Average Standby Current ( $\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$ ) (Note 4)	-	20	-	20	-	20	-	20	-	20	mA
$I_{CC3}$	Power Down Current (all inputs = $V_{CC} - 0.2\text{ V}$ ) (Note 4)	-	5	-	5	-	5	-	5	-	5	mA

- Notes:
1. Measurements with  $GND \leq V_{IN} \leq V_{CC}$ .
  2.  $\overline{R} \geq V_{IH}$ ,  $GND \leq V_{OUT} \leq V_{CC}$ .
  3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
  4.  $I_{CC}$  measurements are made with outputs open.

**AC CHARACTERISTICS**  $V_{CC} = 5 V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+ 70^\circ C$ 

Parameter Symbol	Parameter Description	Figures	Am7203-25 Min. Max.	Am7203-35 Min. Max.	Am7203-50 Min. Max.	Am7203-65 Min. Max.	Am7203-80 Min. Max.	Unit
<b>Write and Flag Timing</b>								
$t_{WC}$	Write Cycle Time	3	35	45	65	80	100	ns
$t_{WPW}$	Write Pulse Width	3	25	35	50	65	80	ns
$t_{WR}$	Write Recovery Time	3	10	10	15	15	20	ns
$t_{DS}$	Data Setup Time	3,9	15	18	30	30	40	ns
$t_{DH}$	Data Hold Time	3,9	0	0	5	10	10	ns
$t_{WFF}$	Write LOW to Full Flag LOW	6,9	25	30	45	60	60	ns
$t_{WHF}$	Write LOW to Half-Full Flag LOW	5	35	45	65	80	100	ns
$t_{WEF}$	Write HIGH to Empty Flag HIGH	4,8	25	30	45	60	60	ns
$t_{WLZ}$	Write pulse HIGH to data bus at LOW Z (Note 1)	8	5	10	15	15	20	ns
<b>Read and Flag Timing</b>								
$t_{RC}$	Read Cycle Time	3	35	45	65	80	100	ns
$t_A$	Access Time	3,4,8,9	25	35	50	65	80	ns
$t_{RR}$	Read Recovery Time	3	10	10	15	15	20	ns
$t_{RPW}$	Read Pulse Width	3	25	35	50	65	80	ns
$t_{RLZ}$	Read pulse LOW to data bus at LOW Z (Note 1)	3	5	5	10	10	10	ns
$t_{DV}$	Data Valid from read pulse HIGH	3	5	5	5	5	5	ns
$t_{RHZ}$	Read pulse HIGH to data bus at HIGH Z (Note 1)	3	18	20	30	30	30	ns
$t_{RFF}$	Read HIGH to Full Flag HIGH	6,9	25	30	45	60	60	ns
$t_{RHF}$	Read HIGH to Half Full-Flag HIGH	5	35	45	65	80	100	ns
$t_{REF}$	Read LOW to Empty Flag LOW	4,8	25	30	45	60	60	ns
<b>Reset Timing</b>								
$t_{RSC}$	Reset Cycle Time	2	35	45	65	80	100	ns
$t_{RS}$	Reset Pulse Width	2	25	35	50	65	80	ns
$t_{RSS}$	Reset Setup Time	2	25	35	50	65	80	ns
$t_{RSR}$	Reset Recovery Time	2	10	10	15	15	20	ns
$t_{EFL}$	Reset to Empty Flag LOW	2	35	45	65	80	100	ns
$t_{HFH}$	Reset to Half-Full Flag High	2	35	45	65	80	100	ns
$t_{FFH}$	Reset to Full Flag HIGH	2	35	45	65	80	100	ns
<b>Retransmit Timing</b>								
$t_{RTC}$	Retransmit Cycle Time	7	35	45	65	80	100	ns
$t_{RT}$	Retransmit Pulse Width	7	25	35	50	65	80	ns
$t_{RTR}$	Retransmit Recovery Time	7	10	10	15	15	20	ns

Note: 1. Characterized parameters.

**2**

## FUNCTIONAL DESCRIPTION

The Am7203 CMOS FIFO is designed around a 2048x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 2047. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7203. The write, read, data-in and data-out lines of the Am7203 are connected in parallel, and the Expansion-Out (XO) and the Expansion-In (XI) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between  $\overline{XO}$  and XI.

## OPERATIONAL DESCRIPTION

### Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of XI and FL are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ( $\overline{R}$ ) and Write ( $\overline{W}$ ) signals must be HIGH  $t_{R_{SS}}$  prior to and  $t_{R_{SR}}$  after the rising edge of Reset (RS). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ( $\overline{EF}$ ) being LOW, active, and both the Half-Full (HF) and Full Flag (FF) being HIGH, inactive.

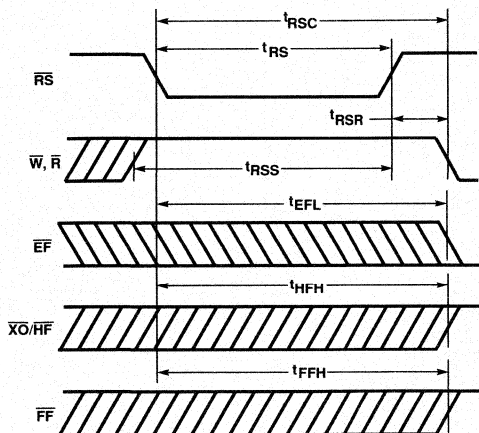


Figure 2. Reset Timing

### Writing Data To The FIFO

The HIGH state of the Full Flag ( $\overline{FF}$ ) indicates that the FIFO is capable of accepting data. The falling edge of Write ( $\overline{W}$ ) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8  $t_{D_{SS}}$  prior to and  $t_{D_{DH}}$  after the rising edge of  $\overline{W}$  will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ( $\overline{EF}$ ) occurs  $t_{WEF}$  after the rising edge of  $\overline{W}$  during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ( $\overline{HF}$ ) will go LOW  $t_{WHF}$  after the falling edge of  $\overline{W}$  during the write operation which creates the half-full condition. (See Figure 5.)  $\overline{HF}$  will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 1024 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ( $\overline{FF}$ ) goes LOW  $t_{WFF}$  after the falling edge of  $\overline{W}$  during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 2048 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

### Reading Data From The FIFO

The HIGH state of the Empty Flag ( $\overline{EF}$ ) indicates that the FIFO is ready to output data. The falling edge of Read ( $\overline{R}$ ) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8  $t_{A}$  after the falling edge of  $\overline{R}$ , and remains until  $t_{D_{V}}$  after the rising edge of  $\overline{R}$ . Q0-Q8 return to a high-impedance state when a valid read is not in progress.

The Full Flag ( $\overline{FF}$ ) will go HIGH  $t_{RFF}$  after the rising edge of  $\overline{R}$  during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ( $\overline{HF}$ ) will go HIGH  $t_{RHF}$  after the rising edge of  $\overline{R}$  during the read operation, which eliminates the half-full condition. (See Figure 5.)  $\overline{HF}$  will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 1023 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of  $\overline{EF}$  occurs  $t_{REF}$  after the falling edge of  $\overline{R}$  during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

### Half-Full Flag

The Half-Full ( $\overline{HF}$ ) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 1024 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 1024 words, and Read and Write pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$  will always settle to the correct state after the appropriate delay,  $t_{WHF}$  or  $t_{RHF}$ . This property of the Half-Full Flag is clearly a function of the dynamic relation between  $\overline{W}$  and  $\overline{R}$ . Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

## RESET AND RETRANSMIT TRUTH TABLE Single-Device Configuration/Width-Expansion Mode

Mode	Input			Internal Status		Outputs		
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF	HF
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes: 1. Flags will change to show correct state according to write pointer.  
 2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

## RESET AND FIRST LOAD TRUTH TABLE Depth-Expansion/Compound-Expansion Mode

Mode	Input			Internal Status		Outputs	
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF
Reset—first device	0	0	$\overline{X0}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{X0}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{X0}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes: 1.  $\overline{XI}$  is connected to  $\overline{X0}$  of previous device. See Figure 12.  
 2. Same as during Reset Cycle.  
 3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

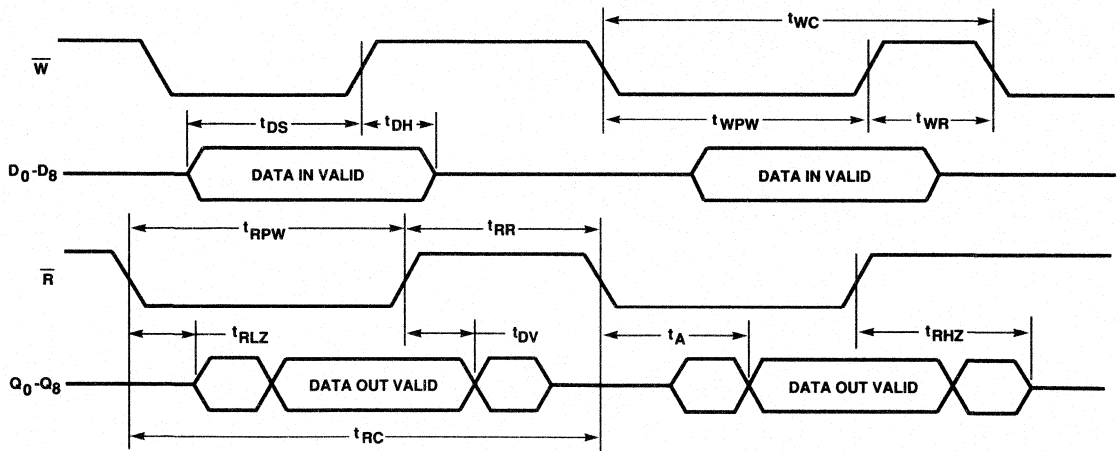


Figure 3. Asynchronous Write and Read Timing

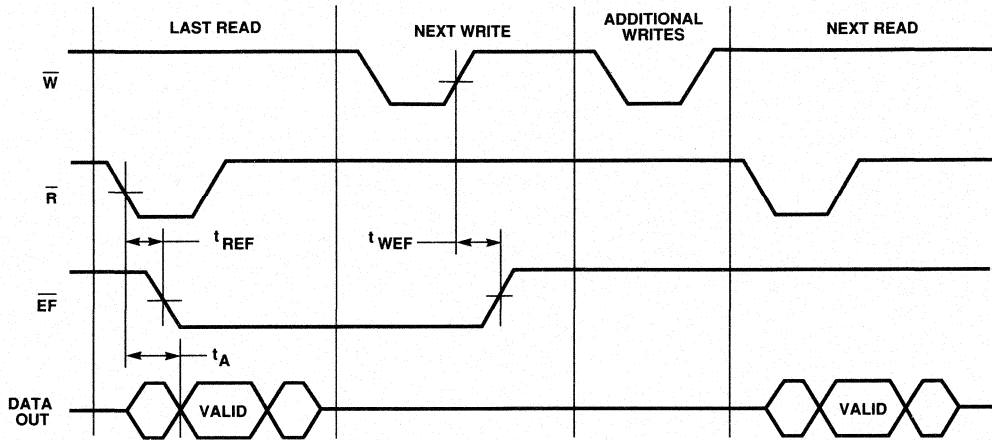
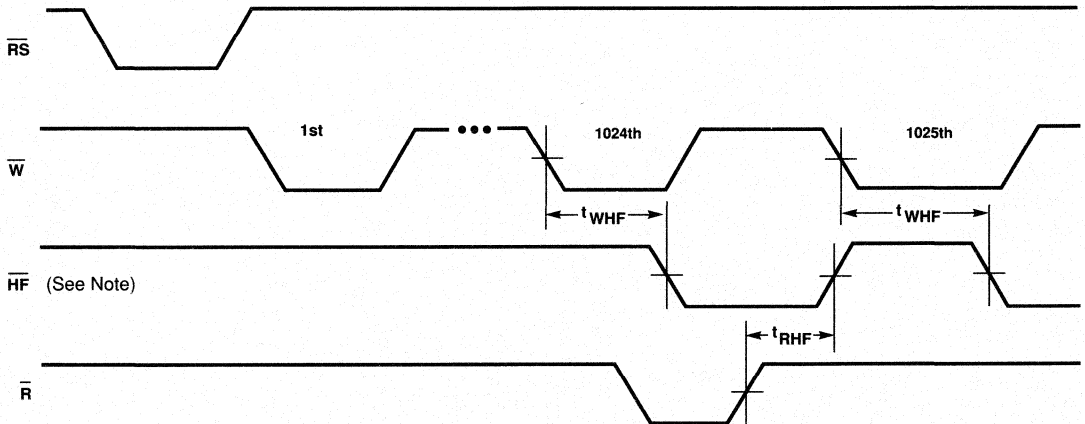


Figure 4. Empty Flag Timing



Note: Depending on the precise phase of  $\overline{W}$  and  $\overline{R}$ , the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when  $\overline{W}$  and  $\overline{R}$  are operating asynchronously near half full.

Figure 5. Half-Full Flag Timing

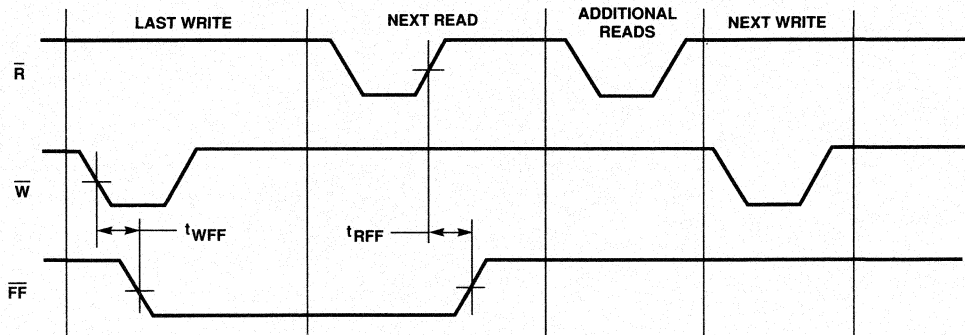


Figure 6. Full Flag Timing

## Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 2048 or less writes between reset cycles.

The  $\overline{FL/RT}$  is used as the Retransmit (RT) input in Single-Device Mode. RT, an active LOW-going pulse of at least  $t_{RT}$  in duration, returns the internal read pointer to address zero and leaves the write pointer unaffected.  $\overline{W}$  and  $\overline{R}$  must both be HIGH during the retransmit cycle. The first write or read cycle should not start until  $t_{RTR}$  after the rising edge of RT. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO  $t_{RTC}$  after the falling edge of RT. (See Figure 7 and Table 1).

### Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ( $\overline{XI}$ ) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7203 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used

as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time ( $t_{WEF}$ ,  $t_{WHF}$ ,  $t_{WFF}$ ,  $t_{REF}$ ,  $t_{RHF}$ , and  $t_{RFF}$ ) for each flag has elapsed.

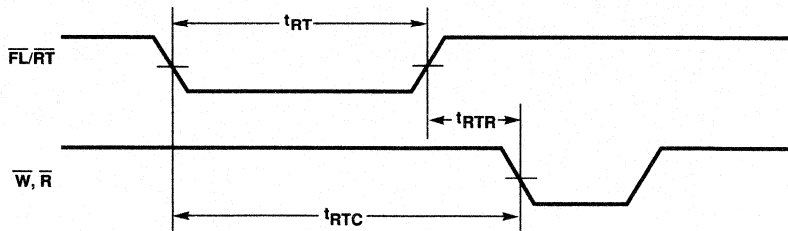
### Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ( $\overline{XO}$ ) of one device must be connected to Expansion In ( $\overline{XI}$ ) of the next device, with  $\overline{XO}$  of the last device being connected to  $\overline{XI}$  of the first device. The device that is to receive data first has its First Load ( $\overline{FL}$ ) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using  $\overline{XO}$  and  $\overline{XI}$ . A LOW-going pulse on  $\overline{XO}$  occurs when the last physical location of an active device, address 2047, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the  $\overline{FF}$  outputs together. Likewise, a composite Empty Flag is created by OR-ing all the EF outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

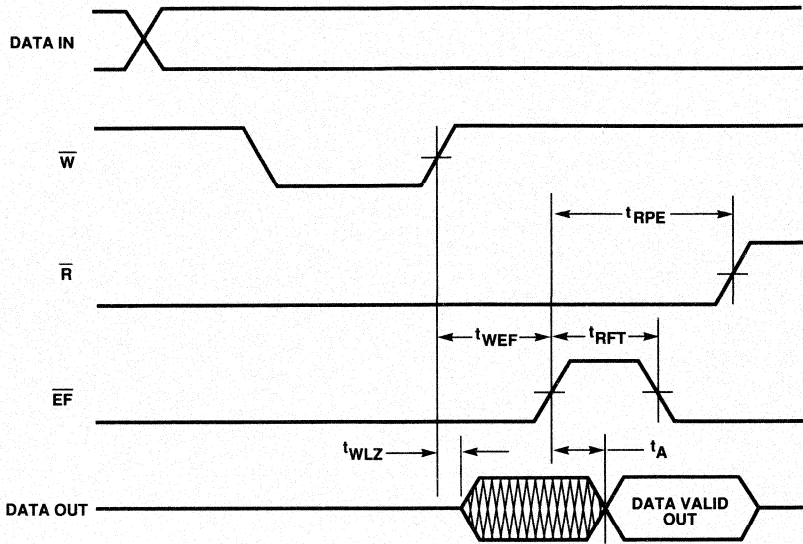
### Compound Expansion

FIFOs of greater width and depth than the Am7203 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)



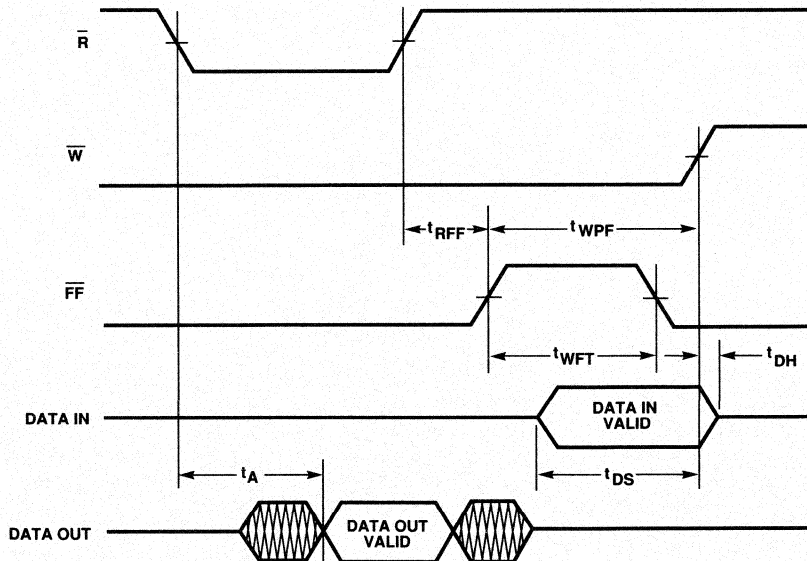
Note:  $\overline{EF}$ ,  $\overline{HF}$  and  $\overline{FF}$  may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at  $t_{RTC}$ .

Figure 7. Retransmit Timing



Note: ( $t_{RPE} = t_{RPW}$ ;  $t_{RFT} = t_{REF}$ )

Figure 8. Read Data Flow-Through Mode



Note: ( $t_{WPF} = t_{WPW}$ ;  $t_{WFT} = t_{WFE}$ )

Figure 9. Write Data Flow-Through Mode



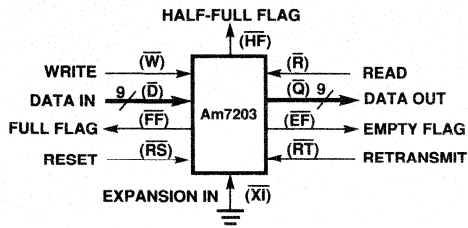


Figure 10. Single FIFO Configuration

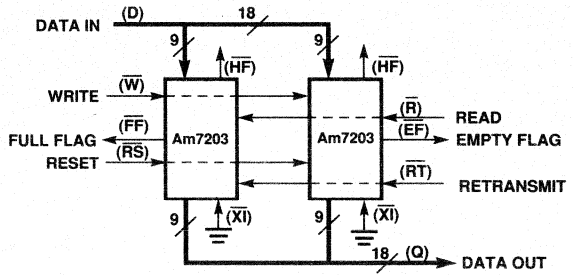


Figure 11. Width-Expansion to Form a 512x18 FIFO

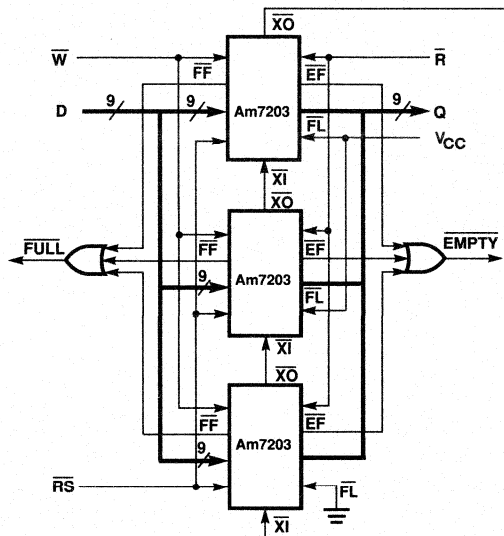


Figure 12. Depth-Expansion to Form a 12288x9 FIFO

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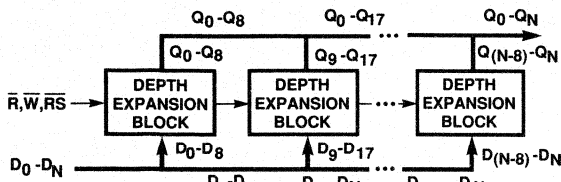


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

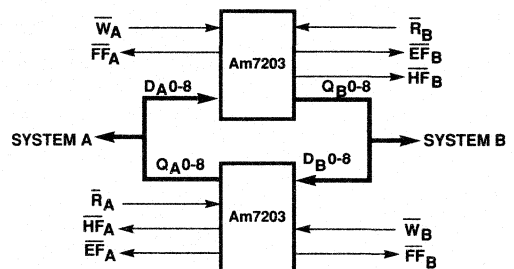


Figure 14. Bidirectional FIFO Mode

# Am7204-25/35/50/65/80

CMOS First-in First-out (FIFO) 4096x9-Bit Buffer



## DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 4096x9 organization
- Cycle times of 35/45/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption
  - 60 mA max, -35/50/65/80
  - 70 mA max, -25
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for  $\overline{X1}$  - CMOS threshold
- Functional and pin compatible with industry standard devices

## GENERAL DESCRIPTION

The Am7204 is a RAM-based CMOS FIFO that is 4096 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7204 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7204 useful in communication, image processing, mass storage, DSP, and printing systems.

## BLOCK DIAGRAM

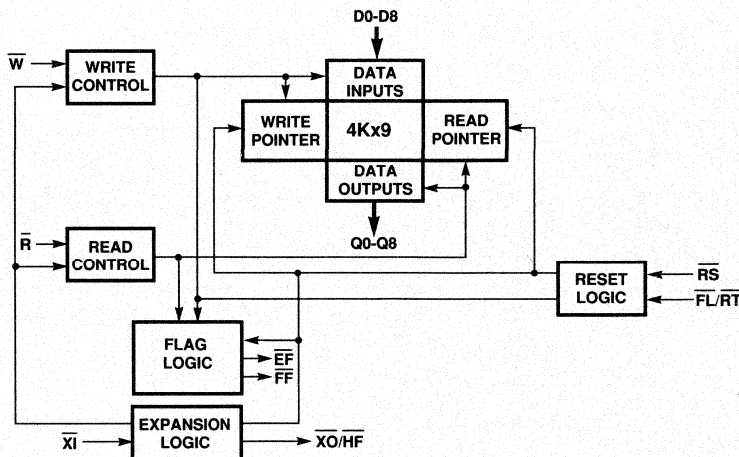
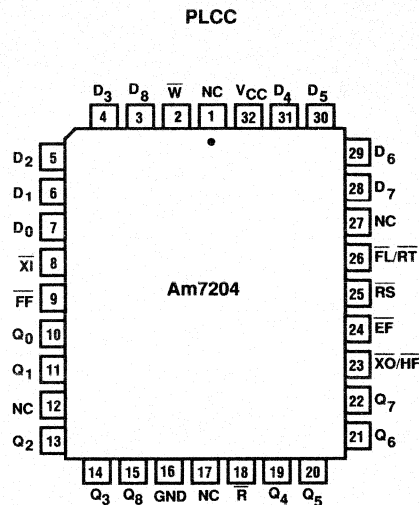
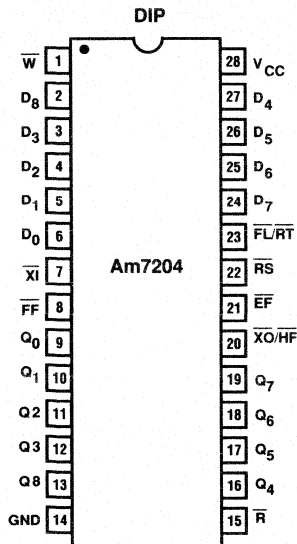


Figure 1.

## CONNECTION DIAGRAMS



- Pin Designations:**
- $\bar{W}$  = Write
  - R = Read
  - $\bar{RS}$  = Reset
  - $\overline{FL/RT}$  = First Load/Retransmit
  - $D_x$  = Data In
  - $Q_x$  = Data Out
  - XI = Expansion In
  - $\overline{XO/HF}$  = Expansion Out/Half-Full Flag
  - FF = Full Flag
  - EF = Empty Flag
  - $V_{CC}$  = Supply Voltage
  - GND = Ground
  - NC = No Connect

Note: Pin 1 is marked for orientation.

2

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

- a. Part Number
- b. Performance
- c. Package Type
- d. Operating Conditions

NOTE: AMD has changed the part numbers on the high-density FIFOs. The following part numbers are equivalent devices with the same DC and AC electrical characteristics.

New P/N	Old P/N
Am7200	67C4500
Am7201	67C4501
Am7202	67C4502
Am7203	67C4503
Am7204	—

### Am7204 - 25 P C

- a. PART NUMBER
- b. PERFORMANCE  
ACCESS TIME
  - 25 = 25 ns
  - 35 = 35 ns
  - 50 = 50 ns
  - 65 = 65 ns
  - 80 = 80 ns
- c. PACKAGE TYPE
  - P = Plastic DIP (600 mil) - PD 028
  - D = Ceramic DIP (600 mil) - CD 028
  - J = Plastic Leaded Chip Carrier - PL 032
- d. OPERATING CONDITIONS
  - C = Commercial (0°C to 70°C)

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to + 7.0 V
Input voltage .....	-0.5 V to $V_{CC} + 0.5$ V
Operating temperature .....	0°C to + 70°C
Storage temperature .....	-55°C to + 150°C
Power dissipation .....	1.0 W
DC output current .....	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## DC CHARACTERISTICS Commercial: $V_{CC} = 5 \text{ V} \pm 10\%$ , $T_A = 0^\circ\text{C}$ to + 70°C

Parameter Symbol	Parameter Description	Am7204-25 $t_A = 25 \text{ ns}$		Am7204-35 $t_A = 35 \text{ ns}$		Am7204-50 $t_A = 50 \text{ ns}$		Am7204-65 $t_A = 65 \text{ ns}$		Am7204-80 $t_A = 80 \text{ ns}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$I_{IL}$	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	-1	1	$\mu\text{A}$
$I_{IO}$	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$V_{IH}$	Input High Voltage (all inputs except $\overline{XI}$ ) (Note 3)	2.0	-	2.0	-	2.0	-	2.0	-	2.0	-	V
$V_{IL}$	Input Low Voltage (all inputs except $\overline{XI}$ ) (Note 3)	-	0.8	-	0.8	-	0.8	-	0.8	-	0.8	V
$V_{IH(XI)}$	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	-	3.5	-	3.5	-	3.5	-	3.5	-	V
$V_{IL(XI)}$	Input Low Voltage, $\overline{XI}$ (Note 3)	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	V
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2 \text{ mA}$	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	V
$V_{OL}$	Output Logic "0" voltage $I_{OL} = 8 \text{ mA}$	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V
$I_{CC1}$	Average $V_{CC}$ Power Supply Current (Note 4)	-	70	-	60	-	60	-	60	-	60	mA
$I_{CC2}$	Average Standby Current ( $\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$ ) (Note 4)	-	20	-	20	-	20	-	20	-	20	mA
$I_{CC3}$	Power Down Current (all inputs = $V_{CC} - 0.2 \text{ V}$ ) (Note 4)	-	5	-	5	-	5	-	5	-	5	mA

- Notes:
1. Measurements with  $\text{GND} \leq V_{IN} \leq V_{CC}$ .
  2.  $\overline{R} \geq V_{IH}$ ,  $\text{GND} \leq V_{OUT} \leq V_{CC}$ .
  3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
  4.  $I_{CC}$  measurements are made with outputs open.

**AC CHARACTERISTICS**  $V_{CC} = 5 V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$

Parameter Symbol	Parameter Description	Figures	Am7204-25 Min. Max.	Am7204-35 Min. Max.	Am7204-50 Min. Max.	Am7204-65 Min. Max.	Am7204-80 Min. Max.	Unit
<b>Write and Flag Timing</b>								
$t_{WC}$	Write Cycle Time	3	35	45	65	80	100	ns
$t_{WPW}$	Write Pulse Width	3	25	35	50	65	80	ns
$t_{WR}$	Write Recovery Time	3	10	10	15	15	20	ns
$t_{DS}$	Data Setup Time	3,9	15	18	30	30	40	ns
$t_{DH}$	Data Hold Time	3,9	0	0	5	10	10	ns
$t_{WFF}$	Write LOW to Full Flag LOW	6,9	25	30	45	60	60	ns
$t_{WHF}$	Write LOW to Half-Full Flag LOW	5	35	45	65	80	100	ns
$t_{WEF}$	Write HIGH to Empty Flag HIGH	4,8	25	30	45	60	60	ns
$t_{WLZ}$	Write pulse HIGH to data bus at LOW Z (Note 1)	8	5	10	15	15	20	ns
<b>Read and Flag Timing</b>								
$t_{RC}$	Read Cycle Time	3	35	45	65	80	100	ns
$t_A$	Access Time	3,4,8,9	25	35	50	65	80	ns
$t_{RR}$	Read Recovery Time	3	10	10	15	15	20	ns
$t_{RPW}$	Read Pulse Width	3	25	35	50	65	80	ns
$t_{RLZ}$	Read pulse LOW to data bus at LOW Z (Note 1)	3	5	5	10	10	10	ns
$t_{DV}$	Data Valid from read pulse HIGH	3	5	5	5	5	5	ns
$t_{RHZ}$	Read pulse HIGH to data bus at HIGH Z (Note 1)	3	18	20	30	30	30	ns
$t_{RFF}$	Read HIGH to Full Flag HIGH	6,9	25	30	45	60	60	ns
$t_{RHF}$	Read HIGH to Half-Full-Flag HIGH	5	35	45	65	80	100	ns
$t_{REF}$	Read LOW to Empty Flag LOW	4,8	25	30	45	60	60	ns
<b>Reset Timing</b>								
$t_{RSC}$	Reset Cycle Time	2	35	45	65	80	100	ns
$t_{RS}$	Reset Pulse Width	2	25	35	50	65	80	ns
$t_{RSS}$	Reset Setup Time	2	25	35	50	65	80	ns
$t_{RSR}$	Reset Recovery Time	2	10	10	15	15	20	ns
$t_{EFL}$	Reset to Empty Flag LOW	2	35	45	65	80	100	ns
$t_{HFH}$	Reset to Half-Full Flag High	2	35	45	65	80	100	ns
$t_{FFH}$	Reset to Full Flag HIGH	2	35	45	65	80	100	ns
<b>Retransmit Timing</b>								
$t_{RTC}$	Retransmit Cycle Time	7	35	45	65	80	100	ns
$t_{RT}$	Retransmit Pulse Width	7	25	35	50	65	80	ns
$t_{RTR}$	Retransmit Recovery Time	7	10	10	15	15	20	ns

Note: 1. Characterized parameters.

2

## FUNCTIONAL DESCRIPTION

The Am7204 CMOS FIFO is designed around a 4096x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 4095. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7204. The write, read, data-in and data-out lines of the Am7204 are connected in parallel, and the Expansion-Out (XO) and the Expansion-In (XI) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between XO and XI.

## OPERATIONAL DESCRIPTION

### Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of XI and FL are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read (R) and Write (W) signals must be HIGH  $t_{RSS}$  prior to and  $t_{RSR}$  after the rising edge of Reset (RS). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag (EF) being LOW, active, and both the Half-Full (HF) and Full Flag (FF) being HIGH, inactive.

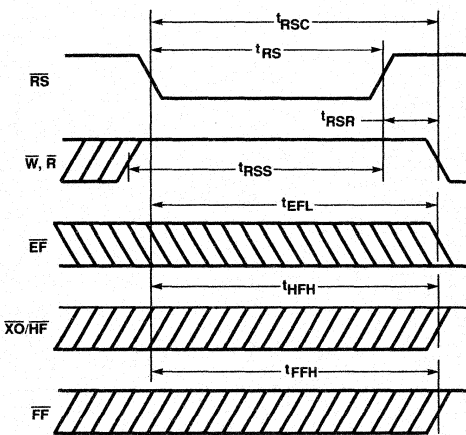


Figure 2. Reset Timing

### Writing Data To The FIFO

The HIGH state of the Full Flag ( $\overline{FF}$ ) indicates that the FIFO is capable of accepting data. The falling edge of Write (W) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8  $t_{DS}$  prior to and  $t_{DH}$  after the rising edge of W will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ( $\overline{EF}$ ) occurs  $t_{WEF}$  after the rising edge of W during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag /HF will go LOW  $t_{WHF}$  after the falling edge of W during the write operation which creates the half-full condition. (See Figure 5.) HF will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 2048 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag (FF) goes LOW  $t_{WFF}$  after the falling edge of W during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 4096 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

### Reading Data From The FIFO

The HIGH state of the Empty Flag ( $\overline{EF}$ ) indicates that the FIFO is ready to output data. The falling edge of Read (R) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8  $t_{x}$  after the falling edge of R, and remains until  $t_{dV}$  after the rising edge of R. Q0-Q8 return to a high-impedance state when a valid read is not in progress.

The Full Flag ( $\overline{FF}$ ) will go HIGH  $t_{RFF}$  after the rising edge of R during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag (HF) will go HIGH  $t_{RHF}$  after the rising edge of R during the read operation, which eliminates the half-full condition. (See Figure 5.) HF will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 2047 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of EF occurs  $t_{REF}$  after the falling edge of R during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

### Half-Full Flag

The Half-Full (HF) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 2048 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 2048 words, and Read and Write pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

HF will always settle to the correct state after the appropriate delay,  $t_{WHF}$  or  $t_{RHF}$ . This property of the Half-Full Flag is clearly a function of the dynamic relation between W and R. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

## RESET AND RETRANSMIT TRUTH TABLE Single-Device Configuration/Width-Expansion Mode

Mode	Input			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes: 1. Flags will change to show correct state according to write pointer.

2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

## RESET AND FIRST LOAD TRUTH TABLE Depth-Expansion/Compound-Expansion Mode

Mode	Input			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset—first device	0	0	$\overline{X0}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{X0}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{X0}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes: 1.  $\overline{XI}$  is connected to  $\overline{X0}$  of previous device. See Figure 12.

2. Same as during Reset Cycle.

3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

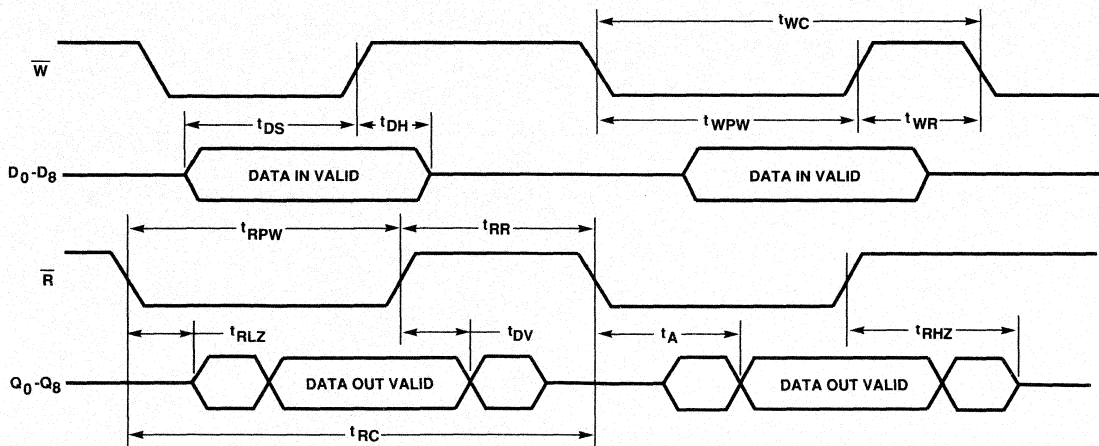


Figure 3. Asynchronous Write and Read Timing

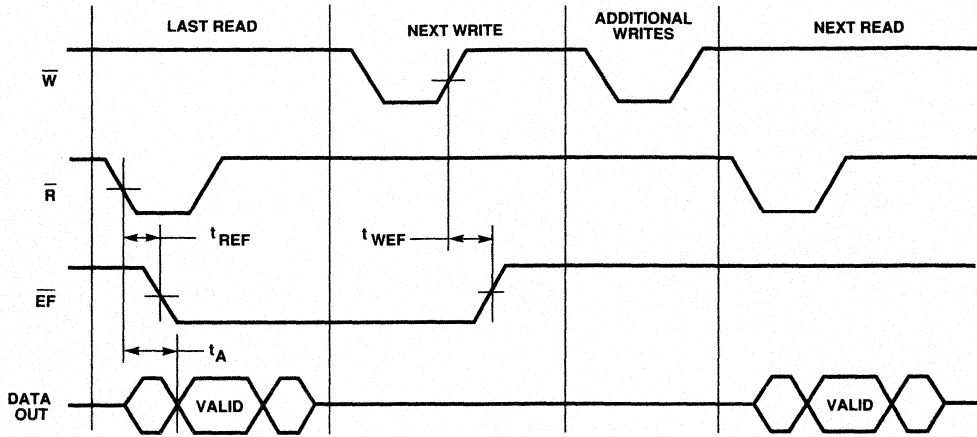
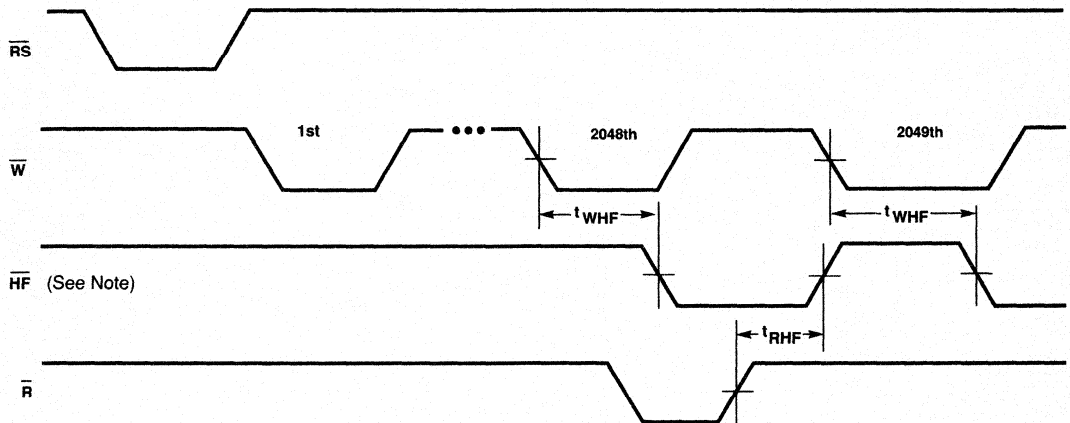


Figure 4. Empty Flag Timing



Note: Depending on the precise phase of  $\overline{W}$  and  $\overline{R}$ , the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when  $\overline{W}$  and  $\overline{R}$  are operating asynchronously near half full.

Figure 5. Half-Full Flag Timing

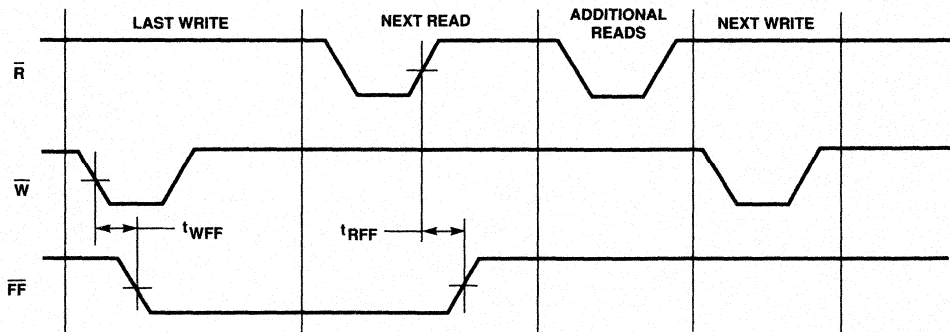


Figure 6. Full Flag Timing



## Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 4096 or less writes between reset cycles.

The  $\overline{FL}/\overline{RT}$  is used as the Retransmit ( $\overline{RT}$ ) input in Single-Device Mode.  $\overline{RT}$ , an active LOW-going pulse of at least  $t_{RT}$  in duration, returns the internal read pointer to address zero and leaves the write pointer unaffected.  $\overline{W}$  and  $\overline{R}$  must both be HIGH during the retransmit cycle. The first write or read cycle should not start until  $t_{RTR}$  after the rising edge of  $\overline{RT}$ . The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO  $t_{RTC}$  after the falling edge of  $\overline{RT}$ . (See Figure 7 and Table 1).

### Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ( $\overline{XI}$ ) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7204 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used

as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time ( $t_{WEP}$ ,  $t_{WHF}$ ,  $t_{WFF}$ ,  $t_{REF}$ ,  $t_{RHF}$ , and  $t_{RFF}$ ) for each flag has elapsed.

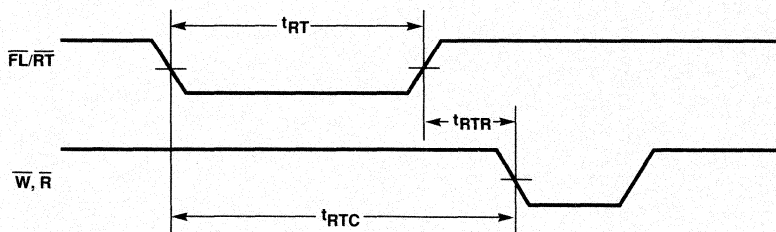
### Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ( $\overline{XO}$ ) of one device must be connected to Expansion In ( $\overline{XI}$ ) of the next device, with  $\overline{XO}$  of the last device being connected to  $\overline{XI}$  of the first device. The device that is to receive data first has its First Load ( $\overline{FL}$ ) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using  $\overline{XO}$  and  $\overline{XI}$ . A LOW-going pulse on  $\overline{XO}$  occurs when the last physical location of an active device, address 4095, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the FF outputs together. Likewise, a composite Empty Flag is created by OR-ing all the  $\overline{EF}$  outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

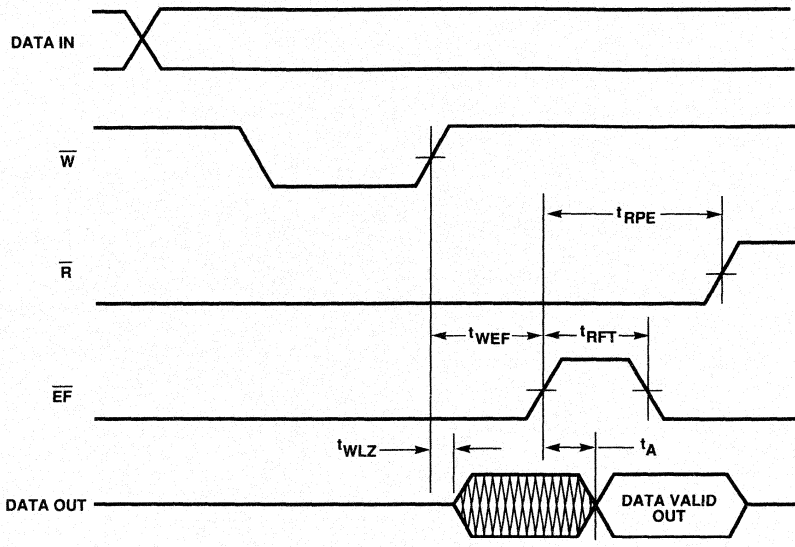
### Compound Expansion

FIFOs of greater width and depth than the Am7204 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)



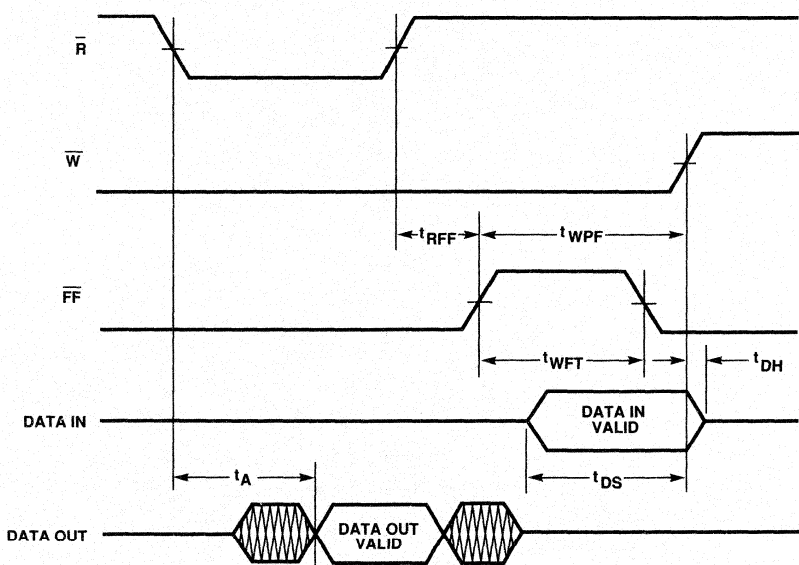
Note:  $\overline{EF}$ ,  $\overline{HF}$  and  $\overline{FF}$  may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at  $t_{RTC}$ .

Figure 7. Retransmit Timing



Note: ( $t_{RPE} = t_{RPW}$ ,  $t_{RFT} = t_{REF}$ )

Figure 8. Read Data Flow-Through Mode



Note: ( $t_{WPF} = t_{WPW}$ ,  $t_{WFT} = t_{WFF}$ )

Figure 9. Write Data Flow-Through Mode

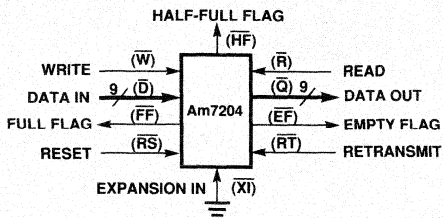


Figure 10. Single FIFO Configuration

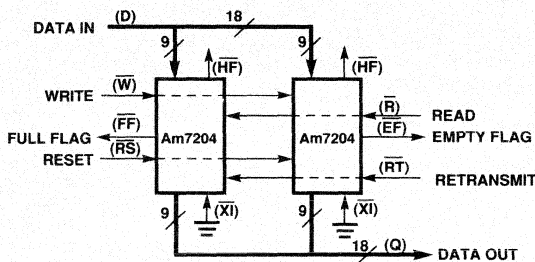


Figure 11. Width-Expansion to Form a 512x18 FIFO

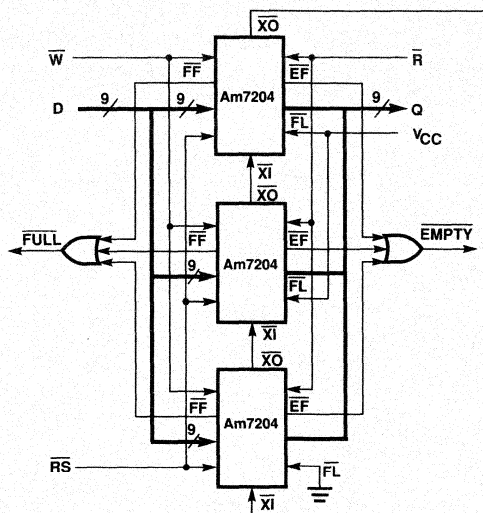


Figure 12. Depth-Expansion to Form a 12288x9 FIFO

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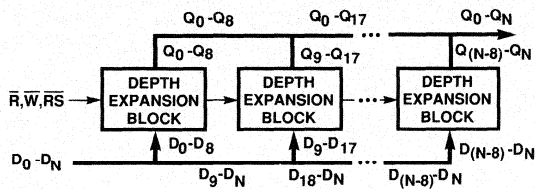


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

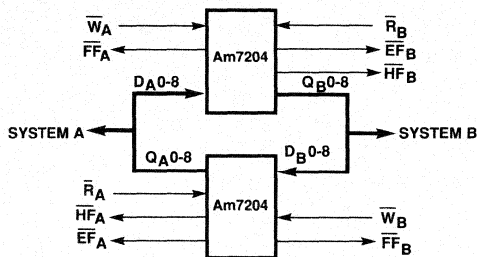
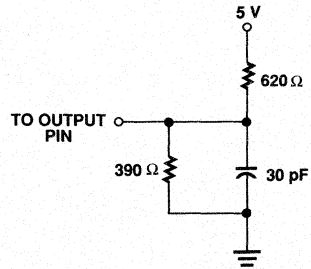


Figure 14. Bidirectional FIFO Mode

## AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



\* Includes jig and scope capacitances.

Figure 15. A.C. Test Load

## CAPACITANCE ( $T_A = +25^\circ\text{C}$ , $f = 1.0\text{ MHz}$ )

Symbol	Parameter (Note 1)	Conditions	Typ.	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$	5	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$	7	pF

Note: 1. For reference only.

# 67C401/13 67C402/23

First-In First-Out (FIFO)  
64x4, 64x5 CMOS MEMORY 25/35 MHZ (Cascadable)



Advanced  
Micro  
Devices

## FEATURES

- Zero standby power
- High-speed 35-MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- RAM-based architecture for short fall-through delay
- Full CMOS cell for maximum noise immunity
- Asynchronous operation
- Output Enable feature (67C4013/23)

## ORDERING INFORMATION

67 C 401 - 35 N	
OPERATING CONDITIONS	PACKAGE TYPE
67 = Commercial (0°C to 70°C)	N = Plastic DIP - PD 020 J = Ceramic DIP - CD 020 NL = Plastic Leaded Chip Carrier - PL 020
CMOS TECHNOLOGY	PERFORMANCE
PART NUMBER	35 = 35 MHz Shift Rate 25 = 25 MHz Shift Rate
401 = 64x4, Totem Pole Output	
4013 = 64x4, Three-State Output	
402 = 64x5, Totem Pole Output	
4023 = 64x5, Three-State Output	

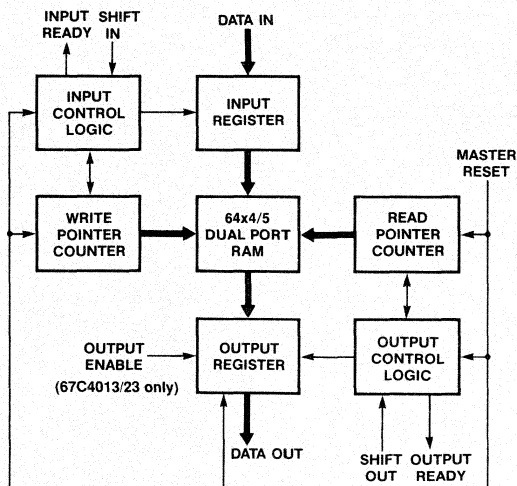
## GENERAL DESCRIPTION

The 67C40X/XX series devices are high-performance CMOS RAM-based First-In First-Out (FIFO) buffer memory products organized as 64 words by 4 or by 5 bits wide. These devices use Advanced Micro Devices latest CMOS process technology and meet the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using both Read and Write pointers for addressing each memory

location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disc controllers, graphics, and communication network systems. The 550- $\mu$ watt standby power specification makes these devices ideal for ultra-low-power and battery-powered systems.

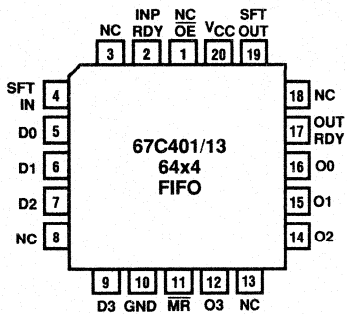
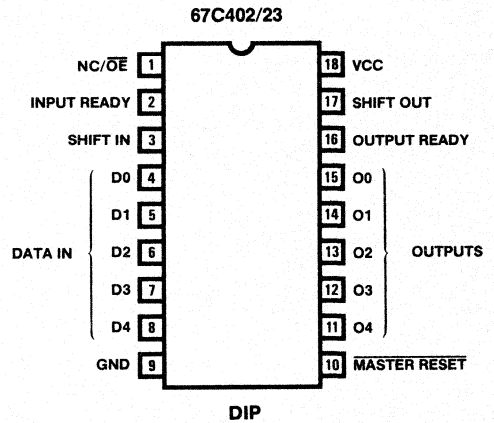
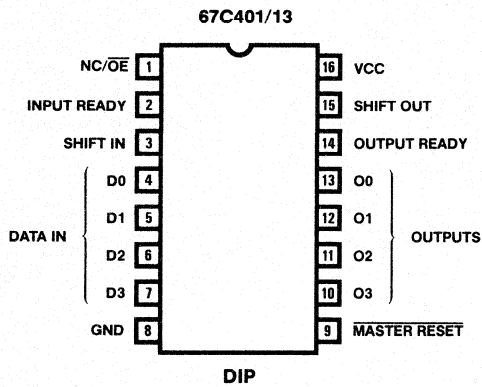
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## BLOCK DIAGRAM

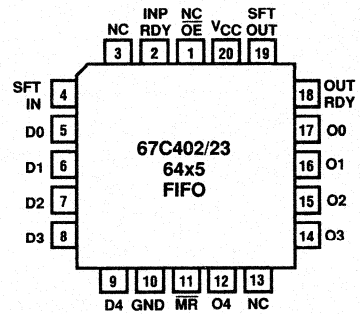


Publication # 10998 Rev. B Amendment /0  
Issue Date: January 1989

# CONNECTION DIAGRAMS



Plastic Leaded Chip Carrier



Plastic Leaded Chip Carrier

## ABSOLUTE MAXIMUM RATINGS

Supply voltage $V_{CC}$ .....	-0.5 V to 7 V
Input voltage .....	-1.5 V to 7 V
Off-state output voltage .....	-0.5 V to $V_{CC} + 0.5$ V
Storage temperature .....	-65°C to +150°C
Power dissipation .....	1.0 W

Note:

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## OPERATING CONDITIONS Commercial: $V_{CC} = 5\text{ V} \pm 10\%$ , $T_A = 0^\circ\text{C to } +70^\circ\text{C}$

SYMBOL	PARAMETER	FIGURE	67C40X/XX-25		67C40X/XX-35		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		4.5	5.5	4.5	5.5	V
$T_A$	Operating free-air temperature		0	70	0	70	°C
$f_{IN}$	Shift in rate	1		25		35	MHz
$t_{SIH}^*$	Shift in HIGH time	1	8		8		ns
$t_{SIL}^*$	Shift in LOW time	1	8		8		ns
$t_{IDS}$	Input data setup to SI (Shift In)	1	0		0		ns
$t_{IDH}$	Input data hold time from SI (Shift In)	1	20		15		ns
$t_{RIDS}$	Input data setup to IR (Input Ready)	3	5		2		ns
$t_{RIDH}$	Input data hold time from IR (Input Ready)	3	20		15		ns
$f_{OUT}$	Shift out rate	4		25		35	MHz
$t_{SOH}^*$	Shift out HIGH time	4	8		8		ns
$t_{SOL}^*$	Shift out LOW time	4	8		8		ns
$t_{MRW}$	Master Reset pulse	8	25		18		ns
$t_{MRS}$	Master Reset to SI	8	10		7		ns

\* See AC test and high-speed application note.

## DC CHARACTERISTICS $V_{CC} = 5\text{ V} \pm 10\%$ , $T_A = 0^\circ\text{C to } +70^\circ\text{C}$

SYMBOL	PARAMETER	TEST CONDITION	67C40X/XX-25		67C40X/XX-35		UNIT
			MIN	MAX	MIN	MAX	
$V_{IL}^*$	Low-level input voltage			0.8		0.8	V
$V_{IH}^*$	High-level input voltage		2		2		V
$I_{IN}$	Input current	$V_{CC} = \text{MAX}$ $GND < V_{IN} < V_{CC}$	-1	1	-1	1	$\mu\text{A}$
$I_{OZ}$	Off-state output current	$V_{CC} = \text{MAX}$ $GND < V_{OUT} < V_{CC}$	-5	5	-5	5	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 20\ \mu\text{A}$	0.1		0.1	V
			$I_{OL} = 8\ \text{mA}$	0.4		0.4	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -20\ \mu\text{A}$	$V_{CC} - 0.1$		$V_{CC} - 0.1$	V
			$I_{OH} = -4\ \text{mA}$	2.4		2.4	
$I_{OS}^{**}$	Output short-circuit current	$V_{CC} = \text{MAX}$ $V_O = 0\ \text{V}$	-90	-20	-90	-20	mA
$I_{CC}$	Standby supply current	$V_{CC} = \text{MAX}$ $I_{OUT} = 0$	$V_{IH} = V_{CC}$ $V_{IL} = GND$	100		100	$\mu\text{A}$
	Operating supply current		$V_{IH} = \text{MIN}$ , $V_{IL} = \text{MAX}$ $f_{IN} = f_{OUT} = \text{MAX}$	50		60	mA

\* These are absolute voltages with respect to GND and include all overshoots due to system and/or tester noise.

\*\* Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.



## SWITCHING CHARACTERISTICS Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67C40X/XX-25		67C40X/XX-35		UNIT
			MIN	MAX	MIN	MAX	
$t_{IRL}^*$	Shift In $\uparrow$ to Input Ready LOW	1		21		18	ns
$t_{IRH}^*$	Shift In $\downarrow$ to Input Ready HIGH			28		20	ns
$t_{ORL}^*$	Shift Out $\uparrow$ to Output Ready LOW	4		19		18	ns
$t_{ORH}^*$	Shift Out $\downarrow$ to Output Ready HIGH			34		20	ns
$t_{ODH}$	Output Data Hold (previous word)		5		5		ns
$t_{ODS}$	Output Data Shift (next word)			34		20	ns
$t_{PT}$	Data throughput		3,6		40		34
$t_{MRORL}$	Master Reset $\downarrow$ to Output Ready LOW	8		35		28	ns
$t_{MRIRH}$	Master Reset $\downarrow$ to Input Ready HIGH			35		28	ns
$t_{MRO}$	Master Reset $\downarrow$ to Outputs LOW			25		22	ns
$t_{IPH}$	Input Ready pulse HIGH	3	8		8		ns
$t_{OPH}$	Output Ready pulse HIGH	6	8		8		ns
$t_{ORD}$	Output Ready $\uparrow$ to Data Valid	4		0		0	ns
$t_{PHZ}^{**}$	Output Disable Delay	A		15		12	ns
$t_{PLZ}^{**}$				15		12	
$t_{PZL}^{**}$	Output Enable Delay			20		15	ns
$t_{PZH}^{**}$				20		15	

\* See AC test and high-speed application note.

\*\* Enable/Disable delays refer to 67C4013/23 only.

## CAPACITANCES\*

SYMBOL	PARAMETER	TEST CONDITION	67C40X/XX-25		67C40X/XX-35		UNIT
			MIN	MAX	MIN	MAX	
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ $V_{CC} = 4.5\text{ V}$		10		10	pF
$C_{OUT}$	Output capacitance			7		7	pF

\* Not tested in production.

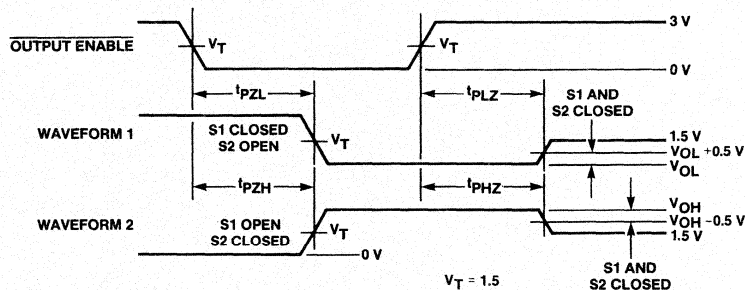


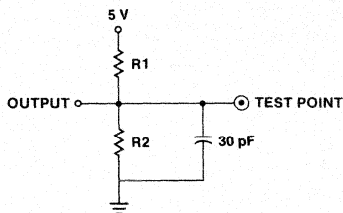
Figure A. Enable and Disable

Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.



## STANDARD AC TEST LOAD

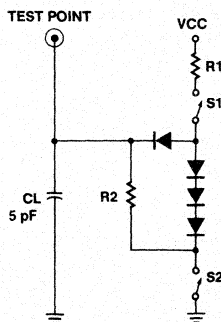


Input Pulse Amplitude = 3 V  
 Input Rise and Fall Time (10%-90%) = 2.5 ns  
 Measurements made at 1.5 V  
 All Diodes are 1N916 or 1N3064

## RESISTOR VALUES

$I_{OL}$	R1	R2
8 mA	600 $\Omega$	1200 $\Omega$

## THREE-STATE TEST LOAD



2

## FUNCTIONAL DESCRIPTION

### Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the  $D_x$  inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

### Data Output

Data is read from the  $O_x$  outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and  $O_x$  remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

## AC TEST AND HIGH-SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Advanced Micro Devices recommends a monolithic ceramic capacitor of 0.1  $\mu$ F directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., a rising edge of the Shift-In

pulse is not recognized until Input Ready is HIGH. If Input Ready is not HIGH due to (a) too high a frequency, or (b) FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time ( $t_{IDH}$ ) and the next activity of Input Ready ( $t_{IRL}$ ) to be extended relative to Shift-In going HIGH. This same type of problem also relates to  $t_{IRH}$ ,  $t_{ORL}$ , and  $t_{ORH}$ . For high-speed applications, proper grounding technique is essential. In order to diminish timing ambiguities between the Shift-In-Input-Ready or Shift-Out-Output-Ready pairs when operating at high frequencies, it is recommended that the  $t_{SIH}$  and  $t_{SOH}$  pulse widths be as short as possible within the specified limits.

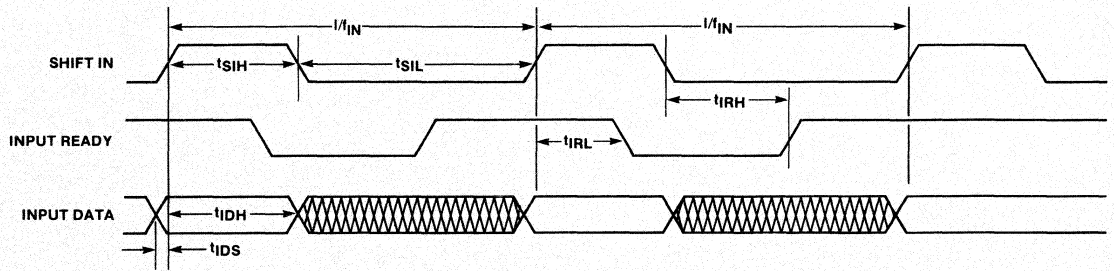


Figure 1. Input Timing

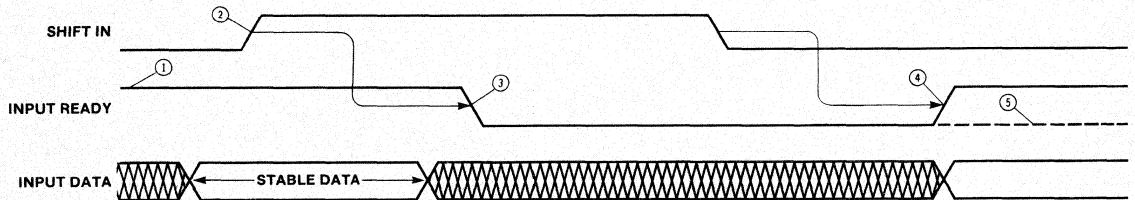


Figure 2. The Mechanism of Shifting Data into the FIFO

- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- ② Input Data is loaded into the first available memory location.
- ③ Input Ready goes LOW indicating this memory location is full.
- ④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
- ⑤ If the FIFO is already full then the Input Ready remains LOW.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

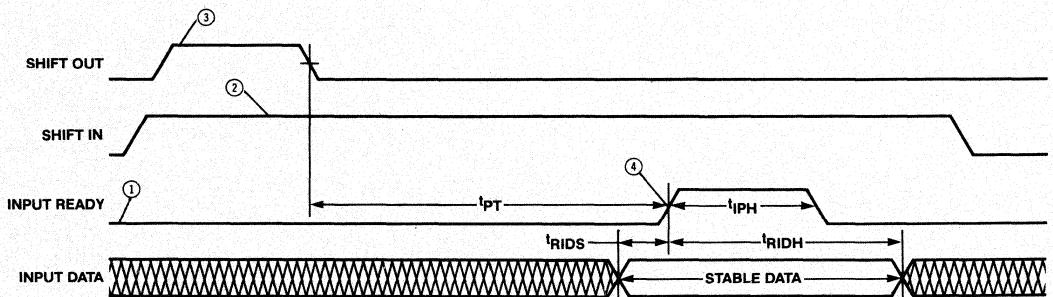


Figure 3. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- ① FIFO is initially full.
- ② Shift In is held HIGH.
- ③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
- ④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

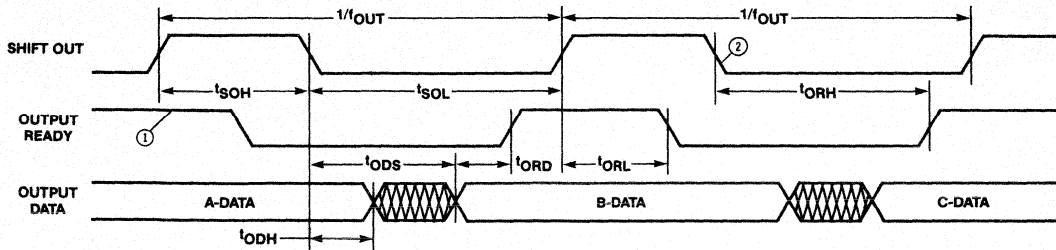


Figure 4. Output Timing

- ① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
- ② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

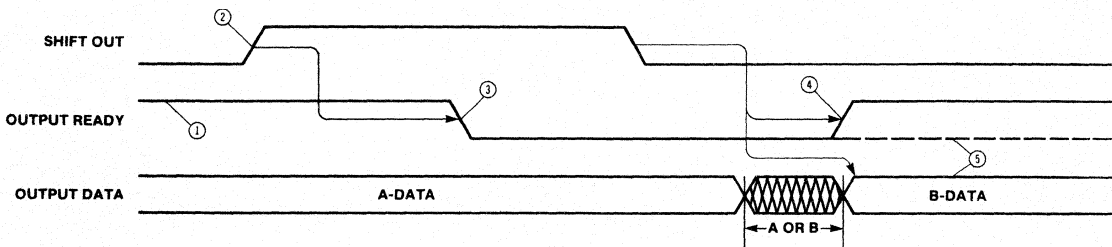


Figure 5. The Mechanism of Shifting Data Out of the FIFO

- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
- ③ Output Ready goes LOW.
- ④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- ⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

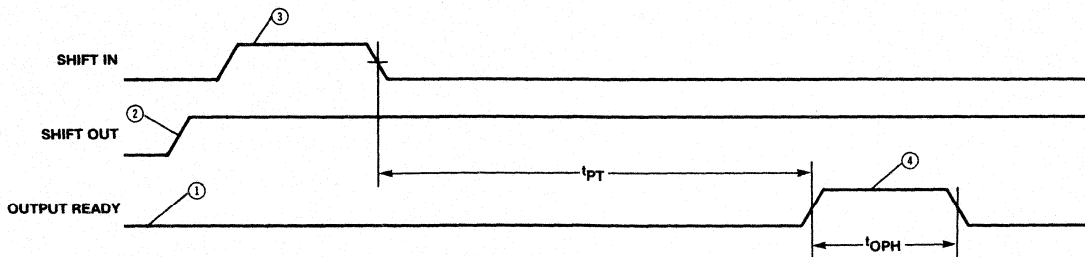
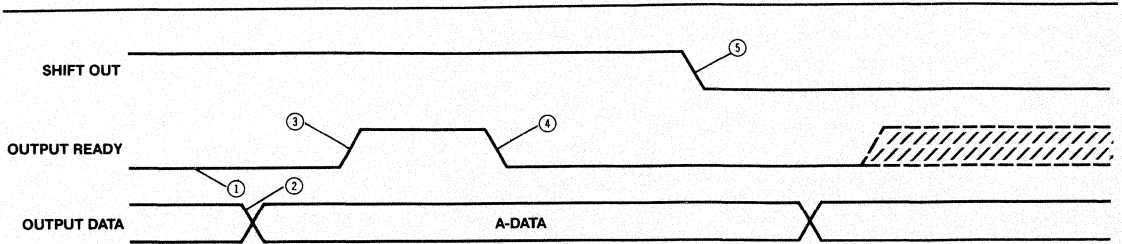


Figure 6.  $t_{PT}$  and  $t_{OPH}$  Specification

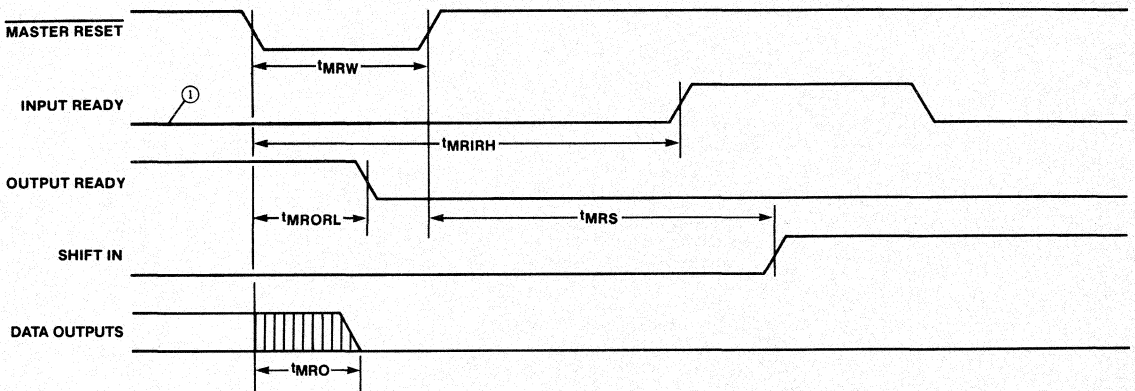
- ① FIFO initially empty.
- ② Shift-Out held HIGH.
- ③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
- ④ As soon as Output Ready becomes HIGH, the word is shifted out.

2



**Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH**

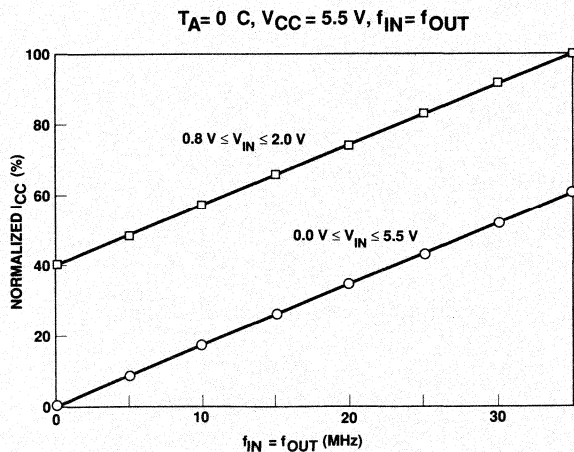
- ① The internal logic does not detect the presence of any words in the FIFO.
- ② New data (A) arrives at the outputs.
- ③ Output Ready goes HIGH indicating arrival of the new data.
- ④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- ⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or remain LOW depending on whether there are any additional words in the FIFO.



① FIFO is initially full.

**Figure 8. Master Reset Timing**

## NORMALIZED $I_{CC}$ vs FREQUENCY





Advanced  
Micro  
Devices

# 67C401/13 67C402/23

First-In First-Out (FIFO) 64x4, 64x5 Memory  
10/15 MHz (Cascadable) CMOS

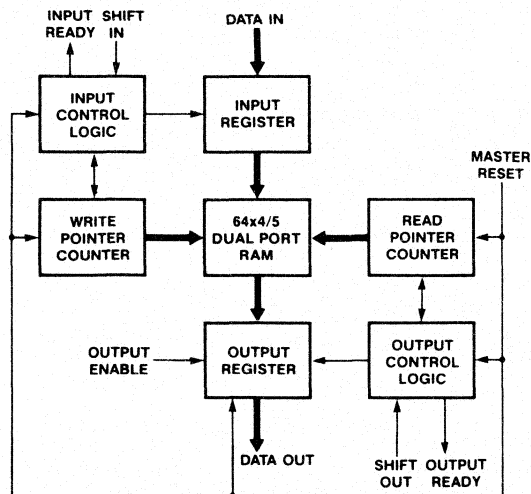
## Features

- Zero standby power
- High-speed 15-MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- RAM-based architecture for short fall-through delay
- Full CMOS 8-transistor cell for maximum noise immunity
- Asynchronous operation
- Output Enable feature (67C4013/23)

## General Description

The 67C40X/XX series devices are high-performance CMOS RAM-based First-In First-Out (FIFO) buffer memory products organized as 64 words by 4 or by 5 bits wide. These devices use Monolithic Memories' latest CMOS process technology and meet the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using both Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disc controllers, graphics, and communication network systems. The 550- $\mu$ watt standby power specification makes these devices ideal for ultra-low-power and battery-powered systems.

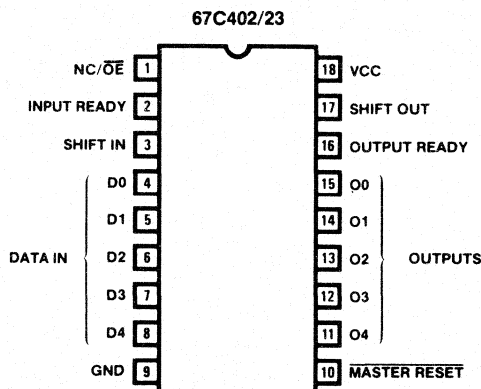
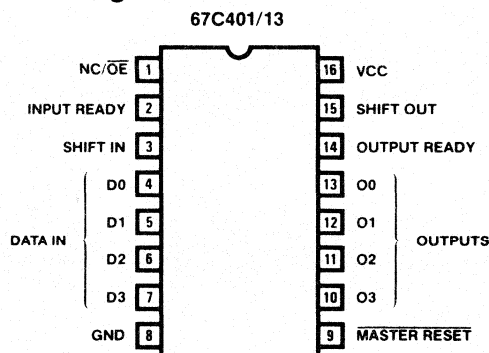
## Block Diagram



## Ordering Information

Part Number	Package	Temp	Output	Description
67401-10	CD 020, PD 020, PL 020	Com	Totem Pole	10 MHz 64x4
67401-15		Com	Totem Pole	15 MHz 64x4
674013-10		Com	3-State	10 MHz 64x4
674013-15		Com	3-State	15MHz 64x4
67C402-10		Com	Totem Pole	10MHz 64x5
67C402-15		Com	Totem Pole	15MHz 64x5
67C4023-10		Com	3-State	10MHz 64x5
67C4023-15		Com	3-State	15MHz 64x5

## Pin Configurations



Publication # Rev. Amendment  
10683 A /0  
Issue Date: May 1988

## Absolute Maximum Ratings

Supply voltage $V_{CC}$	-0.5 V to 7 V
Input voltage	-1.5 V to 7 V
Off-state output voltage	-0.5 V to $V_{CC} + 0.5$ V
Storage temperature	-65°C to +150°C
Power dissipation	1.0 W
Latch-up trigger current (all outputs)	140 mA

## Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	67C40X/XX-10		67C40X/XX-15		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		4.5	5.5	4.5	5.5	V
$T_A$	Operating free-air temperature		0	70	0	70	°C
$f_{IN}$	Shift in rate	1		10		15	MHz
$t_{SIH}$	Shift in HIGH time	1,B	14		14		ns
$t_{SIL}$	Shift in LOW time	1	25		25		ns
$t_{IDS}$	Input data setup to SI (Shift In)	1	0		0		ns
$t_{IDH}$	Input data hold time from SI (Shift In)	1	40		40		ns
$t_{RIDS}$	Input data setup to IR (Input Ready)	3	0		0		ns
$t_{RIDH}$	Input data hold time from IR (Input Ready)	3	30		30		ns
$f_{OUT}$	Shift out rate	4		10		15	MHz
$t_{SOH}$	Shift out HIGH time	4,B	24		21		ns
$t_{SOL}$	Shift out LOW time	4	25		25		ns
$t_{MRW}^*$	Master Reset pulse	8	35		35		ns
$t_{MRS}$	Master Reset to SI	8	65		65		ns

\* See AC test and high-speed application note

## Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION	67C40X/XX-10		67C40X/XX-15		UNIT
			MIN	MAX	MIN	MAX	
$V_{IL}^*$	Low-level input voltage			0.8		0.8	V
$V_{IH}^*$	High-level input voltage		2		2		V
$I_{IN}$	Input current	$V_{CC} = \text{MAX}$ $GND < V_{IN} < V_{CC}$	-1	1	-1	1	$\mu\text{A}$
$I_{OZ}$	Off-state output current	$V_{CC} = \text{MAX}$ $GND < V_{OUT} < V_{CC}$	-5	5	-5	5	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 20 \mu\text{A}$		0.1		V
			$I_{OL} = 8 \text{ mA}$		0.4		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -20 \mu\text{A}$		$V_{CC} - 0.1$		V
			$I_{OH} = -4 \text{ mA}$		2.4		
$I_{OS}^{**}$	Output short-circuit current	$V_{CC} = \text{MAX}$ $V_O = 0 \text{ V}$	-90	-20	-90	-20	mA
$I_{CC}$	Standby supply current	$V_{CC} = \text{MAX}$ $I_{OUT} = 0$	$V_{IH} = V_{CC}$ $V_{IL} = GND$		100		$\mu\text{A}$
	Operating supply current		$V_{IH} = \text{MIN}$ , $V_{IL} = \text{MAX}$ $f_{IN} = f_{OUT} = \text{MAX}$		35		mA

\* These are absolute voltages with respect to GND (Pin 9) and include all overshoots due to system and/or tester noise

\*\* Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second

## Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67C40X/XX-10		67C40X/XX-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{IRL}^*$	Shift In $\uparrow$ to Input Ready LOW	1		60		55	ns
$t_{IRH}^*$	Shift In $\downarrow$ to Input Ready HIGH			50		50	ns
$t_{ORL}^*$	Shift Out $\uparrow$ to Output Ready LOW	4		55		45	ns
$t_{ORH}^*$	Shift Out $\downarrow$ to Output Ready HIGH			50		41	ns
$t_{ODH}$	Output Data Hold (previous word)		5		5		ns
$t_{ODS}$	Output Data Shift (next word)			35		30	ns
$t_{PT}$	Data throughput	3.6		100		90	ns
$t_{MRORL}$	Master Reset $\downarrow$ to Output Ready LOW	8		100		100	ns
$t_{MRIRH}$	Master Reset $\downarrow$ to Input Ready HIGH			100		100	ns
$t_{MRO}$	Master Reset $\downarrow$ to Outputs LOW			35		35	ns
$t_{IPH}$	Input ready pulse HIGH	3.B	19		16		ns
$t_{OPH}$	Output ready pulse HIGH	6.B	14		14		ns
$t_{ORD}$	Output ready $\uparrow$ to Data Valid	4		-3		-3	ns
$t_{PHZ}$	Output Disable Delay	A		25		25	ns
$t_{PLZ}$				25		25	
$t_{PZL}$	Output Enable Delay			30		30	ns
$t_{PZH}$				30		30	

\* See AC test and high-speed application note.

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## Capacitances\*

SYMBOL	PARAMETER	TEST CONDITION	67C40X/XX-10		67C40X/XX-15		UNIT
			MIN	MAX	MIN	MAX	
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ $V_{CC} = 4.5\text{ V}$		10		10	pF
$C_{OUT}$	Output capacitance			7		7	pF

\* Not tested in production.

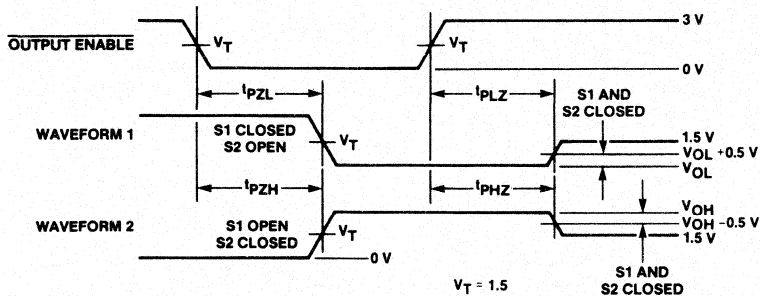
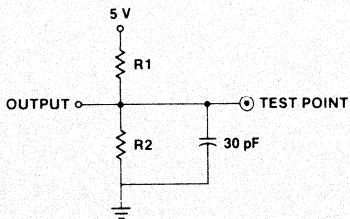


Figure A. Enable and Disable

Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

## Standard AC Test Load

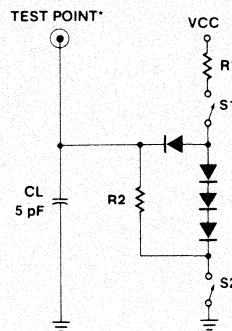


Input Pulse Amplitude = 3 V  
 Input Rise and Fall Time (10%-90%) = 2.5 ns  
 Measurements made at 1.5 V  
 All Diodes are 1N916 or 1N3064

## Resistor Values

$I_{OL}$	R1	R2
8 mA	600 $\Omega$	1200 $\Omega$

## Three-State Test Load



## Functional Description

### Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the  $D_x$  inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

### Data Output

Data is read from the  $O_x$  outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and  $O_x$  remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

## AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1  $\mu$ F directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time ( $T_{IDH}$ ) and the next activity of Input Ready ( $T_{IRL}$ ) to be extended relative to Shift-In going HIGH. This same type of problem is also related to  $T_{IRH}$ ,  $T_{ORL}$ , and  $T_{ORH}$  as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.



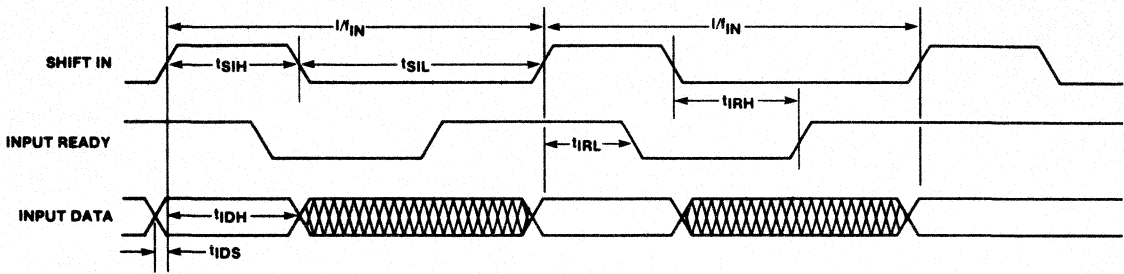


Figure 1. Input Timing

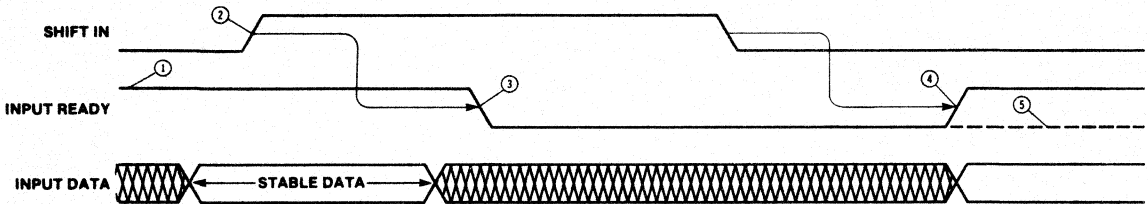


Figure 2. The Mechanism of Shifting Data into the FIFO

2

- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- ② Input Data is loaded into the first available memory location.
- ③ Input Ready goes LOW indicating this memory location is full.
- ④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
- ⑤ If the FIFO is already full then the Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

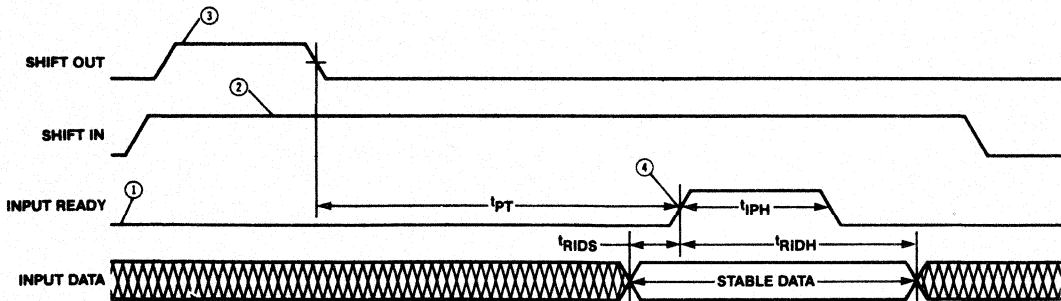


Figure 3. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- ① FIFO is initially full.
- ② Shift In is held HIGH.
- ③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
- ④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

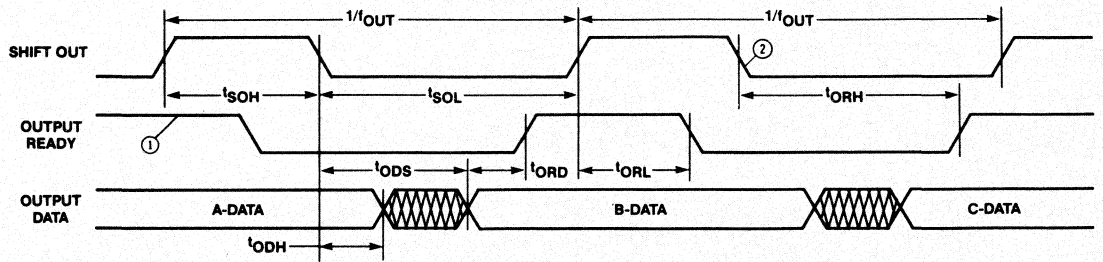


Figure 4. Output Timing

- ① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word)
- ② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

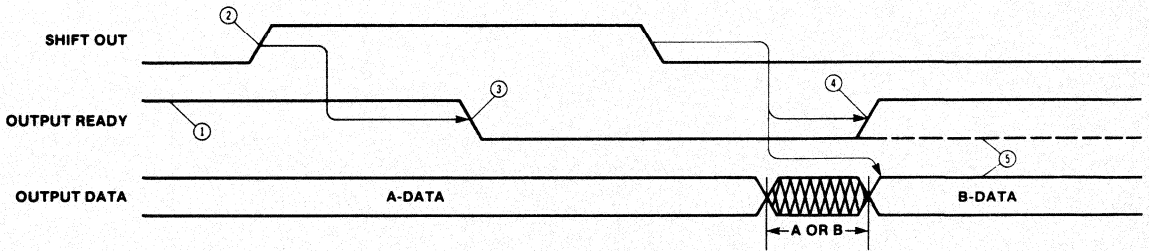


Figure 5. The Mechanism of Shifting Data Out of the FIFO

- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
- ③ Output Ready goes LOW.
- ④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- ⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

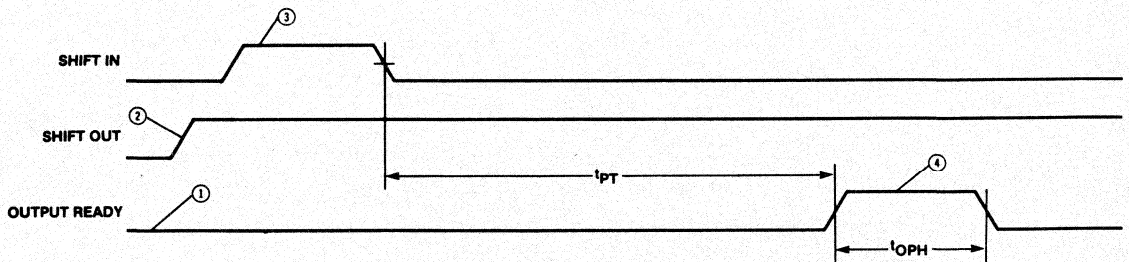


Figure 6.  $t_{PT}$  and  $t_{OPH}$  Specification

- ① FIFO initially empty.
- ② Shift-Out held HIGH.
- ③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
- ④ As soon as Output Ready becomes HIGH, the word is shifted out.

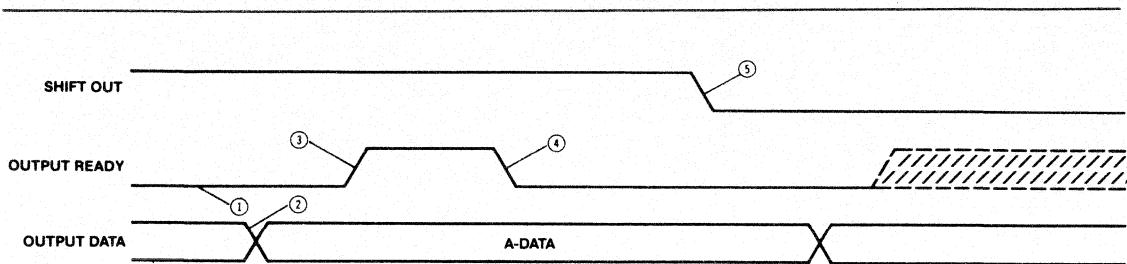


Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

- ① The internal logic does not detect the presence of any words in the FIFO.
- ② New data (A) arrives at the outputs.
- ③ Output Ready goes HIGH indicating arrival of the new data.
- ④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- ⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or remain LOW depending on whether there are any additional words in the FIFO.

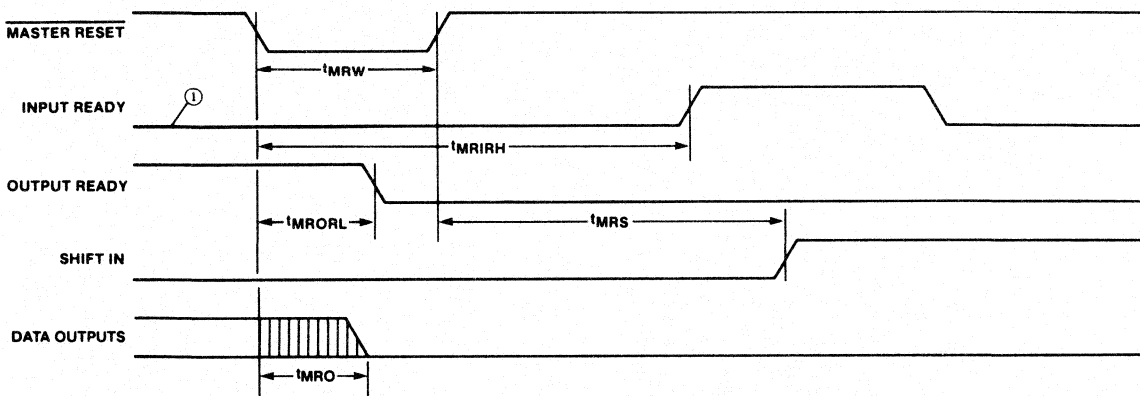
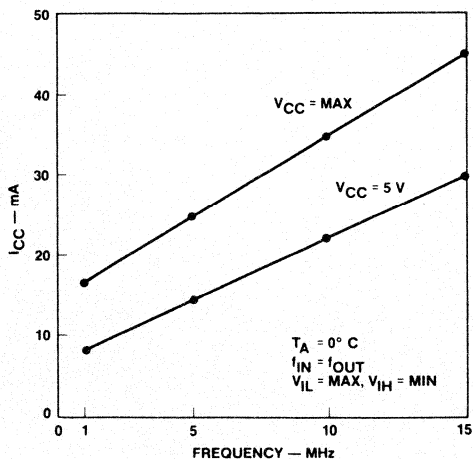


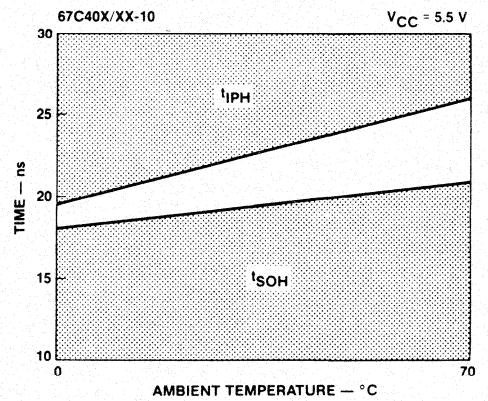
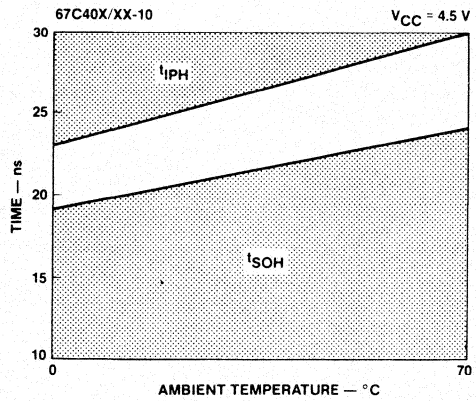
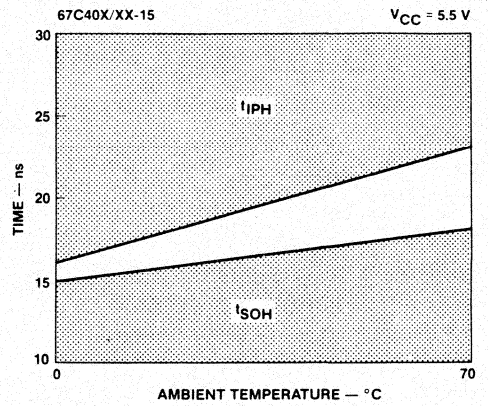
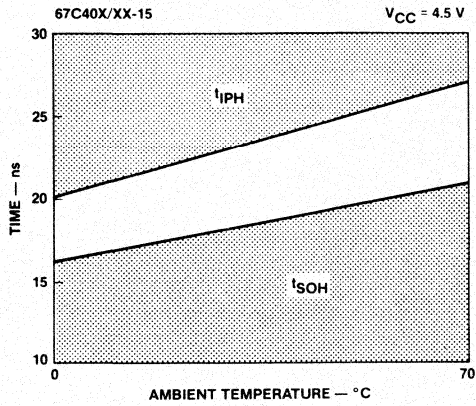
Figure 8. Master Reset Timing

- ① FIFO is initially full.

## ICC vs. Frequency



Guaranteed Distribution of  $t_{1PH}$ ,  $t_{1SOH}$  vs. Temperature (For Cascadability Only)



Guaranteed Distribution of  $t_{OPH}$ ,  $t_{SIH}$  vs. Temperature (For Cascadability Only)

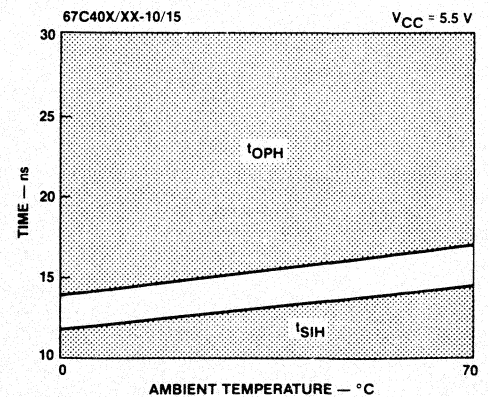
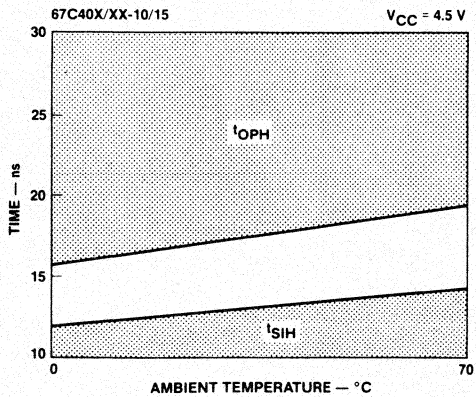


Figure B. Cascadability



# 67C4033

First-In First-Out (FIFO)  
64x5 Memory 10/15 MHz (Cascadable) CMOS

## DISTINCTIVE CHARACTERISTICS

- Zero standby power
- High-speed 15-MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- Half-Full and Almost-Full/Empty status flags
- RAM-based architecture for short fall-through delay
- Full CMOS 8-transistor cell for maximum noise immunity
- Asynchronous operation
- Output enable

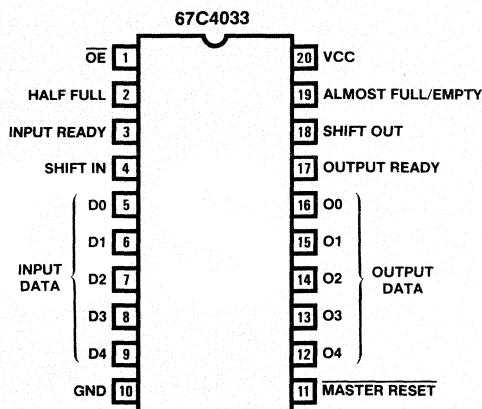
## GENERAL DESCRIPTION

The 67C4033 device is a high-performance CMOS RAM-based First-In First-Out (FIFO) buffer product organized as 64 words by 5 bits wide. This device uses Monolithic Memories' latest CMOS process technology and meets the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disk controllers, graphics, and communication network systems. The 550  $\mu$ watt standby power specification of this device makes it ideal for ultra-low-power and battery-powered systems.

## ORDERING INFORMATION

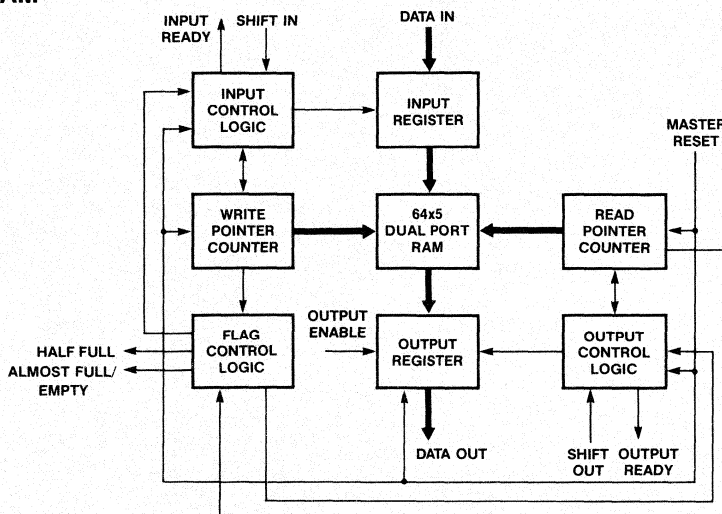
Part Number	Package	Temp	Description
67C4033-10	CD 020, PD 020, PL 020	Com	10 MHz in/out
67C4033-15	CD 020, PD 020, PL 020	Com	15 MHz in/out

## CONNECTION DIAGRAMS



2

## BLOCK DIAGRAM



Publication #	Rev.	Amendment
10684	A	/0
Issue Date: January 1989		

## ABSOLUTE MAXIMUM RATINGS

Supply voltage $V_{CC}$	-0.5 V to 7 V
Input voltage	-1.5 V to 7 V
Off-state output voltage	-0.5 V to $V_{CC} + 0.5$ V
Storage temperature	-65°C to +150°C
Power dissipation	1.0 W
Latch-up trigger current, all outputs	140 mA

## OPERATING RANGES Over Temperature Range

SYMBOL	PARAMETER	FIGURE	67C4033-10		67C4033-15		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		4.5	5.5	4.5	5.5	V
$T_A$	Operating free-air temperature		0	70	0	70	°C
$f_{IN}$	Shift In rate	1		10		15	MHz
$t_{SIH}$	Shift in HIGH time	1,B	14		14		ns
$t_{SIL}$	Shift in LOW time	1	25		25		ns
$t_{IDS}$	Input data setup to SI (Shift In)	1	0		0		ns
$t_{IDH}$	Input data hold time from SI (Shift In)	1	40		40		ns
$t_{RIDS}$	Input data setup to IR (Input Ready)	3	0		0		ns
$t_{RIDH}$	Input data hold time from IR (Input Ready)	3	30		30		ns
$f_{OUT}$	Shift Out rate	4		10		15	MHz
$t_{SOH}$	Shift Out HIGH time	4,B	24		21		ns
$t_{SOL}$	Shift Out LOW time	4	25		25		ns
$t_{MRW}^*$	Master Reset pulse	8	35		35		ns
$t_{MRS}$	Master Reset to SI	8	65		65		ns

\* See AC test and high-speed application note.

## DC CHARACTERISTICS Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION	67C4033-10		67C4033-15		UNIT
			MIN	MAX	MIN	MAX	
$V_{IL}^*$	Low-level input voltage			0.8		0.8	V
$V_{IH}^*$	High-level input voltage		2		2		V
$I_{IN}$	Input current	$V_{CC} = \text{MAX}$ GND < $V_{IN}$ < $V_{CC}$	-1	1	-1	1	$\mu\text{A}$
$I_{OZ}$	Off-state output current	$V_{CC} = \text{MAX}$ GND < $V_{OUT}$ < $V_{CC}$	-5	5	-5	5	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 20 \mu\text{A}$	0.1		0.1	V
			$I_{OL} = 8 \text{ mA}$	0.4		0.4	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -20 \mu\text{A}$	$V_{CC} - 0.1$		$V_{CC} - 0.1$	V
			$I_{OH} = -4 \text{ mA}$	2.4		2.4	
$I_{OS}^{**}$	Output short-circuit current	$V_{CC} = \text{MAX}$ $V_O = 0 \text{ V}$	-90	-20	-90	-20	mA
$I_{CC}$	Standby supply current	$V_{CC} = \text{MAX}$ $I_{OUT} = 0$	$V_{IH} = V_{CC}$ $V_{IL} = \text{GND}$	100		100	$\mu\text{A}$
	Operating supply current		$V_{IH} = \text{MIN}$ , $V_{IL} = \text{MAX}$ $f_{IN} = f_{OUT} = \text{MAX}$	35		45	mA

\* These are absolute voltages with respect to GND (Pin 10) and include all overshoots due to system and/or tester noise.

\*\* Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

## SWITCHING CHARACTERISTICS Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67C4033-10		67C4033-15		UNIT
			MIN	MAX	MIN	MAX	
t <sub>IRL</sub> *	Shift In ↑ to Input Ready LOW	1		60		55	ns
t <sub>IRH</sub> *	Shift In ↓ to Input Ready HIGH			50		50	ns
t <sub>ORL</sub> *	Shift Out ↑ to Output Ready LOW	4		55		45	ns
t <sub>ORH</sub> *	Shift Out ↓ to Output Ready HIGH			50		41	ns
t <sub>ODH</sub>	Output Data Hold (previous word)		5		5		ns
t <sub>ODS</sub>	Output Data Shift (next word)			35		30	ns
t <sub>PT</sub>	Data throughput	3,6		100		90	ns
t <sub>MRORL</sub>	Master Reset ↓ to Output Ready LOW	8		100		100	ns
t <sub>MRIRH</sub>	Master Reset ↓ to Input Ready HIGH			100		100	ns
t <sub>MRO</sub>	Master Reset ↓ to Outputs LOW			35		35	ns
t <sub>MRHFL</sub>	Master Reset ↓ to Half-Full Flag LOW	9		100		100	ns
t <sub>MRAEH</sub>	Master Reset ↓ to Almost Empty Flag HIGH			100		100	ns
t <sub>IPH</sub>	Input ready pulse HIGH	3,B	19		16		ns
t <sub>OPH</sub>	Output ready pulse HIGH	6,B	14		14		ns
t <sub>ORD</sub>	Output ready ↑ to Data Valid	4		-3		-3	ns
t <sub>AEH</sub>	Shift Out ↑ to AF/E HIGH	10		110		110	ns
t <sub>AEL</sub>	Shift In ↑ to AF/E LOW			110		110	ns
t <sub>AFL</sub>	Shift Out ↑ to AF/E LOW	11		110		110	ns
t <sub>AFH</sub>	Shift In ↑ to AF/E HIGH			110		110	ns
t <sub>HFH</sub>	Shift In ↑ to HF HIGH	12		110		110	ns
t <sub>HFL</sub>	Shift Out ↑ to HF LOW			110		110	ns
t <sub>PHZ</sub>	Output Disable Delay	A		25		25	ns
t <sub>PLZ</sub>				25		25	
t <sub>PZL</sub>	Output Enable Delay			30		30	ns
t <sub>PZH</sub>				30		30	

\* See timing diagram for explanation of parameters.

## CAPACITANCES\*

SYMBOL	PARAMETER	TEST CONDITION	67C4033-XX		UNIT
			MIN	MAX	
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25°C, f = 1 MHz V <sub>CC</sub> = 4.5 V		10	pF
C <sub>OUT</sub>	Output capacitance			7	pF

\* Values not tested in production.

2

## THREE-STATE TEST LOAD

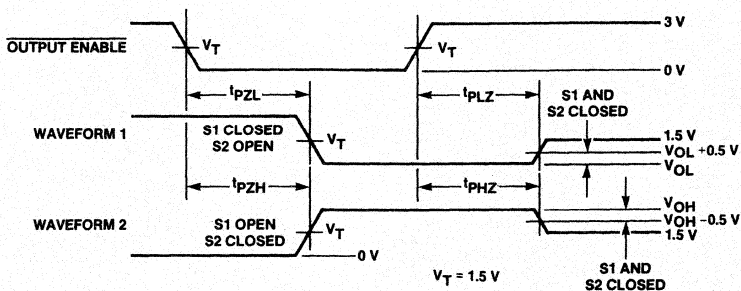
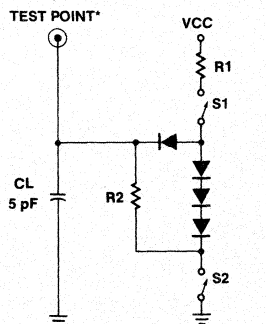
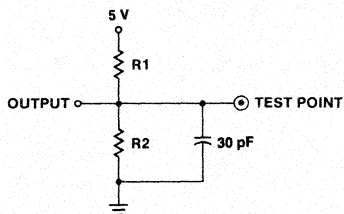


Figure A. Enable and Disable

Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

## STANDARD A.C. TEST LOAD



Input Pulse Amplitude = 3 V  
 Input Rise and Fall Time (10%-90%) = 2.5 ns  
 Measurements made at 1.5 V  
 All Diodes are 1N916 or 1N3064

## RESISTOR VALUES

$I_{OL}$	R1	R2
8 mA	600 $\Omega$	1200 $\Omega$

## FUNCTIONAL DESCRIPTION

### Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the  $D_x$  inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

### Data Output

Data is read from the  $O_x$  outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and  $O_x$  remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

## AC TEST AND HIGH-SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1  $\mu$ F directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time ( $T_{IDH}$ ) and the next activity of Input Ready ( $T_{IRL}$ ) to be extended relative to Shift-In going HIGH. This same type of problem is also related to  $T_{IRH}$ ,  $T_{ORL}$ ,  $T_{ORH}$ , and the Status Flag timing as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.



## HF AND AFE STATUS FLAGS

The Half-Full (HF) will be high only when the net balance of words shifted into the FIFO exceeds the number of words shifted out by thirty-two or more (i.e., when the FIFO contains thirty-two or more words). The Almost-Full/Empty (AFE) flag will be HIGH when the FIFO contains fifty-six or more words or when the FIFO contains eight or fewer words (see Figures 9, 10, and 11).

Care should be exercised in using the status flags because they are capable of producing arbitrarily short pulses. For example, if

the FIFO contains thirty-one words, and SI and SO pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of SI and SO.

The flags will always settle to the correct state after the appropriate delay (e.g.,  $T_{HFL}$ ,  $T_{HFH}$  in this example). This property of the status flags will clearly be a function of the dynamic relation between SI and SO. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

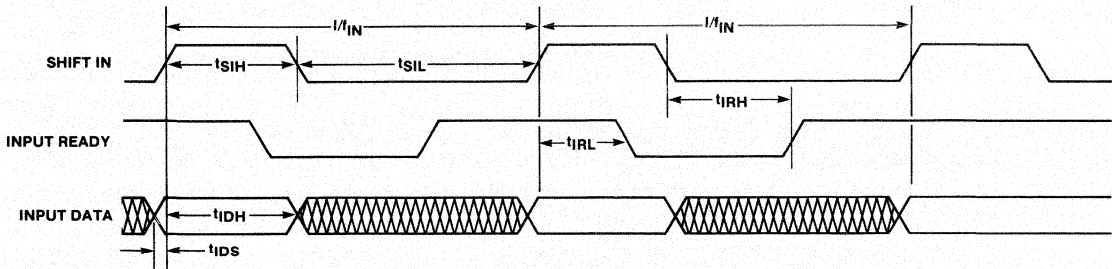


Figure 1. Input Timing

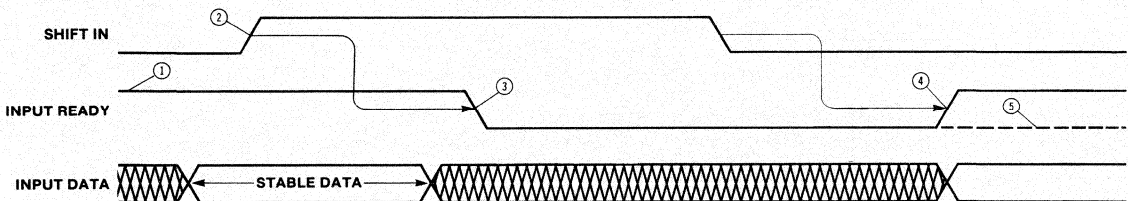
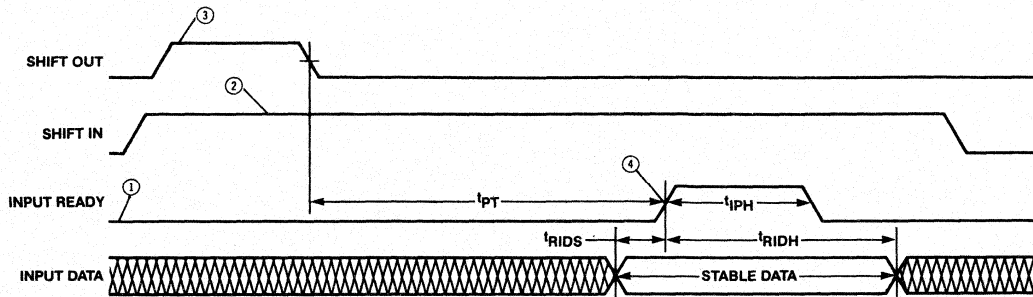


Figure 2. The Mechanism of Shifting Data into the FIFO

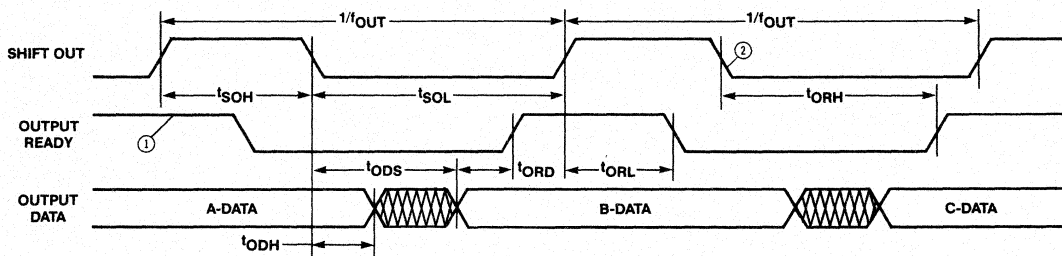
- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- ② Input Data is loaded into the first available memory location.
- ③ Input Ready goes LOW indicating this memory location is full.
- ④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
- ⑤ If the FIFO is already full then the Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored.



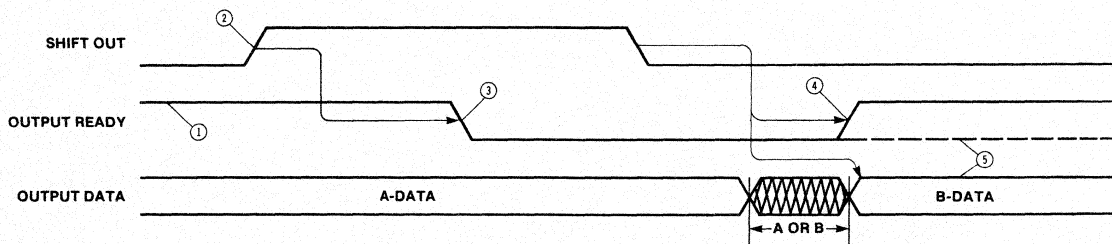
**Figure 3. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH**

- ① FIFO is initially full.
- ② Shift In is held HIGH.
- ③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
- ④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.



**Figure 4. Output Timing**

- ① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
- ② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.



**Figure 5. The Mechanism of Shifting Data Out of the FIFO**

- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
- ③ Output Ready goes LOW.
- ④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- ⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

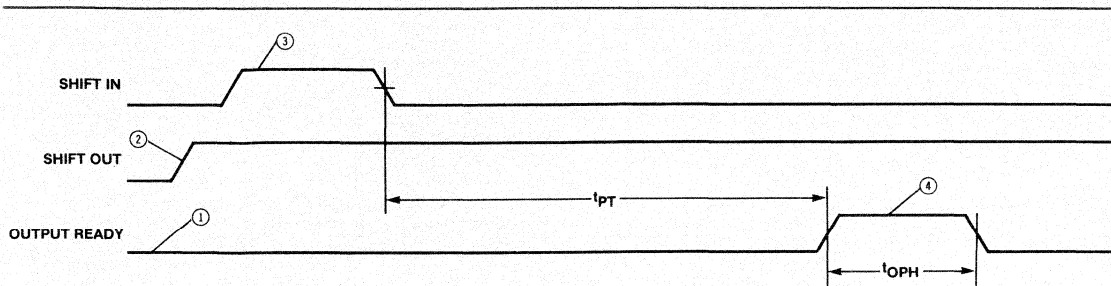


Figure 6.  $t_{PT}$  and  $t_{OPH}$  Specification

- ① FIFO is initially empty.
- ② Shift-Out is held HIGH.
- ③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In
- ④ As soon as Output Ready becomes HIGH, the word is shifted out.

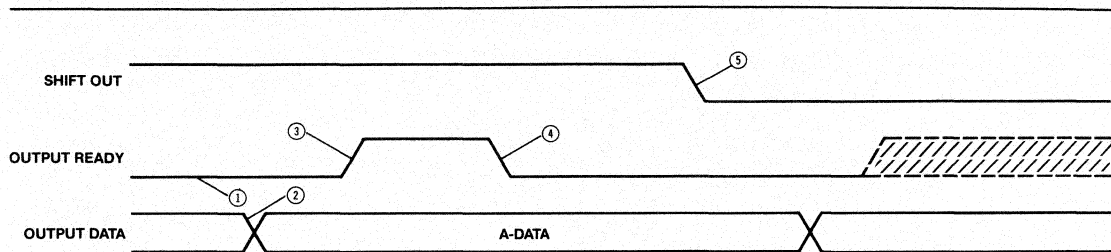


Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

- ① The internal logic does not detect the presence of any data in the FIFO.
- ② New data (A) arrives at the outputs.
- ③ Output Ready goes HIGH indicating arrival of the new data.
- ④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- ⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or remain LOW depending on whether there are any additional upstream words in the FIFO.

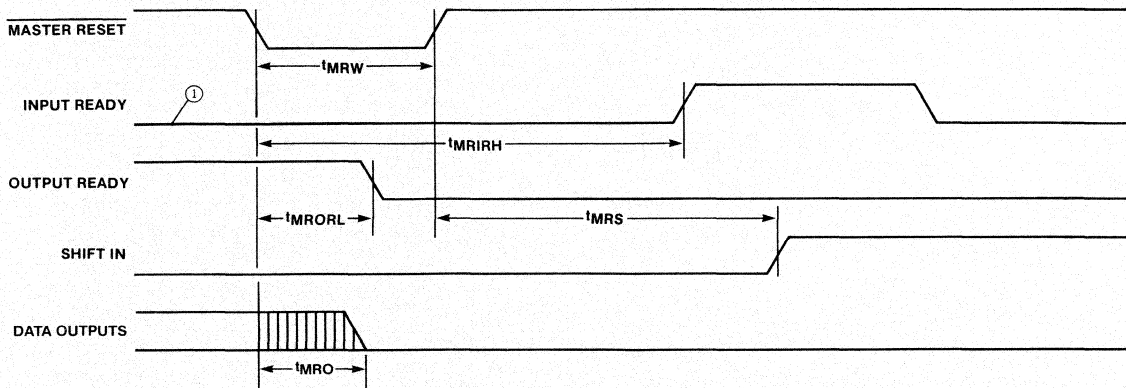


Figure 8. Master Reset Timing

- ① FIFO is initially full.

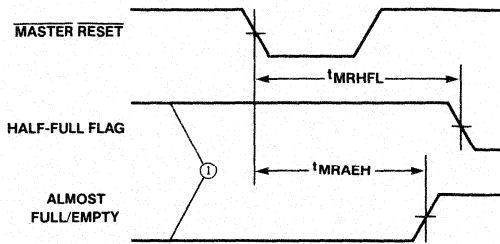


Figure 9.  $t_{MRHFL}$ ,  $t_{MRAEH}$  Specifications

① FIFO initially has between 32 and 56 words.

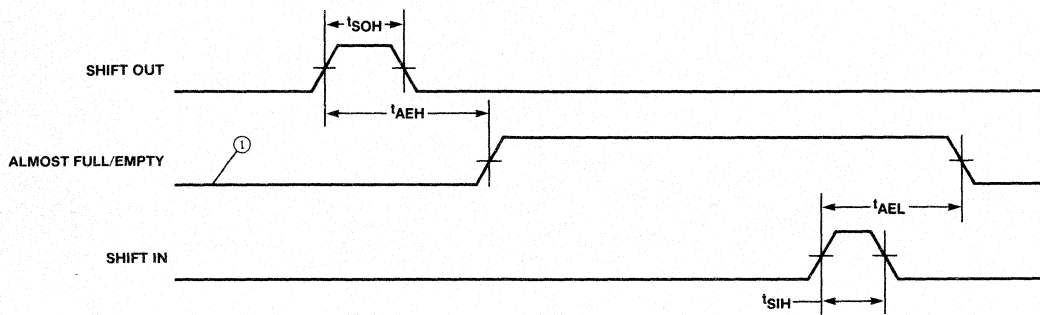


Figure 10.  $t_{AEH}$ ,  $t_{AEL}$  Specifications

① FIFO contains 9 words (one more than almost empty).

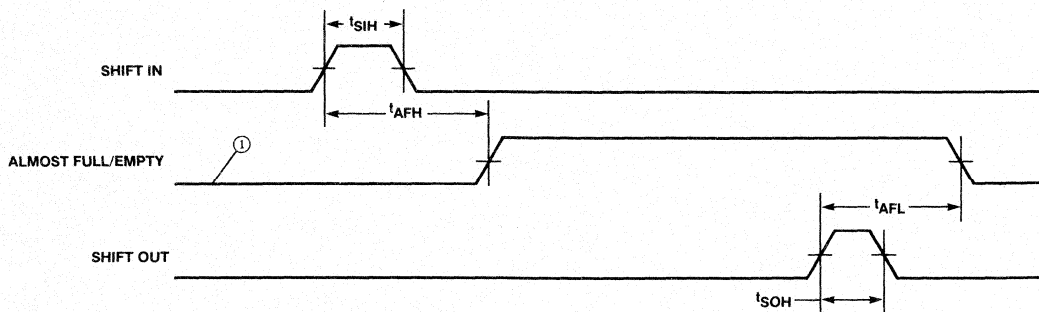


Figure 11.  $t_{AFH}$ ,  $t_{AFL}$  Specifications

① FIFO contains 55 words (one short of almost full).

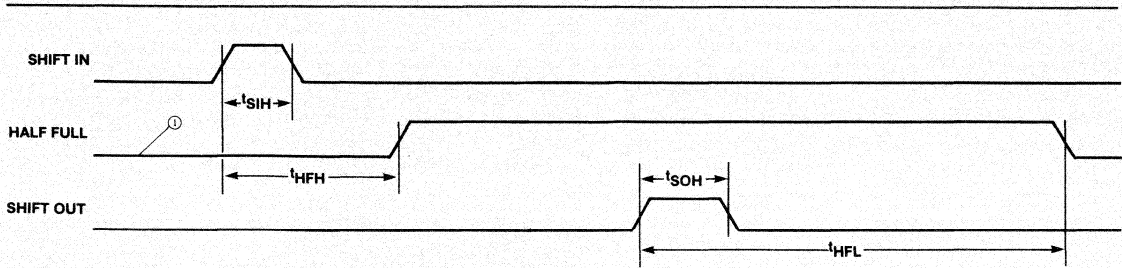
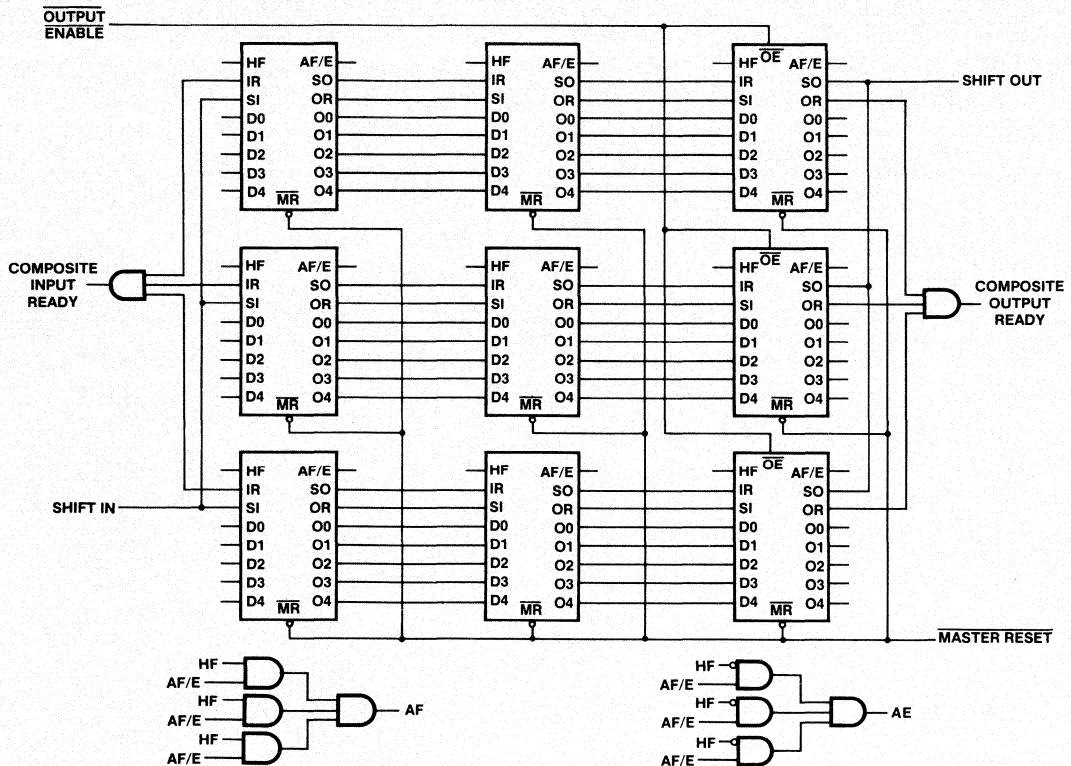


Figure 12.  $t_{HFL}$ ,  $t_{HFH}$  Specifications

① FIFO contains 31 words (one short of half full).



Almost Full (AF) is eight words or less to FIFO full.  
 Almost Empty (AE) is eight words or less to FIFO empty

Figure 13. 192x15 FIFO

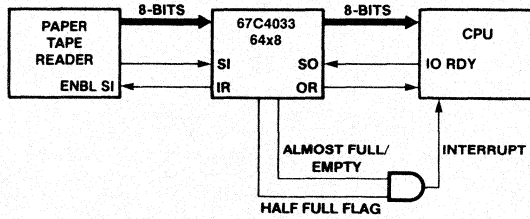
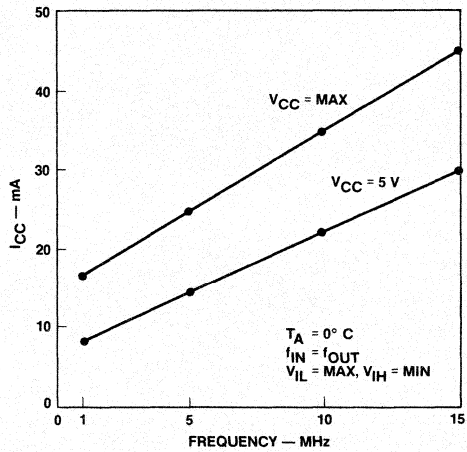


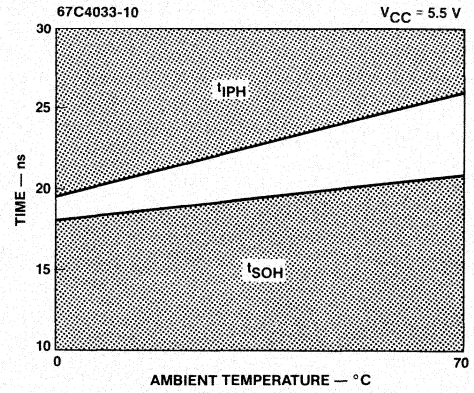
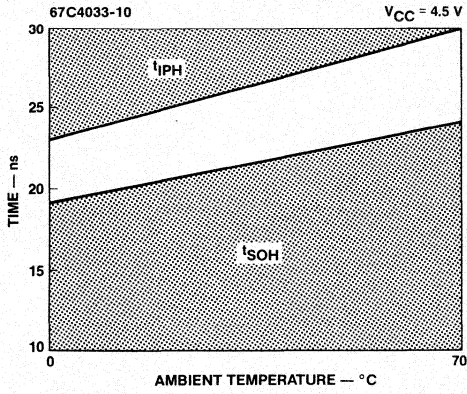
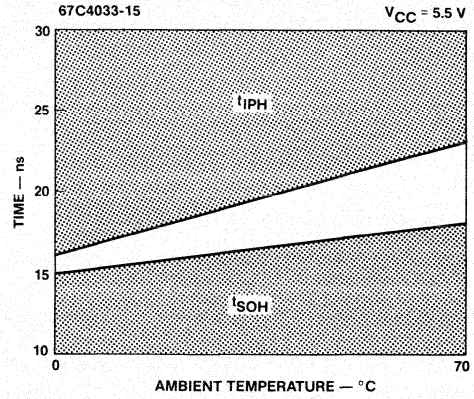
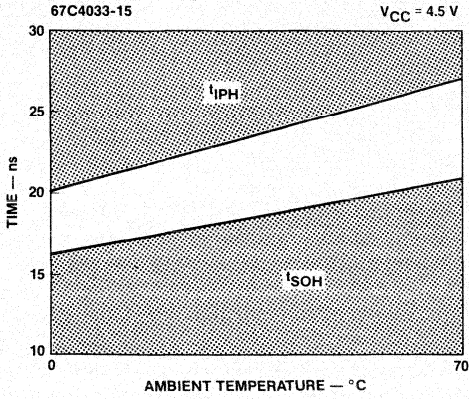
Figure 14. Application for 67C4033 "Slow and Steady Rate to Fast 'Blocked Rate' "

Note: Expanding the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

## $I_{CC}$ VS. FREQUENCY



Guaranteed Distribution of  $t_{1PH}$ ,  $t_{1SOH}$  vs. Temperature (For Cascadability Only)



Guaranteed Distribution of  $t_{0PH}$ ,  $t_{0SIH}$  vs. Temperature (For Cascadability Only)

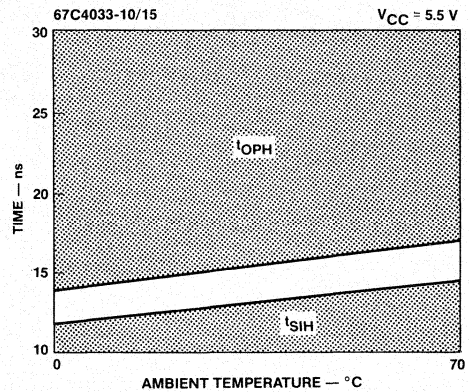
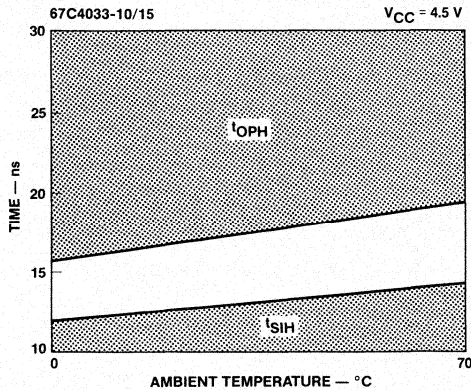


Figure B. Cascadability



# 67C413

First-in First-out (FIFO) 40 MHz 64x5 CMOS Memory

## DISTINCTIVE CHARACTERISTICS

- Zero standby power
- High-speed 40-MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width
- Half-Full and Almost-Full/Empty status flags
- RAM-based architecture for short fall-through delay
- Full CMOS transistor cell for maximum noise immunity
- Asynchronous operation
- Output enable

## GENERAL DESCRIPTION

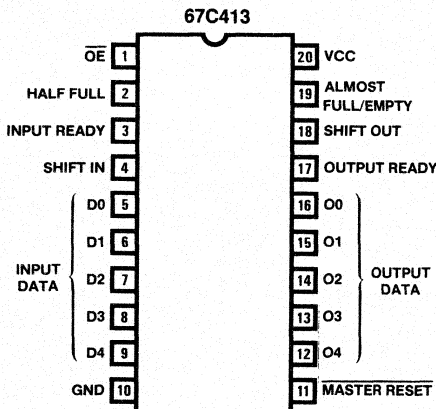
The 67C413 device is a high-performance CMOS RAM-based First-In First-Out (FIFO) buffer product organized as 64 words by 5 bits wide. This device uses Advanced Micro Devices' CMOS process technology and meets the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disk controllers, graphics, and communication

network systems. The 550- $\mu$ watt standby power specification of this device makes it ideal for ultra-low-power and battery-powered systems.

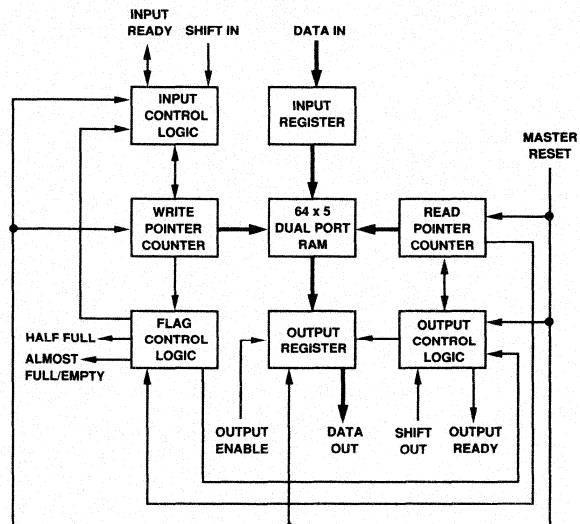
## ORDERING INFORMATION

Part Number	Package	Temp	Description
67C413-40	CD 020, PD 020, PL 020	Com	40 MHz in/out

## CONNECTION DIAGRAM



## BLOCK DIAGRAM





## FUNCTIONAL DESCRIPTION

### Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the  $D_x$  inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

### Data Output

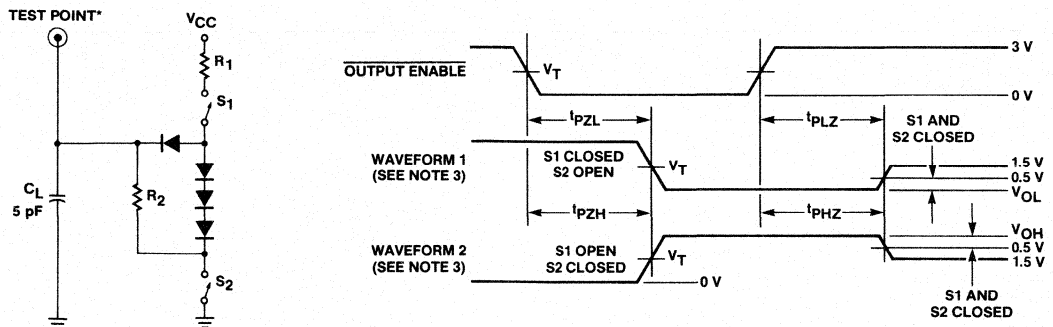
Data is read from the  $O_x$  outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and  $O_x$  remains as before (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

## OPERATING CONDITIONS Over temperature range

Symbol	Parameter	Figure	67C413-10		67C413-15		Unit
			Min.	Max.	Min.	Max.	
$V_{CC}$	Supply Voltage		4.5	5.5	4.5	5.5	V
$T_A$	Operating Free-Air Temperature		0	70	0	70	°C
$f_{IN}$	Shift In Rate	1		10		15	MHz
$t_{SHI}^\dagger$	Shift in HIGH Time	1,B	14		14		ns
$t_{SIL}$	Shift in LOW Time	1	25		25		ns
$t_{IDS}$	Input Data Setup to SI (Shift In)	1	0		0		ns
$t_{IDH}$	Input Data Hold Time from SI (Shift In)	1	40		40		ns
$t_{RIDS}$	Input Data Setup to IR (Input Ready)	3	0		0		ns
$t_{RIDH}$	Input Data Hold Time from IR (Input Ready)	3	30		30		ns
$f_{OUT}$	Shift Out Rate	4		10		15	MHz
$t_{SOH}$	Shift Out HIGH Time	4,B	24		21		ns
$t_{SOL}$	Shift Out LOW Time	4	25		25		ns
$t_{MWR}^*$	Master Reset Pulse	8	35		35		ns
$t_{MRS}$	Master Reset to SI	8	65		65		ns

\* See AC test and high-speed application note.

## THREE-STATE TEST LOAD



## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to + 7.0 V
Input voltage .....	-1.5 V to 7.0 V
Off-state output voltage .....	-0.5 V to $V_{CC}$ +0.5 V
Storage temperature .....	-65°C to + 150°C
Power dissipation .....	1.0 W
Latch-up trigger current, all options .....	140 mA

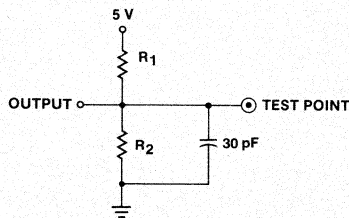
## ELECTRICAL CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Test Condition	67C413-10		67C413-15		Unit
			Min.	Max.	Min.	Max.	
$V_{IL}^*$	Low-level Input Voltage			0.8		0.8	V
$V_{IH}$	High-level Input Voltage		2		2		V
$I_{IN}$	Input Current	$V_{CC} = \text{MAX}$ $\text{GND} < V_{IN} < V_{CC}$	-1	1	-1	1	$\mu\text{A}$
$I_{OZ}$	Off-State Output Current	$V_{CC} = \text{MAX}$ $\text{GND} < V_{OUT} < V_{CC}$	-5	5	-5	5	$\mu\text{A}$
$V_{OL}$	Low-Level Output Voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 20 \mu\text{A}$			0.1	V
			$I_{OL} = 8 \text{ mA}$		0.4	0.4	
$V_{OH}$	High-Level Output Voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -20 \mu\text{A}$	$V_{CC} - 0.1$	$V_{CC} - 0.1$		V
			$I_{OH} = -4 \text{ mA}$	2.4	2.4		
$I_{OS}^{**}$	Output Short-Circuit Current	$V_{CC} = \text{MAX}$ $V_O = 0 \text{ V}$	-90	-20	-90	-20	mA
$I_{CC}$	Standby Supply Current			100		100	$\mu\text{A}$
	Operating Supply Current		$V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$ $f_{IN} = f_{OUT} = \text{MAX}$	35		45	mA

\* These are absolute voltages with respect to GND (Pin 10) and include all overshoots due to system or tester noise.

\*\* No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

## STANDARD A.C. TEST LOAD



## RESISTOR VALUES

$I_{OL}$	R1	R2
8 mA	600 $\Omega$	1200 $\Omega$

## AC TEST AND HIGH-SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Advanced Micro Devices recommends a monolithic ceramic capacitor of 0.1  $\mu\text{F}$  directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements

may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time ( $T_{IDH}$ ) and the next activity of Input Ready ( $T_{IRL}$ ) to be extended relative to Shift-In going HIGH. This same type of problem is also related to  $T_{IRH}$ ,  $T_{ORL}$ ,  $T_{ORH}$ , and the Status Flag timing as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.

# 67401 67401A 67402 67402A

First-In First-Out (FIFO)  
64x4 64x5 Standalone Memory



Advanced  
Micro  
Devices

## DISTINCTIVE CHARACTERISTICS

- Choice of 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in word dimension only
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation

## ORDERING INFORMATION

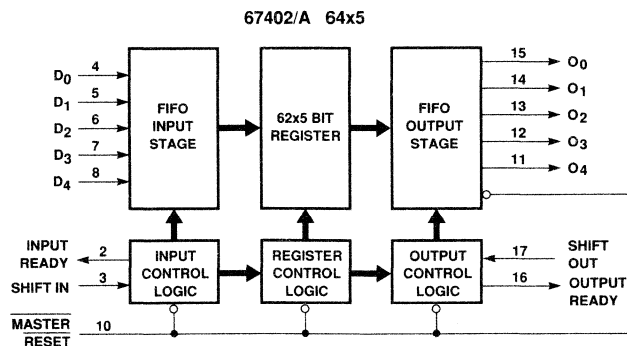
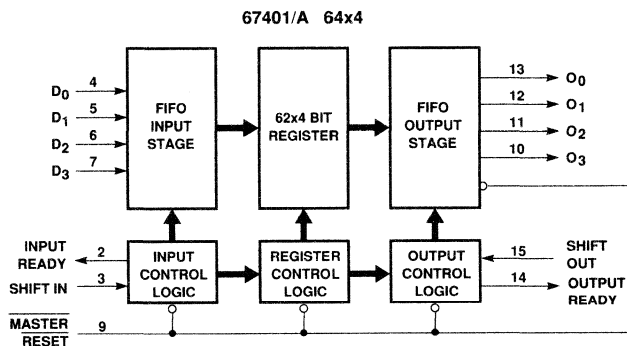
Part Number	Package	Temp	Description
67401	CD 016,PD 016,PL 020	Com	10 MHz 64x4 FIFO
67402	CD 018,PD 018,PL 020	Com	10 MHz 64x5 FIFO
67401A	CD 016,PD 016,PL 020	Com	15 MHz 64x4 FIFO
67402A	CD 018,PD 018,PL 020	Com	15MHz 64x5 FIFO

## GENERAL DESCRIPTION

The 67401/1A/2/2A are "fall-through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits respectively. A 15 MHz data rate

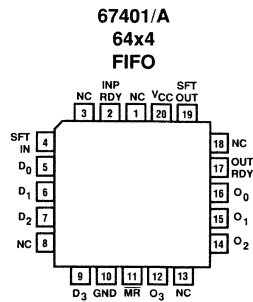
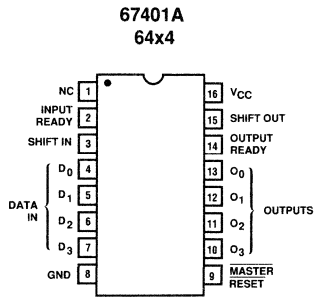
allows usage in high speed tape or disc controllers and communication buffer applications. Word length is expandable; FIFO depth is not expandable.

## BLOCK DIAGRAMS

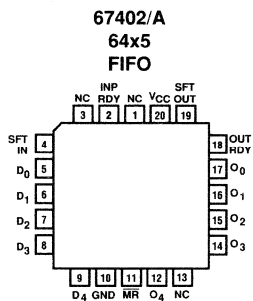
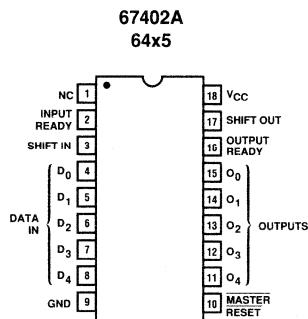


**2**

## CONNECTION DIAGRAMS

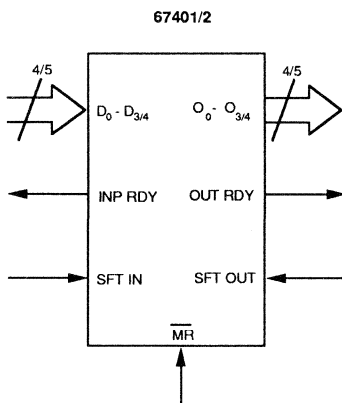


Plastic Chip Carrier



Plastic Chip Carrier

## LOGIC SYMBOL



10676-001A

## PIN DESCRIPTION

- $D_0 - D_{3/4}$  = Data Input
- $O_0 - O_{3/4}$  = Data Output
- INP RDY = Input Ready
- OUT RDY = Output Ready
- SFT IN = Shift In
- SFT OUT = Shift Out
- $\overline{\text{MR}}$  = Master Reset
- $V_{CC}$  = 5 V Power Supply
- GND = Ground

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-1.5 V to +7.0 V
Input voltage .....	-1.5 V to +7.0 V
Off-state output voltage .....	-0.5 V to +5.5 V
Storage temperature .....	-65°C to +150°C

## OPERATING CONDITIONS

Symbol	Parameter	Figure	67401A/2A			67401/2			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	Supply Voltage		4.75	5	5.25	4.75	5	5.25	V
$T_A$	Operating Free-Air Temperature		0		75	0		75	°C
$t_{SIH}^\dagger$	Shift-In HIGH Time	1	23		28†	35			ns
$t_{SIL}$	Shift-In LOW Time	1	25			35			ns
$t_{IDS}$	Input Data Setup	1	5			5			ns
$t_{IDH}$	Input Data Hold Time	1	40			45			ns
$t_{SOH}^\dagger$	Shift-Out HIGH Time	5	23			35			ns
$t_{SOL}$	Shift-Out LOW Time	5	25			35			ns
$t_{MRW}$	Master Reset Pulse	10	35			35			ns
$t_{MRS}$	Master Reset to SI	10	35			35			ns

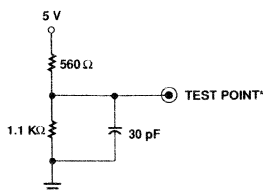
## SWITCHING CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Figure	67401A/2A			67401/2			Unit
			Min	Typ	Max	Min	Typ	Max	
$f_{IN}$	Shift-In Rate	1	15			10			MHz
$t_{IRL}^\dagger$	Shift In to Input Ready LOW	1			40			45	ns
$t_{IRH}^\dagger$	Shift In to Input Ready HIGH	1			40			45	ns
$f_{OUT}^\dagger$	Shift-Out Rate	5	15			10			MHz
$t_{ORL}^\dagger$	Shift Out to Output Ready LOW	5			45			55	ns
$t_{ORH}^\dagger$	Shift Out to Output Ready HIGH	5			50			60	ns
$t_{ODH}$	Output Data Hold (previous word)	5	10			10			ns
$t_{ODS}$	Output Data Shift (next word)	5			45			55	ns
$t_{PT}$	Data Throughput or "Fall Through"	4, 8			1.6			3	μs
$t_{MRORL}$	Master Reset to OR LOW	10			60			60	ns
$t_{MRIRH}$	Master Reset to IR HIGH	10			60			60	ns
$t_{IPH}^*$	Input Ready Pulse HIGH	4	23			23			ns
$t_{OPH}^*$	Output Ready Pulse HIGH	8	23			23			ns

† See AC test and high speed application note.

## TEST LOAD

\* The "TEST POINT" is driven by the output under test and observed by instrumentation.



Input Pulse 0 to 3 V  
 Input Rise and Fall Time (10% - 90%)  
 5 ns minimum  
 Measurements made at 1.5 V

## DC CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit		
$V_{IL}$	Low-level input voltage				0.8†	V		
$V_{IH}$	High-level input voltage				2†	V		
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{MIN}$		$I_I = -18 \text{ mA}$		-1.5	V	
$I_{IL1}$	Low-Level Input Current	$V_{CC} = \text{MAX}$		$V_I = 0.45 \text{ V}$		-0.8	mA	
$I_{IL2}$						-1.6	mA	
$I_{IH}$	High-Level Input Current	$V_{CC} = \text{MAX}$		$V_I = 2.4 \text{ V}$		50	$\mu\text{A}$	
$I_I$	Maximum Input Current	$V_{CC} = \text{MAX}$		$V_I = 5.5 \text{ V}$		1	mA	
$V_{OL}$	Low-Level Output Voltage	$V_{CC} = \text{MIN}$		$I_{OL} = 8 \text{ mA}$		0.5	V	
$V_{OH}$	High-Level Output Voltage	$V_{CC} = \text{MIN}$		$I_{OH} = -0.9 \text{ mA}$	2.4		V	
$I_{OS}$	Output Short-Circuit Current	$V_{CC} = \text{MAX}$		$V_O = 0 \text{ V}$		-20	-90	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{MAX}$ All inputs low. All outputs open.		67401		160		
				67402		180		
				67401A		170		
				67402A		190		

\* No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

† These are absolute voltages with respect to GND (PIN 8 or 9) and includes all overshoots due to system or tester noise.

## FUNCTIONAL DESCRIPTION

### Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH, the location is ready to accept data from the  $D_x$  inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

### Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front.  $t_{PT}$  defines the time required for the first data to travel from input to the output of a previously empty device.

### Data Output

Data is read from the  $O_x$  outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data

is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and  $O_x$  remains as before (i.e., data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least  $t_{PT}$ ) or completely empty (Output Ready stays LOW for at least  $t_{PT}$ ).

## AC TEST AND HIGH SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1  $\mu\text{F}$  directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time ( $t_{IDH}$ ) and the next activity of Input Ready ( $t_{IR}$ ) to be extended relative to Shift-In going High. This same type of problem is also related to  $t_{RH}$ ,  $t_{ORL}$  and  $t_{ORH}$  as related to Shift-Out.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

08125-040A

# SWITCHING WAVEFORMS

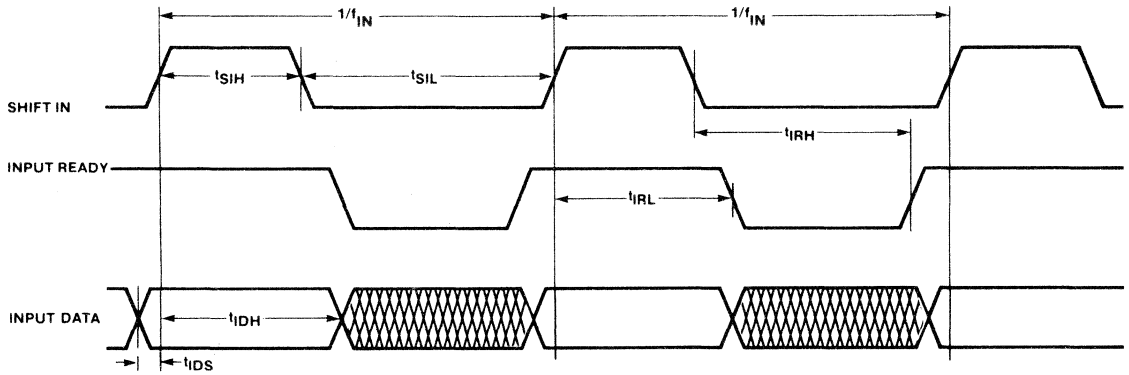


Figure 1. Input Timing

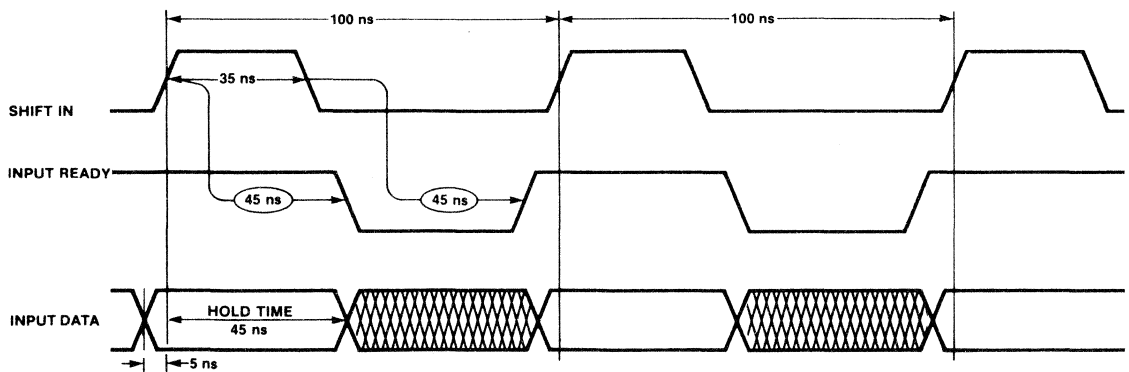
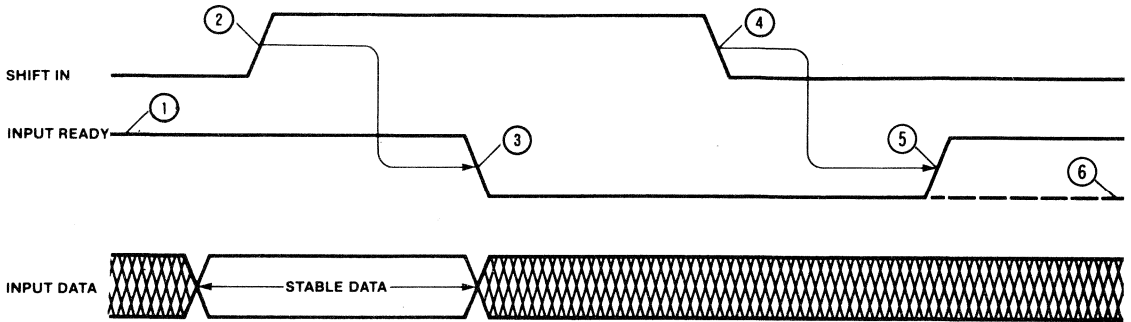


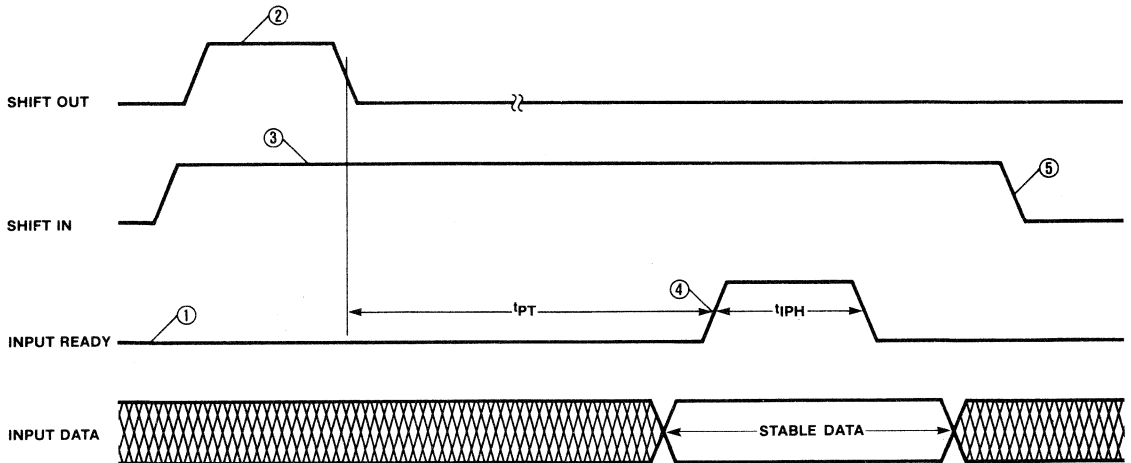
Figure 2. Typical Waveforms for 10-MHz Shift In Data Rate (67401/2)

## SWITCHING WAVEFORMS



- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
  - ② Input Data is loaded into the first word.
  - ③ Input Ready goes LOW indicating the first word is full.
  - ④ The Data from the first word is released for "fall-through" to second word.
  - ⑤ The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.
  - ⑥ If the second word is already full, then the data remains at the first word. Since the FIFO is now full, Input Ready remains low.
- NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 3).

**Figure 3. The Mechanism of Shifting Data Into the FIFO**

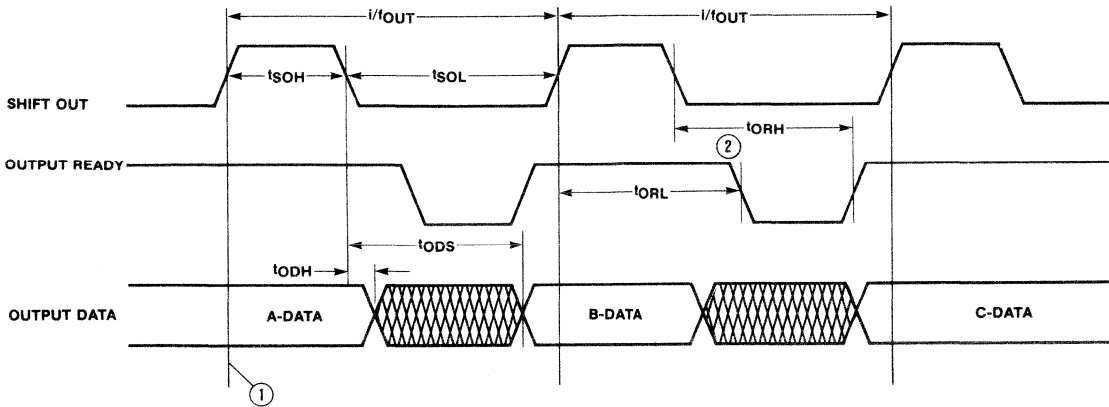


- ① FIFO is initially full.
- ② Shift Out pulse is applied. An empty location starts "bubbling" to the front.
- ③ Shift In is held HIGH.
- ④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
- ⑤ The Data from the first word is released for "fall through" to second word.

**Figure 4. Data Is Shifted In Whenever Shift In and Input Ready Are Both HIGH**



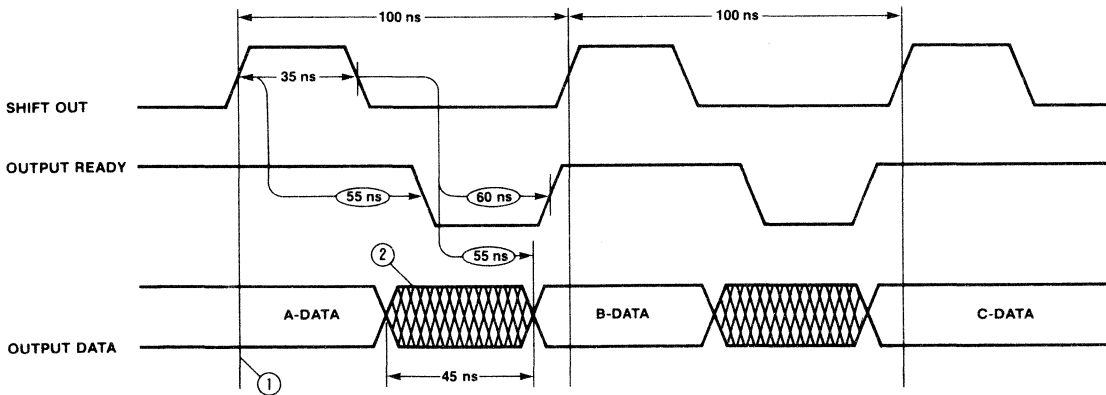
## SWITCHING WAVEFORMS



- ① The diagram assumes that at this time, words 63, 62, and 61 are loaded with A, B, and C Data, respectively.
- ② Data is shifted out when Shift Out makes a HIGH-to-LOW transition.

Figure 5. Output Timing

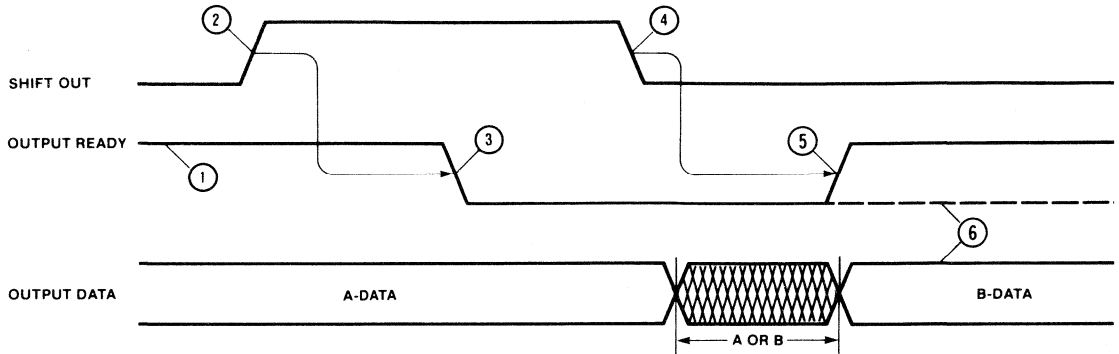
2



- ① The diagram assumes that at this time words 63, 62, and 61 are loaded with A, B, and C Data respectively.
- ② Data in the crosshatched region may be A or B Data.

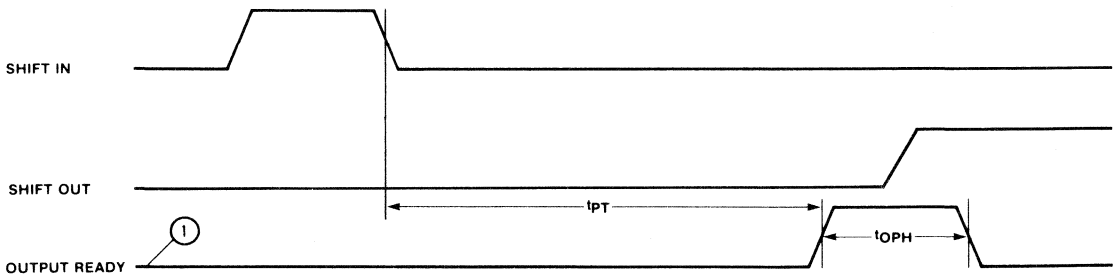
Figure 6. Typical Waveforms for 10-MHz Shift Out Data Rate (67401/2)

## SWITCHING WAVEFORMS



- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
  - ② Shift-Out goes HIGH causing the next step.
  - ③ Output Ready goes LOW.
  - ④ Contents of word 62 (B-DATA) to be released for "fall-through" to word 63.
  - ⑤ Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
  - ⑥ If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
- NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.

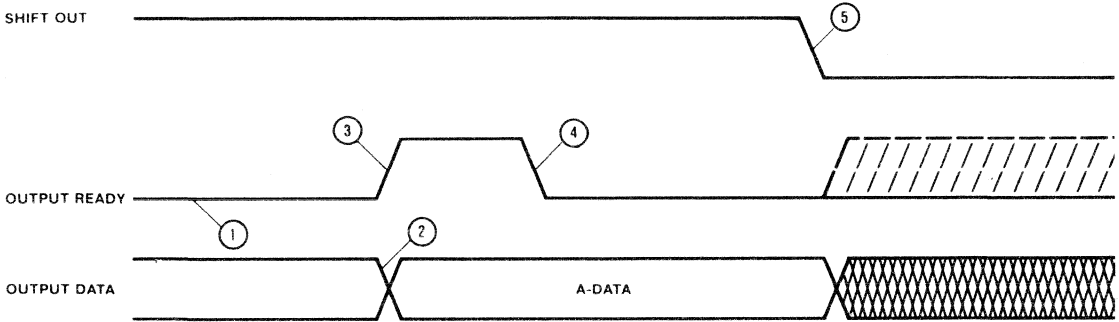
Figure 7. The Mechanism of Shifting Data Out of the FIFO



- ① FIFO is initially empty.
- ② Shift Out held HIGH.

Figure 8.  $t_{PT}$  and  $t_{OPH}$  Specification

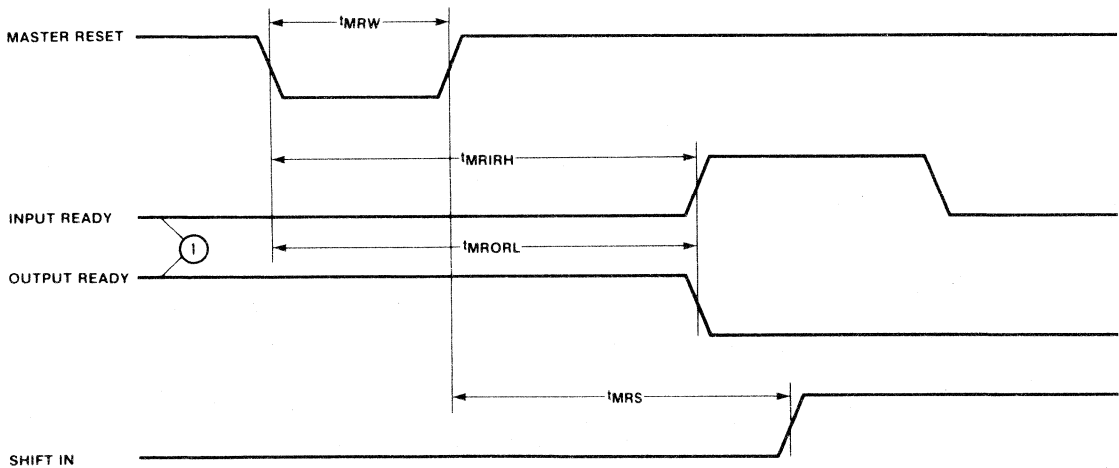
## SWITCHING WAVEFORMS



- ① Word 63 is empty.
- ② New data (A) arrives at the outputs (word 63).
- ③ Output Ready goes HIGH indicating arrival of the new data.
- ④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- ⑤ As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

**Figure 9. Data Is Shifted Out Whenever Shift Out and Output ready Are Both HIGH**

**2**



- ① FIFO is initially full.

**Figure 10. Master Reset Timing**

# C67401 C67401A C67402 C67402A

First-In First-Out (FIFO)  
64x4, 64x5 Cascadable Memory



## DISTINCTIVE CHARACTERISTICS

- Choice of 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in the word and bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation

## ORDERING INFORMATION

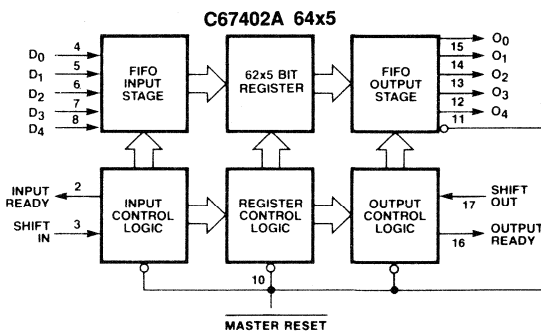
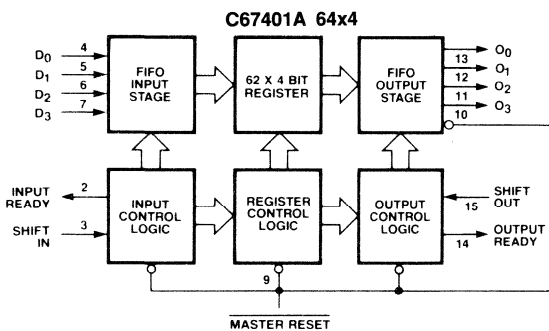
Part Number	Package	Temp	Description
C67401	CD 016,PD 016,PL 020	Com	10 MHz 64x4 FIFO
C67402	CD 018,PD 018,PL 020	Com	10 MHz 64x5 FIFO
C67401A	CD 016,PD 016,PL 020	Com	15 MHz 64x4 FIFO
C67402A	CD 018,PD 018,PL 020	Com	15MHz 64x5 FIFO

## GENERAL DESCRIPTION

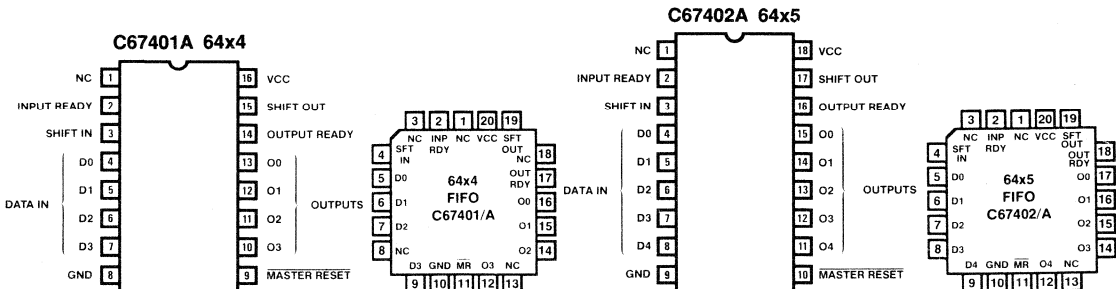
The C67401/2/1A/2A are "fall-through" high speed First-In-First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. A 15 MHz data rate allows usage in high

speed tape or disc controllers and communications buffer applications. Both word length and FIFO depth are expandable.

## BLOCK DIAGRAMS



## CONNECTION DIAGRAMS



## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to + 7.0 V
Input voltage .....	-1.5 V to + 7.0 V
Off-state output voltage .....	-0.5 V to + 5.5 V
Storage temperature .....	-65°C to + 150°C

## OPERATING CONDITIONS

Symbol	Parameter	Figure	C67401A/2A			C67401/2			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$V_{CC}$	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
$T_A$	Operating free-air temperature		0		75	0		75	°C
$t_{SIH}^\dagger$	Shift in HIGH time	1	23			23			ns
$t_{SIL}$	Shift in LOW time	1	25			35			ns
$t_{IDS}$	Input data setup	1	0			0			ns
$t_{IDH}$	Input data hold time	1	40			45			ns
$t_{SOH}^\dagger$	Shift Out HIGH time	5	23			23			ns
$t_{SOL}$	Shift Out LOW time	5	25			35			ns
$t_{MRW}$	Master Reset pulse	10	35			35			ns
$t_{MRS}$	Master Reset to SI	10	35			35			ns

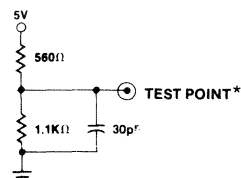
## SWITCHING CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Figure	C67401A/2A			C67401/2			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$f_{IN}$	Shift In rate	1	15			10			MHz
$t_{IRL}$	Shift In to Input Ready LOW	1			40			45	ns
$t_{IRH}$	Shift In to Input Ready HIGH	1			40			45	ns
$f_{OUT}$	Shift Out rate	5	15			10			MHz
$t_{ORL}^\dagger$	Shift Out to Output Ready LOW	5			45			55	ns
$t_{ORH}^\dagger$	Shift Out to Output Ready HIGH	5			50			60	ns
$t_{ODH}$	Output Data Hold (previous word)	5	10			10			ns
$t_{ODS}$	Output Data Shift (next word)	5			45			55	ns
$t_{PT}$	Data throughput or "fall through"	4,8			1.6			3	μs
$t_{MRORL}$	Master Reset to OR LOW	10			60			60	ns
$t_{MRIRH}$	Master Reset to IR HIGH	10			60			60	ns
$t_{IPH}$	Input Ready pulse HIGH	4	23			23			ns
$t_{OPH}^*$	Output Ready pulse HIGH	8	23			23			ns

† See AC test and High Speed application note.

\* This parameter applies to FIFOs communicating with each other in a cascaded mode.

## SWITCHING TEST CIRCUIT



\* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse 0 to 3 V  
 Input Rise and Fall Time (10% - 90%)  
 5 ns minimum  
 Measurements made at 1.5 V

## DC CHARACTERISTICS Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IL}$	Low-level input voltage						0.8†	V
$V_{IH}$	High-level input voltage				2†			V
$V_{IC}$	Input clamp voltage		$V_{CC} = \text{MIN}$	$I_I = -18\text{mA}$			-1.5	V
$I_{IL1}$	Low-level input current	$D_0-D_n, \overline{MR}$	$V_{CC} = \text{MAX}$	$V_I = 0.45\text{V}$			-0.8	mA
$I_{IL2}$		SI, SO					-1.6	mA
$I_{IH}$	High-level input current		$V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$			50	$\mu\text{A}$
$I_I$	Maximum input current		$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$			1	mA
$V_{OL}$	Low-level output voltage		$V_{CC} = \text{MIN}$	$I_{OL} = 8\text{mA}$			0.5	V
$V_{OH}$	High-level output voltage		$V_{CC} = \text{MIN}$	$I_{OH} = -0.9\text{mA}$	2.4			V
$I_{OS}$	Output short-circuit current *		$V_{CC} = \text{MAX}$	$V_O = 0\text{V}$	-20		-90	mA
$I_{CC}$	Supply current		$V_{CC} = \text{MAX}$ All inputs low. All outputs open.	C67401			160	mA
				C67402			180	
				C67401A			170	
				C6702A			190	

\*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†There are absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment

## FUNCTIONAL DESCRIPTION

### Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the  $D_x$  inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

### Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front.

$t_{PT}$  defines the time required for the first data to travel from input to the output of a previously empty device.

### Data Output

Data is read from the  $O_x$  outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and  $O_x$  remains as before, (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least  $t_{PT}$ ) or completely empty (Output Ready stays LOW for at least  $t_{PT}$ ).

## AC TEST AND HIGH-SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1  $\mu\text{F}$  directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift

In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time ( $t_{IDH}$ ) and the next activity of Input Ready ( $t_{IRL}$ ) to be extended relative to Shift-In going High. This same type of problem is also related to  $t_{IRH}$ ,  $t_{ORL}$  and  $t_{ORH}$  as related to Shift-Out.

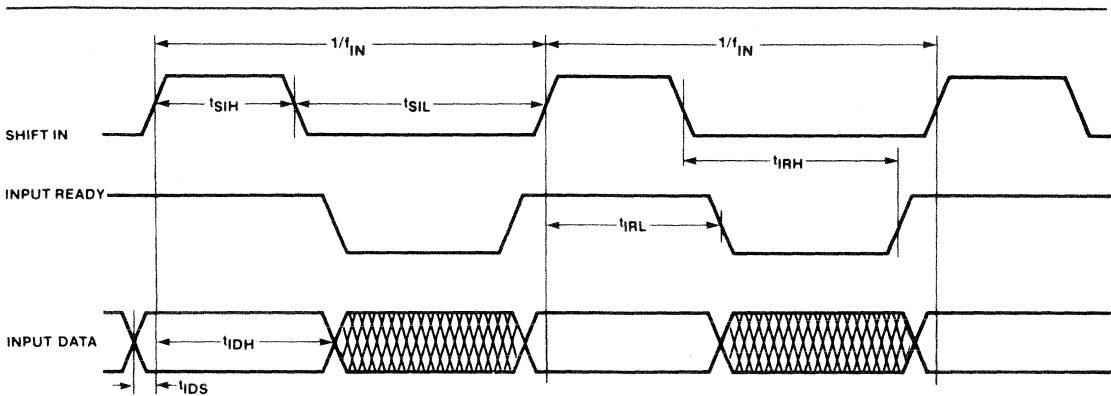


Figure 1. Input Timing

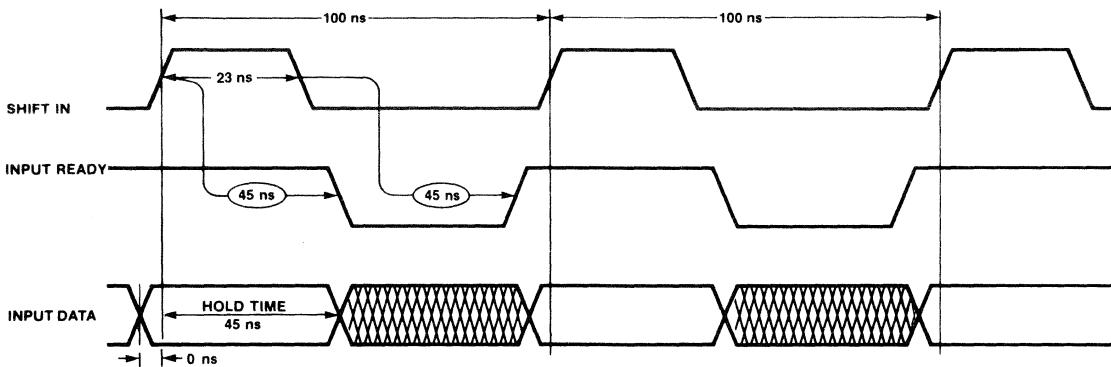


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate

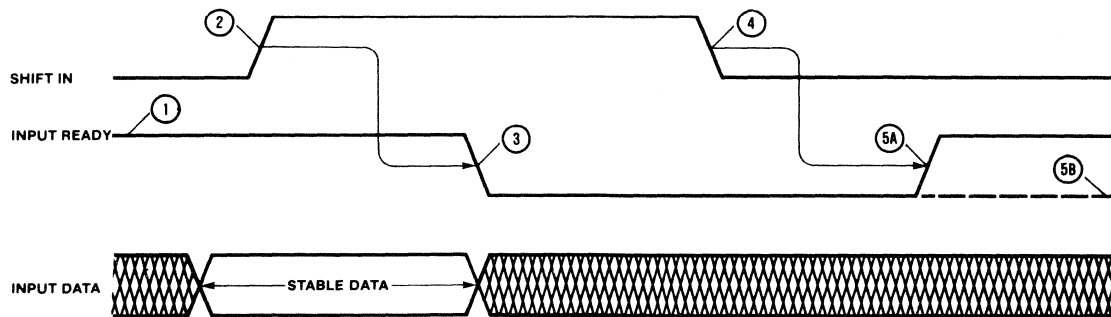


Figure 3. The Mechanism of Shifting Data into the FIFO

- ① Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
- ② Input Data is loaded into the first word.
- ③ Input Ready goes LOW indicating the first word is full.
- ④ The Data from the first word is released for "fall-through" to second word.
- ⑤A The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.
- ⑤B If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored. (See Figure 4).

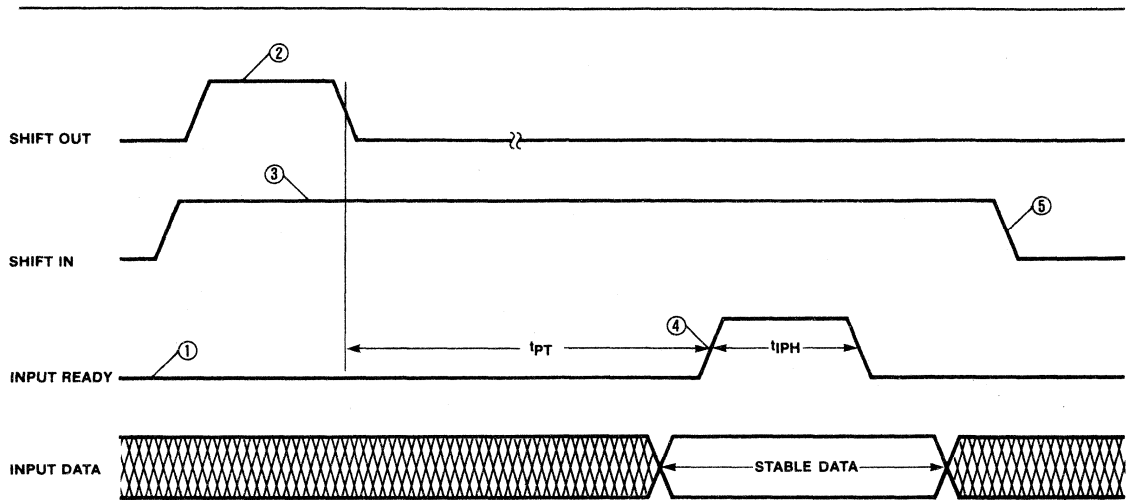
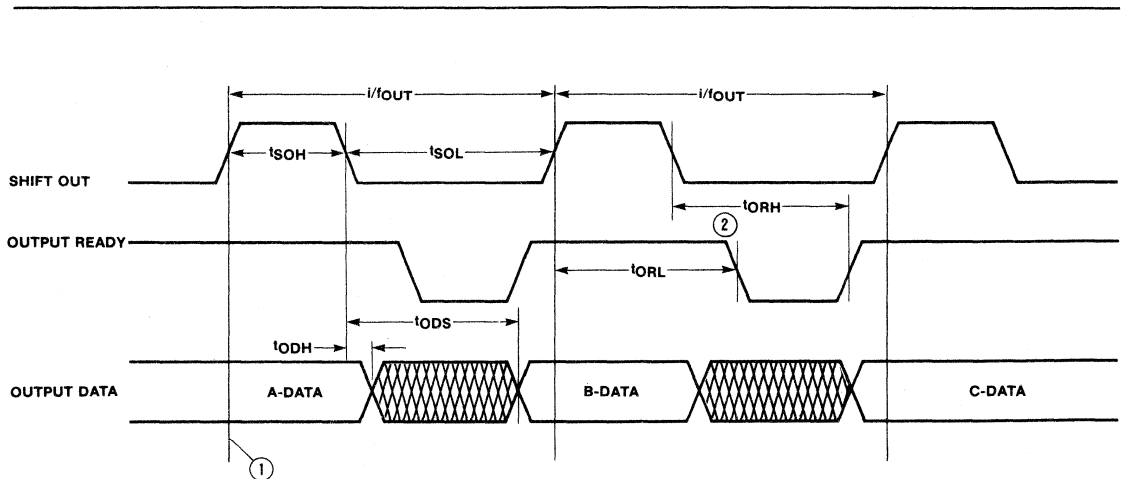


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- ① FIFO is initially full.
- ② Shift Out pulse is applied. An empty location starts "bubbling" to the front.
- ③ Shift In is held HIGH.
- ④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
- ⑤ The Data from the first word is released for "fall through" to second word.



- ① The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
- ② Data is shifted out when Shift Out makes a HIGH to LOW transition.

Figure 5. Output Timing



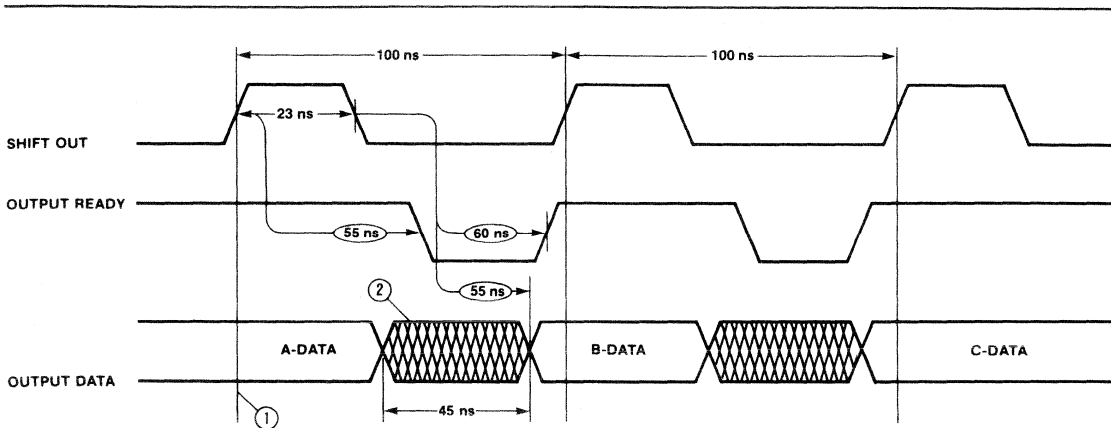


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate

- ① The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
- ② Data in the crosshatched region may be A or B Data.

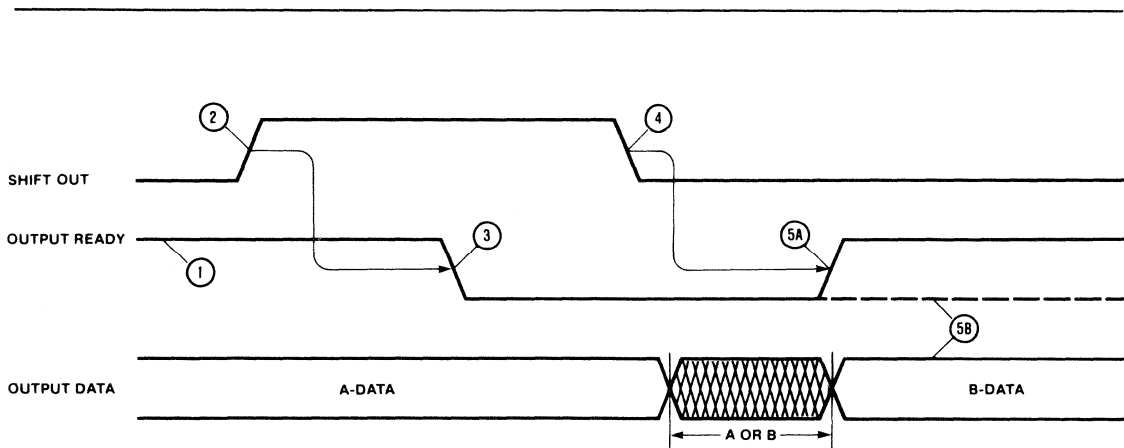
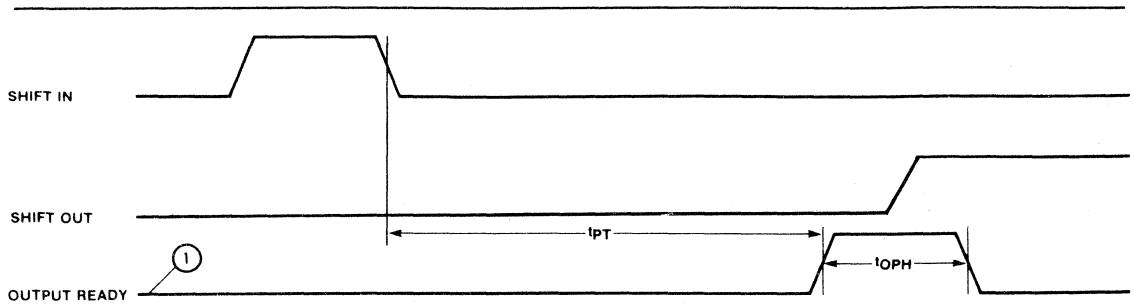


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

- ① Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
- ② Shift Out goes HIGH causing the next step.
- ③ Output Ready goes LOW.
- ④ Contents of word 62 (B-DATA) is released for "fall through" to word 63.
- ⑤A Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
- ⑤B If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.



① FIFO initially empty.

Figure 8.  $t_{PT}$  and  $t_{OPH}$  Specification

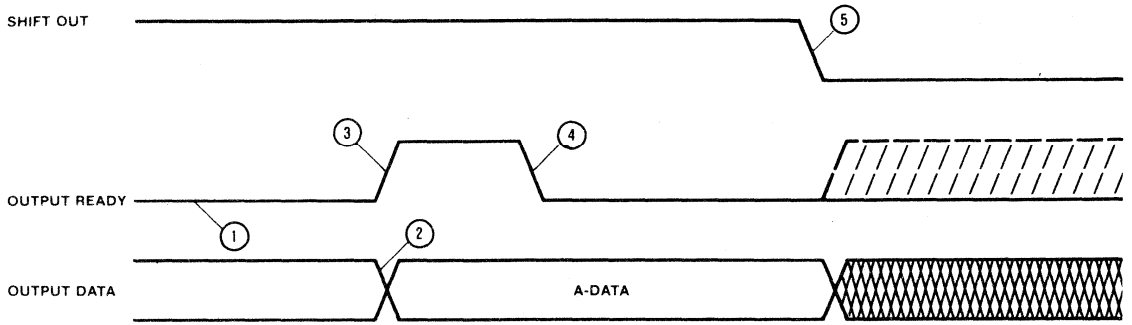


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

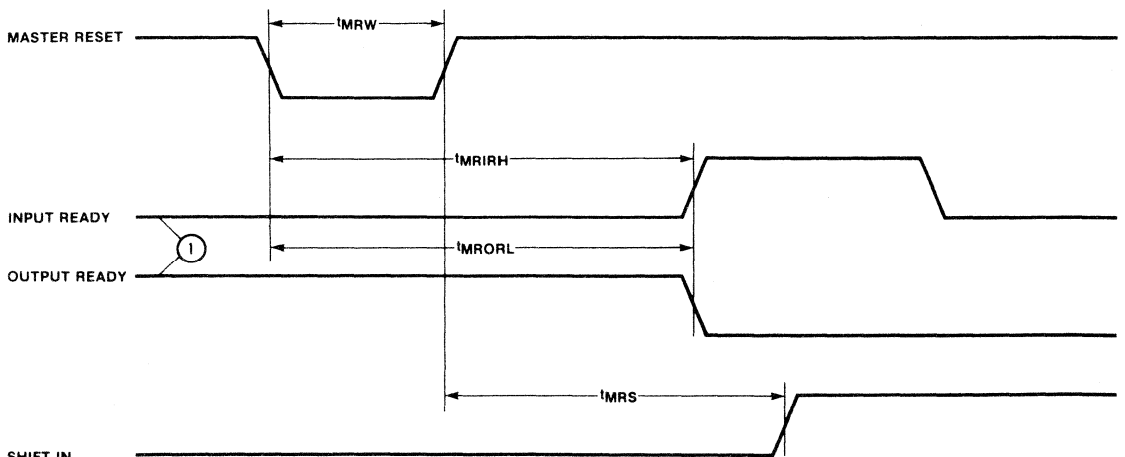
① Word 63 is empty.

② New data (A) arrives at the outputs (word 63).

③ Output Ready goes HIGH indicating the arrival of the new data.

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.

⑤ As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



① FIFO initially full.

Figure 10. Master Reset Timing

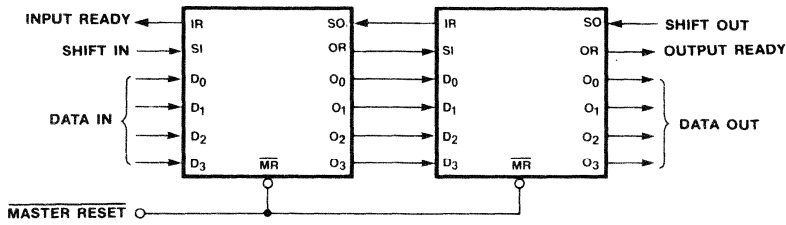


Figure 11. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

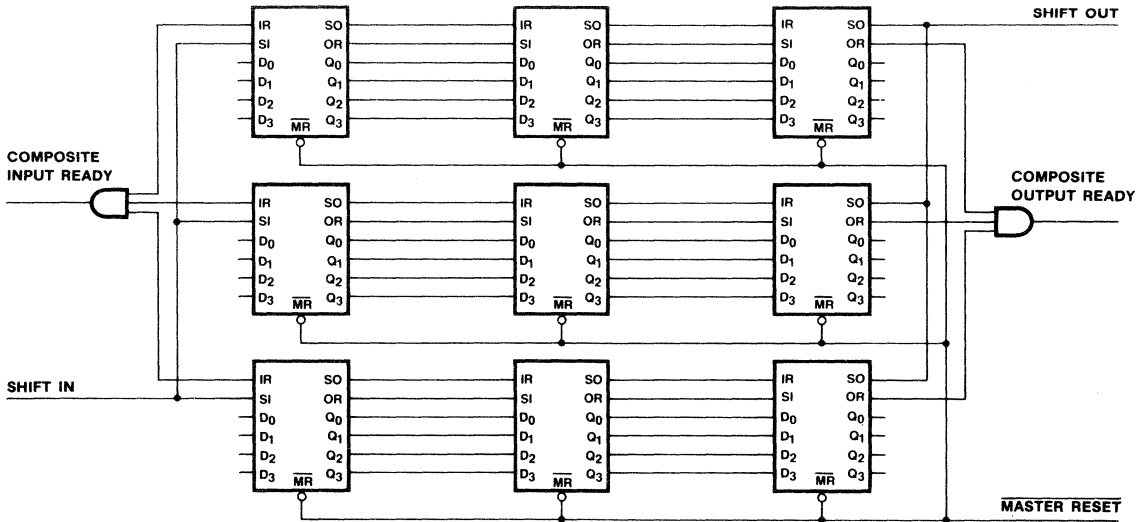
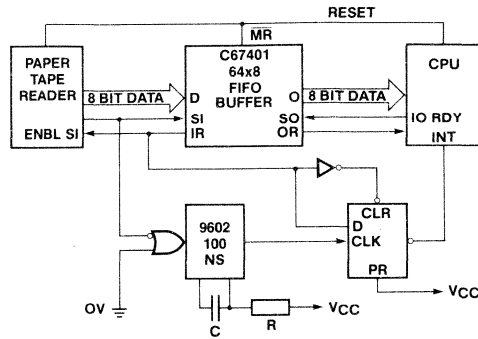


Figure 12. 192x12 FIFO with C5/C67401/1A

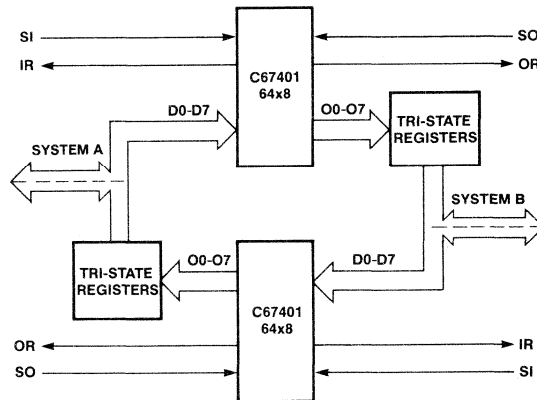
FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.

## APPLICATIONS



NOTE: The output of monostable holds off the "Buffer full" interrupt for 100ns. If 100ns after shift in, there has not been an input Ready to reset the "D Flip-flop" an interrupt is issued, as the FIFO is full. The CPU then empties the FIFO before the next character is output from the tape drive.

Figure 13. Slow Steady Rate to Fast "Blocked" Rate



NOTE: Both depth and width expansion can be used in this mode. The IR and OR signals are theanded versions of the individual IR and OR signals.

Figure 14. Bidirectional FIFO Application



# 74S225/A

Asynchronous First-In First-Out Memory (FIFO) 16 x 5

## Features/Benefits

- DC to 20-MHz shift-in/shift-out rates
- Fully expandable by word width and depth
- Three-state outputs
- TTL-compatible inputs and outputs
- Functionally compatible with T.I. SN74S225
- Designed for extended testability

## Description

The 74S225/A is a Schottky-clamped transistor-transistor logic (STTL) 16x5 First-In-First-Out memory (FIFO) which operates from DC to 10/20 MHz. The data is loaded and emptied on a

## Pin Names

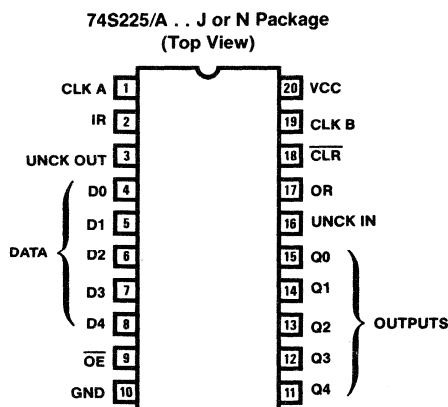
PIN #	PIN NAME	DESCRIPTION
1	CLK A	Load clock A
2	IR	Input ready
3	UNCK OUT	Unload clock output
4-8	D0-D4	Data inputs
9	$\overline{OE}$	Output enable
10	GND	Ground pin
11-15	Q4-Q0	Data outputs
16	UNCK IN	Unload clock input
17	OR	Output ready
18	$\overline{CLR}$	Clear
19	CLK B	Load clock B
20	V <sub>CC</sub>	Supply voltage

## Ordering Information

Part Number	Package	Temp	Description
74S225	CD 020, PD 020	Com	10 MHz in/out
74S225A	CD 020, PD 020	Com	20 MHz in/out

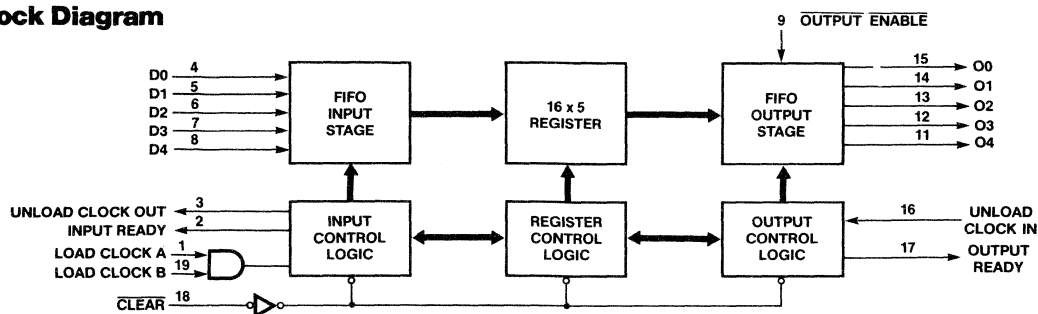
first-in-first-out basis through asynchronous input and output ports. These devices are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. Both word length and FIFO depth are expandable. Unload clock output (Pin 3) is designed for testability of V<sub>OL</sub>.

## Pin Configuration



2

## Block Diagram



## Absolute Maximum Ratings

Supply voltage $V_{CC}$ .....	-0.5 V to 7 V
Input voltage .....	-1.5 V to 7 V
Off-state output voltage .....	-0.5 V to 5.5 V
Storage temperature .....	-65 to +150°C

## Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225A			74S225			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage		4.75	5.25		4.75	5.25		V
$t_A$	Operating free-air temperature		0		75	0		75	°C
$t_{LCKH}$	LOAD CLOCK pulse width, A or B, $t_W$ (HIGH)	2	22		36	25			ns
$t_{IDS}$	Setup time, data to load clock	2	-20†*			-20†*			ns
$t_{IDH}$	Hold time, data from load clock	2	50†			70†			ns
$t_{UCKL}$	UNLOAD CLOCK INPUT pulse width, $t_W$ (LOW)	4	7		36	7			ns
$t_{CLW}$	CLEAR pulse width, $t_W$ (low)	2	20			40			ns
$t_{CLCK}$	Setup time, clear release to load clock, $t_{SU}$	2	10			25†			ns

\* Data must be setup within 20 ns after valid Load Clock (A or B) pulse (positive transition).

† = Arrow indicates that it is referenced to the LOW-to-HIGH transition.

## Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	74S225A			74S225			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$f_{IN}$	Load clock A or clock B	Cascade Mode**	2	20	22		10	20		MHz
		Standalone Mode								
$t_{LCIRL}$	CLK A or CLK B to IR! **		2		43	55		55	75	ns
$t_{LCCOL}$	CLK A or CLK B to UNCK OUT†		2		31	40		25	50	ns
$f_{OUT}$	Unload clock input	Cascade Mode***	4	20	22		10	20		MHz
		Standalone Mode								
$t_{UCKORL}$	UNCK IN † to OR LOW		4		26	35		30	45	ns
$t_{UCKORH}$	UNCK IN † to OR HIGH		4		32	45		40	60	ns
$t_{ODH}$	Output data hold, UNCK IN to output data		4	20	30		20	50		ns
$t_{ODS}$	Output data setup, UNCK IN to output data		4		41	55		50	75	ns
$t_{RIP}$	CLK A or CLK B to OR †		7		167	220		190	300	ns
$t_{CLOL}$	CLR to OR †		6		31	40		35	60	ns
$t_{CLIH}$	CLR to IR †		6		15	20		16	35	ns
$t_{UCKOW}$	Pulse width, UNCK OUT, $t_W$		2	7	11		7	14		ns
$t_{ORD}$	OR † to output data		4		9	15		10	20	ns
$t_{BUBI}$	UNCK IN to IR † (bubble-back time)		8		214	290		255	400	ns
$t_{BUBC}$	UNCK IN to UNCK OUT † (bubble-back time)		8		226	290		270	400	ns

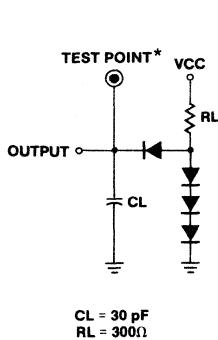
† Arrow indicates that it is referenced to the HIGH-to-LOW transition.

\*\* 16th word only.

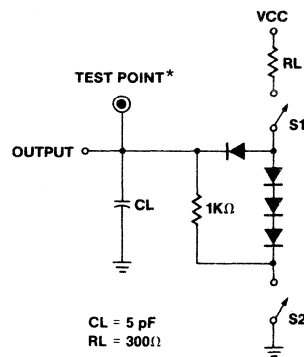
## Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225A			74S225			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PHZ}$	Output disable delay, $\overline{OE}$ to $Q_i$ , $C_L = 5$ pF	1	8		25	10	25	ns	
$t_{PLZ}$			18		25				
$t_{PZL}$	Output enable delay, $\overline{OE}$ to $Q_i$ , $C_L = 5$ pF	1	19		40	25	40	ns	
$t_{PZH}$			23		40				

### Test Load for Bi-State Output



### Test Load for Three-State Output



\* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse Amplitude = 3.0 V  
Input Rise and Fall Time (15%–90%) = 2.5 ns  
Measurements made at 1.5 V

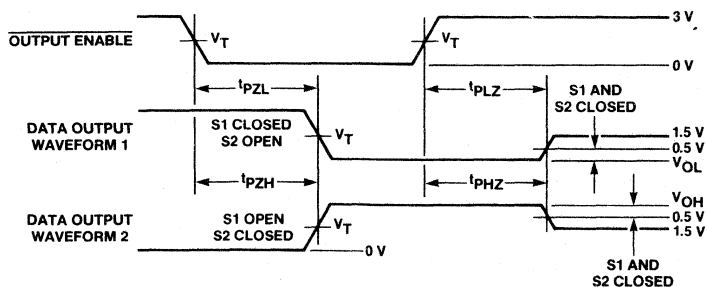


Figure 1. Enable and Disable

Waveform 1 is for an output with internal conditions such that the output is low except when disabled.

Waveform 2 is for an output with internal conditions such that the output is high

## Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{IL}$	Low-level input voltage						0.8	V	
$V_{IH}$	High-level input voltage				2.0			V	
$V_{IC}$	Input clamp voltage		$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.5	V	
$I_{IL1}$	Low-level input current	$D_0\text{-}D_4$	$V_{CC} = \text{MAX}$	$V_I = 0.5 \text{ V}$			-1	mA	
$I_{IL2}$		All others							-0.25
$I_{IH}$	High-level input current		$V_{CC} = \text{MAX}$	$V_I = 2.7 \text{ V}$	Data inputs			40	$\mu\text{A}$
					Others				
$I_I$	Maximum input current		$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$			1	mA	
$V_{OL}$	Low-level output voltage*		$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$ (Data outputs)				0.5	V
				$I_{OL} = 8 \text{ mA}$ (All others)					
$V_{OH}$	High-level output voltage		$V_{CC} = \text{MIN}$	$I_{OH} = -6.5 \text{ mA}$ (Data outputs)				2.4	V
				$I_{OH} = -3.2 \text{ mA}$ (All others)					
$I_{OS}$	Output short-circuit current**		$V_{CC} = \text{MAX}$	$V_O = 0 \text{ V}$	-30	-100		mA	
$I_{HZ}$	Off-state output current		$V_{CC} = \text{MAX}$	$V_O = 2.4 \text{ V}$			50	$\mu\text{A}$	
$I_{LZ}$			$V_{CC} = \text{MAX}$	$V_O = 0.5 \text{ V}$					-50
$I_{CC}$	Supply current		$V_{CC} = \text{MAX}$	Inputs low, All outputs open	74S225	80	120	mA	
					74S225A	80	125		

\* To measure  $V_{OL}$  on Pin 3, force 10 V on Pin 9 (Extended Testability).

\*\* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

## Functional Description

### Data Input

After power up the CLEAR is pulsed low (Figure 5) to prepare the FIFO to accept data in the first location. Clear must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH, the first location is ready to accept data from the  $D_X$  inputs. Data then present at the data inputs is entered into the first location when both Load Clocks (CLK A and CLK B) are brought HIGH. The CLK A HIGH and CLK B HIGH signal causes the IR and UNCK OUT to pulse LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front.  $t_{RIP}$  defines the time required for the first data to travel from input to the output of a previously empty device. When the sixteenth word is clocked into the device, the memory is full (sixteen words) and IR remains low. The Unload Clock Output is provided chiefly for use in cascading devices to extend FIFO depth (Figure 9). When Input Ready is Low, do not attempt to shift-in new data.

### Data Output

Data is read from the  $Q_X$  outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Unload Clock Input (UNCK IN) LOW. A LOW signal at UNCK IN causes the OR to go LOW. Valid data is maintained while the UNCK IN is LOW. When UNCK IN is brought HIGH the upstream data, provided that stage has valid data, is shifted to the output stage.

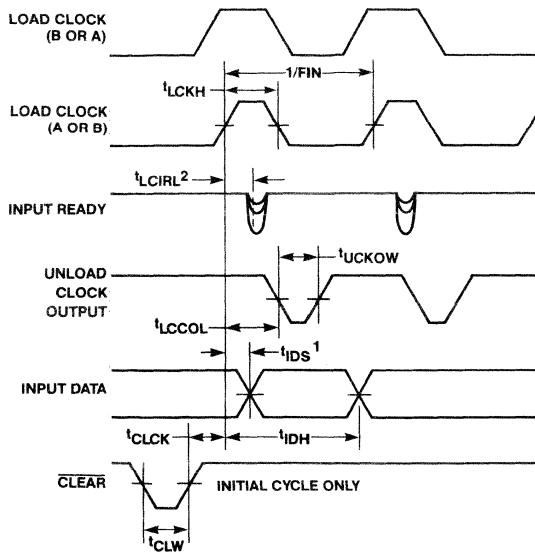
When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data remains valid for the last word.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least  $t_{BUBI}$ ) or completely empty (Output Ready stays LOW for at least  $t_{RIP}$ ).

## AC Test and High-Speed App. Notes

Since the FIFO is a high-speed device, care must be exercised in the design of the hardware and the timing utilized within the PC board design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1  $\mu\text{F}$  directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Load Clocks (A, B) — Unload Clock Output-Input Ready combination, as well as the Unload Clock Input-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Load Clock pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or affected by ( $\overline{\text{CLR}}$ ), the LOAD-CK activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time ( $t_{D(H)}$ ) and the next activity of Input Ready ( $t_{LCIRL}$ ) to be extended relative to Load Clock (A or B) going HIGH.

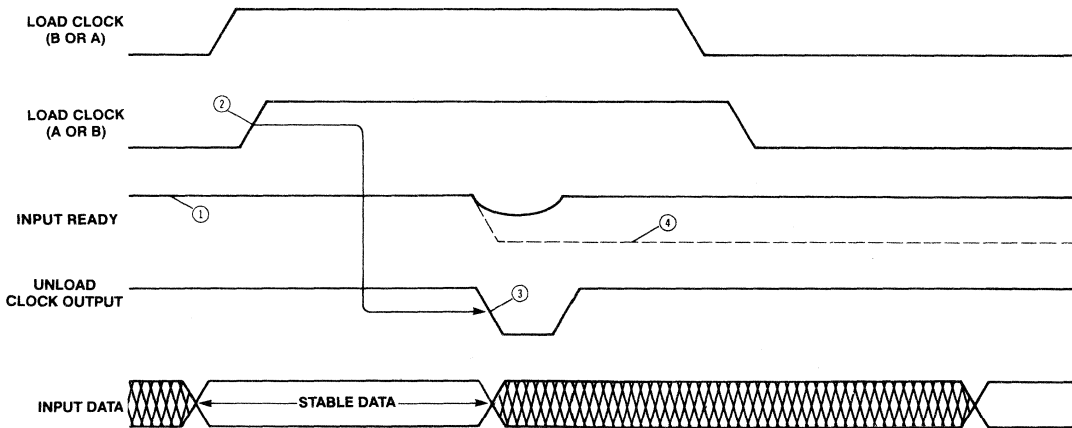




NOTES: 1. Permissible negative setup time for input data  
 2. Measure  $t_{LCIRL}$  for 16th input word only

2

Figure 2. Input Timing



NOTES: 1. Input Ready HIGH indicates space is available and a Load Clock (A and B) pulse may be applied.  
 2. Input Data is loaded into the first word.  
 3. Unload Clock Output pulses indicating the first word is full and the Data from the first word is released for "fall-through" to second word.  
 4. If the second word is already full, then the data remains at the first word. Since the FIFO is now full, Input Ready remains LOW.

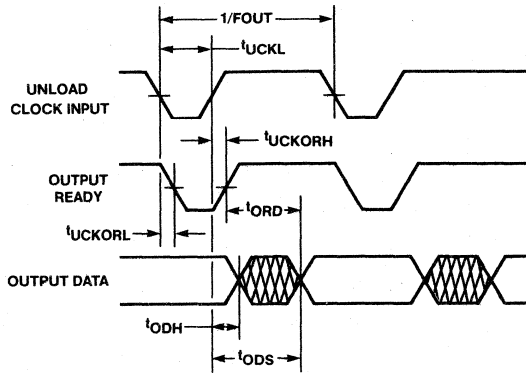
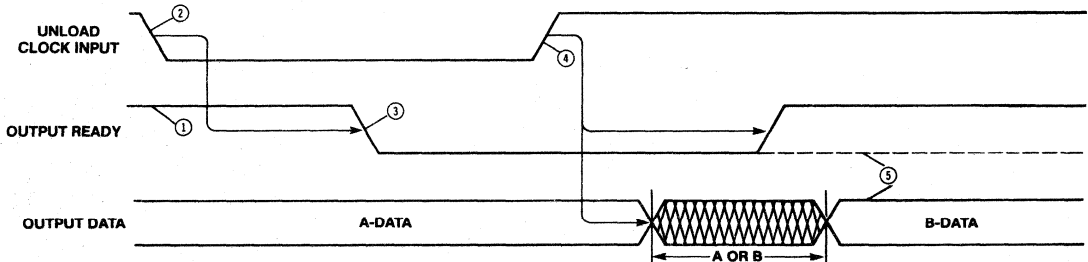


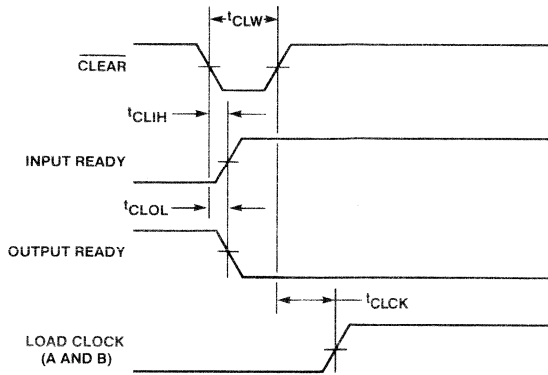
Figure 4. Output Timing



- NOTES: 1. Output Ready HIGH indicates that data is available and an Unload Clock Input pulse may be applied.  
 2. Unload Clock Input goes LOW creating an empty position at word 16 for word 15 to "fall-through" to.  
 3. Output Ready goes LOW.  
 4. Unload Clock Input goes HIGH, causing Output Ready to go HIGH, indicating that new data (B) is now available at the FIFO outputs.  
 5. If the FIFO has only one word loaded (A-DATA), then Output Ready stays LOW and the A-DATA remains on the outputs.

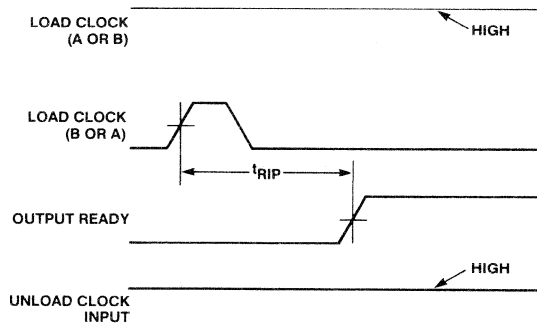
NOTE: Assume FIFO initially contains at least two words.

Figure 5. The Mechanism of Shifting Data Out of the FIFO



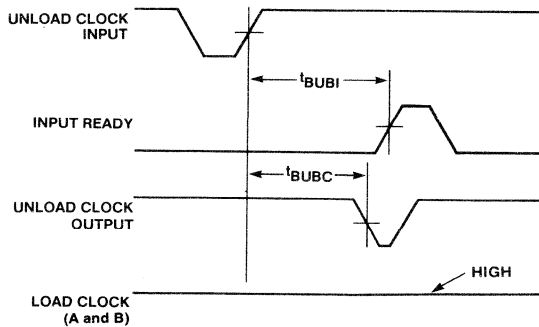
NOTE: Assume FIFO is full before  $\overline{\text{CLEAR}}$  goes active.

**Figure 6. Clear Timing**



NOTES: 1. FIFO is initially empty.  
2. Unload Clock Input and one Load Clock held HIGH throughout.

**Figure 7.  $t_{RIP}$  Specifications**



NOTES: 1. FIFO is initially full.  
2. Load Clock (A and B) held HIGH throughout.

**Figure 8.  $t_{BUBI}$ ,  $t_{BUBC}$  Specifications**

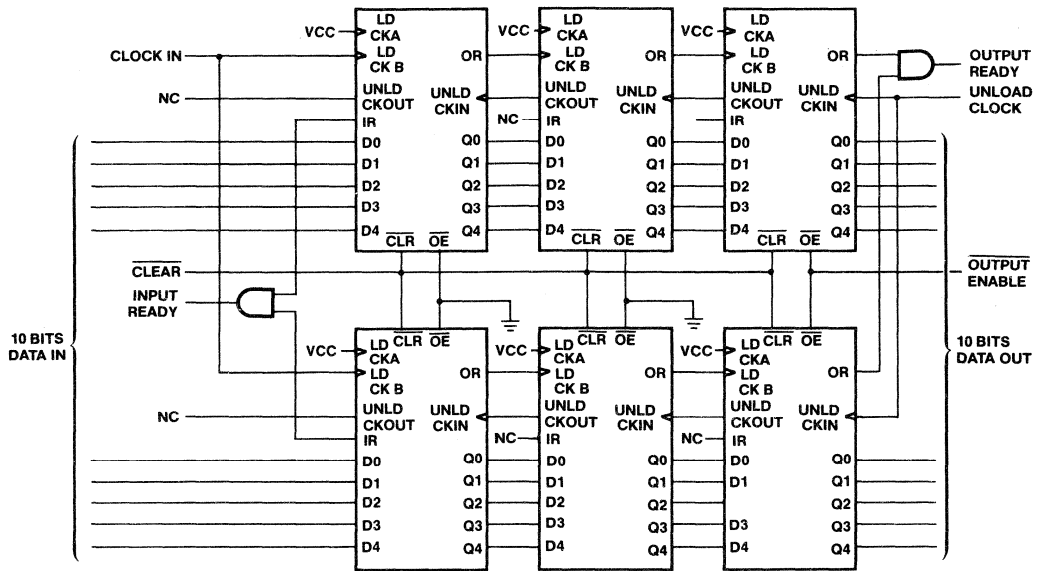


Figure 9. 48x10 FIFO with 74S225/A



# 67413A/67413

First-In First-Out (FIFO)  
64 x 5 Memory

## Features/Benefits

- High-speed 35 MHz shift-in/shift-out rates
- High-drive capability
- Three-state outputs
- Half-full and Almost-full/Empty status flags
- Structured pinouts. Output pins directly opposite corresponding input pins.
- Asynchronous operation
- TTL-compatible inputs and outputs

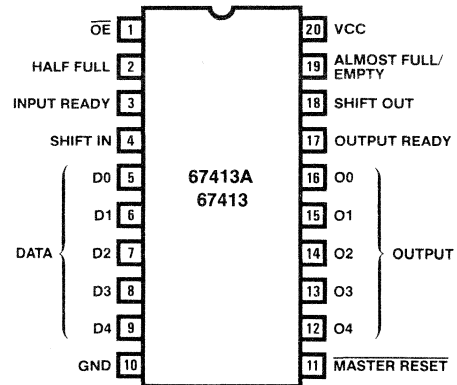
## Ordering Information

Part Number	Package	Temp	Description
67413A	CD 020	Com	35 MHz in/out
67413	CD 020	Com	25 MHz in/out

## Description

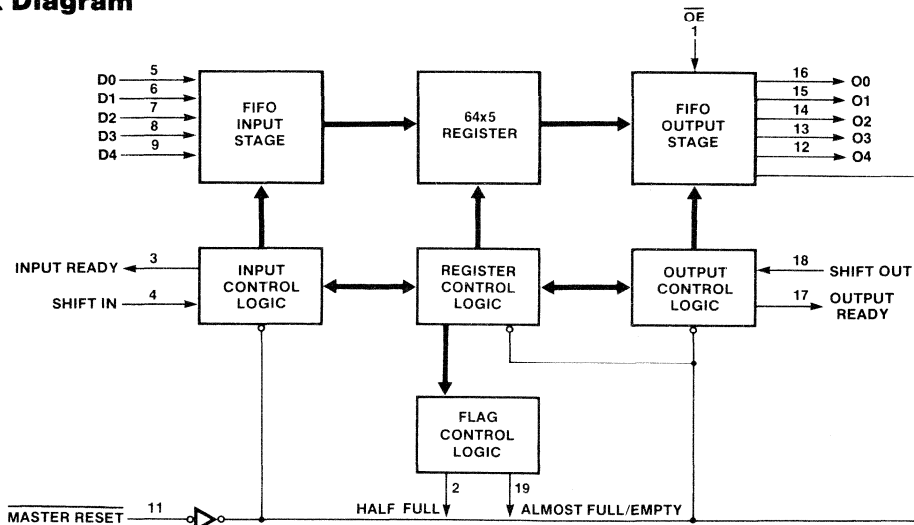
The 67413A is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at 35-MHz input/output rates (67413 operates at 25-MHz in-out). The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive ( $I_{OL} = 24 \text{ mA}$ ) data outputs. These devices can be connected in parallel to give FIFOs of any word length. It has a Half-full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of 67413A, 67413 are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

## Pin Configuration



2

## Block Diagram



## Absolute Maximum Ratings

Supply voltage $V_{CC}$ .....	-0.5 to 7 V
Input voltage .....	-1.5 to 7 V
Off-state output voltage .....	-0.5 to 5.5 V
Storage temperature .....	-65°C to +150°C

## Operating Conditions

SYMBOL	PARAMETER	FIGURE	67413A			67413			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
$T_A$	Operating free-air temperature		0		75	0		75	°C
$t_{SIH}^\dagger$	Shift in HIGH time	1	9			16			ns
$t_{SIL}^\dagger$	Shift in LOW time	1	17			20			ns
$t_{IDS}$	Input data setup	1	2			3			ns
$t_{IDH}$	Input data hold time	1	15			25			ns
$t_{SOH}^\dagger$	Shift Out HIGH time	5	9			16			ns
$t_{SOL}$	Shift Out LOW time	5	17			20			ns
$t_{MRW}^\dagger$	Master Reset pulse	10	30			35			ns
$t_{MRS}$	Master Reset to SI	10	35			35			ns

## Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67413A			67413			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$f_{IN}$	Shift in rate	1	DC DC		$\dagger\dagger 30$ $\dagger\dagger\dagger 35$	DC		25	MHz
$t_{IRL}^\dagger$	Shift In $\uparrow$ to Input Ready LOW	1		12	18		12	28	ns
$t_{IRH}^\dagger$	Shift In $\downarrow$ to Input Ready HIGH	1		14	20		14	25	ns
$f_{OUT}$	Shift Out rate	5	DC DC		$\dagger\dagger 30$ $\dagger\dagger\dagger 35$	DC		25	MHz
$t_{ORL}^\dagger$	Shift Out $\uparrow$ to Output Ready LOW	5		12	18		12	28	ns
$t_{ORH}^\dagger$	Shift Out $\downarrow$ to Output Ready HIGH	5		14	20		14	25	ns
$t_{ODH}^\dagger$	Output Data Hold (previous word)	5	12				10		ns
$t_{ODS}$	Output Data Shift (next word)	5			34			40	ns
$t_{PT}$	Data throughput or "fall through"	4, 8		510	650		510	750	ns
$t_{MRORL}$	Master Reset $\downarrow$ to Output Ready LOW	10		18	28		18	30	ns
$t_{MRIRH}$	Master Reset $\uparrow$ to Input Ready HIGH	10		21	28		21	30	ns
$t_{MRIRL}$	Master Reset $\downarrow$ Input Ready LOW*	10		18	28		18	30	ns
$t_{MRO}^*$	Master Reset $\downarrow$ to Outputs LOW	10		32	45		32	55	ns

Note: Typical at 5 V  $V_{CC}$  and 25°C  $T_A$ .

\* If the FIFO is not full (IR High), MR low forces IR low, followed by IR returning high when  $\overline{MR}$  goes high.

$\dagger$  See AC test and high-speed application note.

$\dagger\dagger$  Tested

$\dagger\dagger\dagger$  Guaranteed by design (see test load).

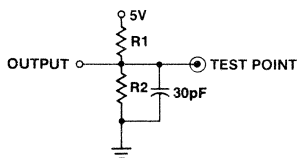
## Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	67413A			67413			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>IPH</sub>	Input ready pulse HIGH	4	5	12		5	12		ns
t <sub>OPH</sub>	Output ready pulse HIGH	8	5	12		5	12		ns
t <sub>ORD</sub>	Output ready † HIGH to Data Valid	5			18			20	ns
t <sub>AEH*</sub>	Shift Out † to AF/E HIGH	11		100	135		100	145	ns
t <sub>AEL*</sub>	Shift In † to AF/E LOW	11		450	600		450	650	ns
t <sub>AFL*</sub>	Shift Out † to AF/E LOW	12		450	600		450	650	ns
t <sub>AFH*</sub>	Shift In † AF/E HIGH	12		100	135		100	145	ns
t <sub>HFH*</sub>	Shift In † to HF HIGH	13		280	360		280	380	ns
t <sub>HFL*</sub>	Shift Out † to HF LOW	13		280	360		280	380	ns
t <sub>PHZ</sub>	Output Disable Delay	A		14	25		14	30	ns
t <sub>PLZ</sub>		A		14	25		14	30	
t <sub>PZL</sub>	Output Enable Delay	A		14	25		14	30	ns
t <sub>PZH</sub>		A		24	38		24	50	

Note: Input rise and fall time (10%-90%) = 2.5 ns. \* See timing diagram for explanation of parameters.

## 67413A/67413

### Standard Test Load

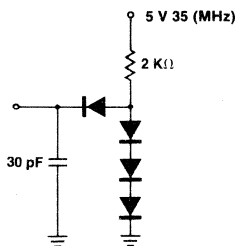


Input Pulse Amplitude = 3V  
 Input Rise and Fall Time (10%–90%) = 2.5 ns  
 Measurements made at 1.5 V

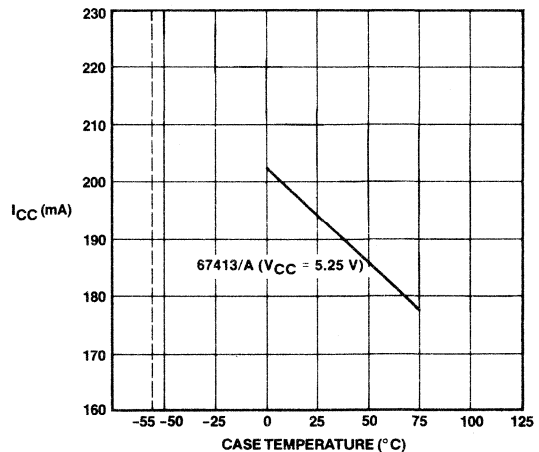
I <sub>OL</sub>	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

2

### Design Test Load



### Typical I<sub>CC</sub> vs Temperature (V<sub>CC</sub> = MAX)



## 67413 Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL			UNIT
			MIN	TYP	MAX	
t <sub>IPH</sub>	Input ready pulse HIGH	4	5	12		ns
t <sub>OPH</sub>	Output ready pulse HIGH	8	5	12		ns
t <sub>ORD</sub>	Output ready ↑ HIGH to Data Valid	5			20	ns
t <sub>AEH</sub> *	Shift Out ↑ to AF/E HIGH	11		100	145	ns
t <sub>AEL</sub> *	Shift In ↑ to AF/E LOW	11		450	650	ns
t <sub>AFL</sub> *	Shift Out ↑ to AF/E LOW	12		450	650	ns
t <sub>AFH</sub> *	Shift In ↑ to AF/E HIGH	12		100	145	ns
t <sub>HFH</sub> *	Shift In ↑ to HF HIGH	13		280	380	ns
t <sub>HFL</sub> *	Shift Out ↑ to HF LOW	13		280	380	ns
t <sub>PHZ</sub>	Output Disable Delay	A		14	30	ns
t <sub>PLZ</sub>		A		14	30	ns
t <sub>PZL</sub>	Output Enable Delay	A		14	30	ns
t <sub>PZH</sub>		A		24	50	ns

Note: Input rise and fall time (10%-90%) = 2.5 ns.

\* See timing diagram for explanation of parameters.



## Absolute Maximum Ratings

Supply voltage $V_{CC}$ .....	-0.5 V to 7 V
Input voltage .....	-1.5 V to 7 V
Off-state output voltage .....	-0.5 V to 5.5 V
Storage temperature .....	-65° to +150°C

## 67413 Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL			UNIT
			MIN	TYP	MAX	
$V_{CC}$	Supply voltage		4.75	5	5.25	V
$T_A$	Operating free-air temperature		0		75	°C
$t_{SIH}^\dagger$	Shift in HIGH time	1	16			ns
$t_{SIL}^\dagger$	Shift in LOW time	1	20			ns
$t_{IDS}$	Input data set up	1	3			ns
$t_{IDH}$	Input data hold time	1	25			ns
$t_{SOH}^\dagger$	Shift Out HIGH time	5	16			ns
$t_{SOL}$	Shift Out LOW time	5	20			ns
$t_{MRW}$	Master Reset pulse $\dagger$	10	35			ns
$t_{MRS}$	Master Reset to SI	10	35			ns

2

## 67413 Switching Characteristics Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL			UNIT
			MIN	TYP	MAX	
$f_{IN}$	Shift in rate	1	DC		25	MHz
$t_{IRL}^\dagger$	Shift In $\uparrow$ to Input Ready LOW	1		12	28	ns
$t_{IRH}^\dagger$	Shift In $\downarrow$ to Input Ready HIGH	1		14	25	ns
$f_{OUT}$	Shift Out rate	5	DC		25	MHz
$t_{ORL}^\dagger$	Shift Out $\uparrow$ to Output Ready LOW	5		12	28	ns
$t_{ORH}^\dagger$	Shift Out $\downarrow$ to Output Ready HIGH	5		14	25	ns
$t_{ODH}^\dagger$	Output Data Hold (previous word)	5	10			ns
$t_{ODS}$	Output Data Shift (next word)	5			40	ns
$t_{PT}$	Data throughput or "fall through"	4,8		510	750	ns
$t_{MRORL}$	Master Reset $\downarrow$ to Output Ready LOW	10		18	30	ns
$t_{MRIRH}$	Master Reset $\uparrow$ to Input Ready HIGH	10		21	30	ns
$t_{MRIRL}$	Master Reset $\downarrow$ Input Ready LOW*	10		18	30	ns
$t_{MRO}$	Master Reset $\downarrow$ to Outputs LOW	10		32	55	ns

Note: Typical at 5 V  $V_{CC}$  and 25°C  $T_A$ .

\* If the FIFO is not full (IR High),  $\overline{MR}$  low forces IR low, followed by IR returning high when  $\overline{MR}$  goes high.

$\dagger$  See AC test and high-speed application note.

## Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
V <sub>IL</sub>	Low-level input voltage				0.8 †		V	
V <sub>IH</sub>	High-level input voltage				2 †		V	
V <sub>IC</sub>	Input clamp voltage	V <sub>CC</sub> = MIN	I <sub>I</sub> = -18 mA		-1.5		V	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX	V <sub>I</sub> = 0.45 V		-250		μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX	V <sub>I</sub> = 2.4 V		50		μA	
I <sub>I</sub>	Maximum input current	V <sub>CC</sub> = MAX	V <sub>I</sub> = 5.5 V		1		mA	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN	I <sub>OL</sub> (Data outputs)	67413A 67413	24 mA		0.5	V
			I <sub>OL</sub> (IR, OR)	67413A 67413	8 mA ††			
			I <sub>OL</sub> (Flag outputs)	67413A 67413	8 mA			
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN	I <sub>OH</sub> (Data outputs)	67413A 67413	-3.0 mA		2.4	V
			I <sub>OH</sub> (IR, OR)		-0.9 mA			
			I <sub>OH</sub> (Flag outputs)		-0.9 mA			
I <sub>OS</sub>	Output short-circuit current*	V <sub>CC</sub> = MAX	V <sub>O</sub> = 0 V		-20	-90	mA	
I <sub>HZ</sub>	Off-state output current	V <sub>CC</sub> = MAX	V <sub>O</sub> = 2.4 V		+20		μA	
I <sub>LZ</sub>		V <sub>CC</sub> = MAX	V <sub>O</sub> = 0.4 V		-20		μA	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX. All inputs low. All outputs open. (67413A/67413)			**240		mA	

\* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

\*\* See curve for I<sub>CC</sub> vs. temp.

† There are absolute voltages with respect to GND (PIN 8 or 9) and includes all overshoots due to test equipment.

†† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

## Functional Description

### Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D<sub>x</sub> inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). t<sub>PT</sub> defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

### Data Output

Data is read from the O<sub>x</sub> outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the

presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t<sub>PT</sub>) or completely empty (Output Ready stays LOW for at least t<sub>PT</sub>).

## AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V<sub>CC</sub> and GND with very short lead length. In addition,

care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity

will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time ( $T_{IDH}$ ) and the next activity of Input Ready ( $T_{IRL}$ ) to be extended relative to Shift-Ingoing HIGH. This same type of problem is also related to  $T_{IRH}$ ,  $T_{ORL}$  and  $T_{ORH}$  as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

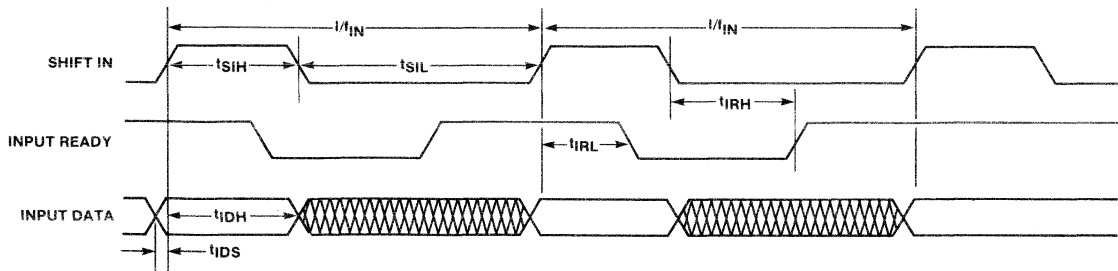


Figure 1. Input Timing

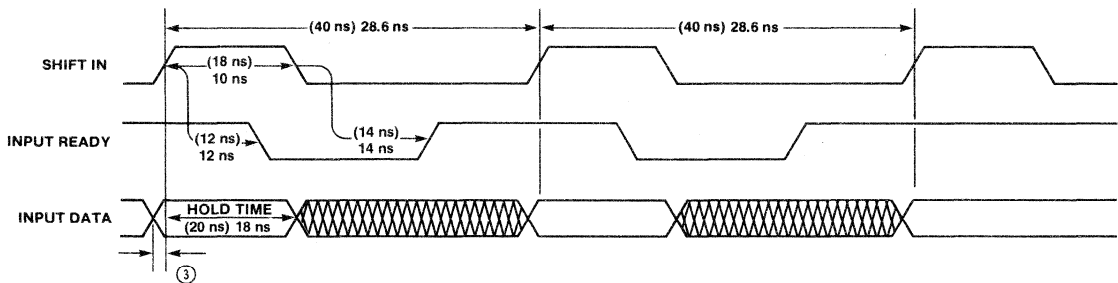


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate (67413A)

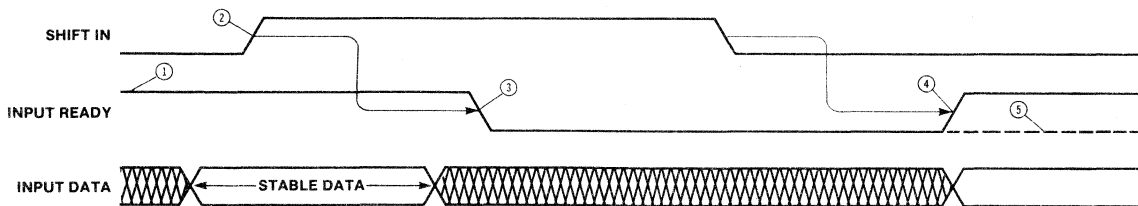
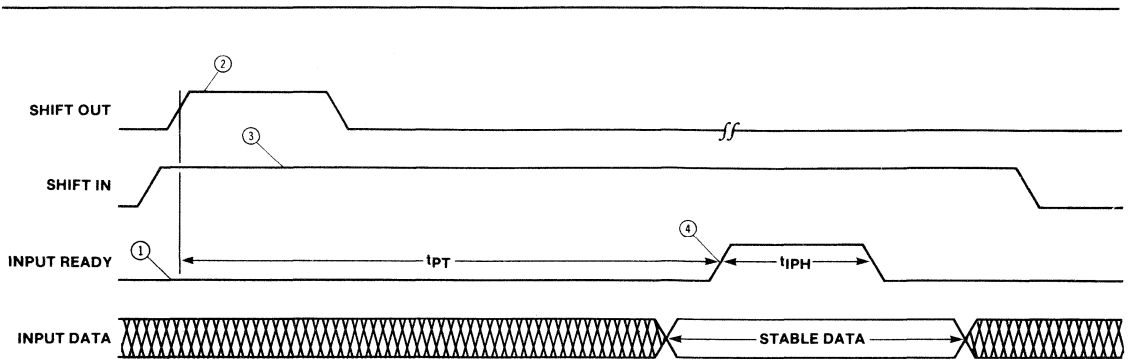


Figure 3. The Mechanism of Shifting Data into the FIFO

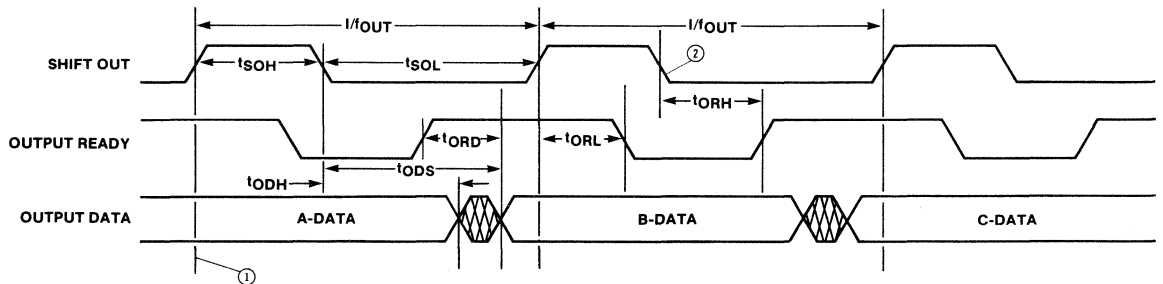
- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- ② Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
- ③ Input Ready goes LOW indicating the first word is full.
- ④ Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
5. If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored. (See Figure 5).



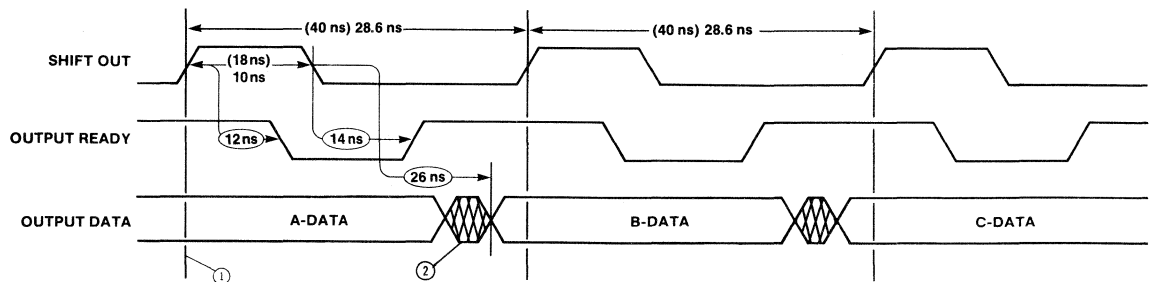
**Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH**

- ① FIFO is initially full.
- ② Shift Out pulse is applied. An empty location starts "bubbling" to the front.
- ③ Shift In is held HIGH
- ④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.



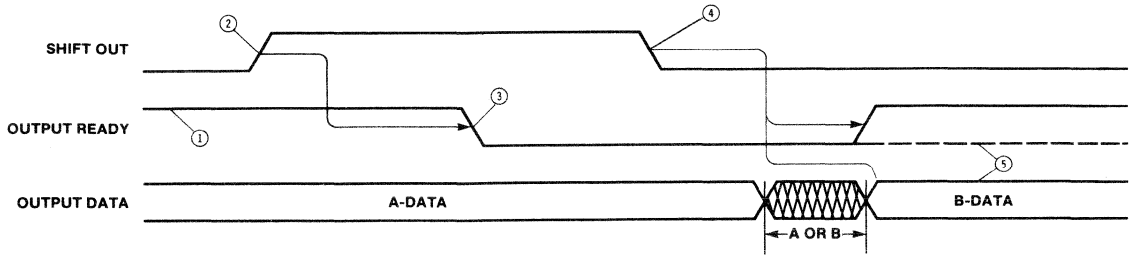
**Figure 5. Output Timing**

- ① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- ② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.



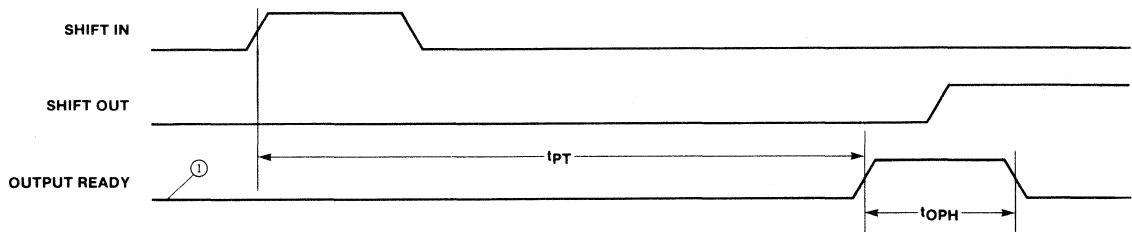
**Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate (67413A)**

- ① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- ② Data in the first crosshatched region may be A or B Data.



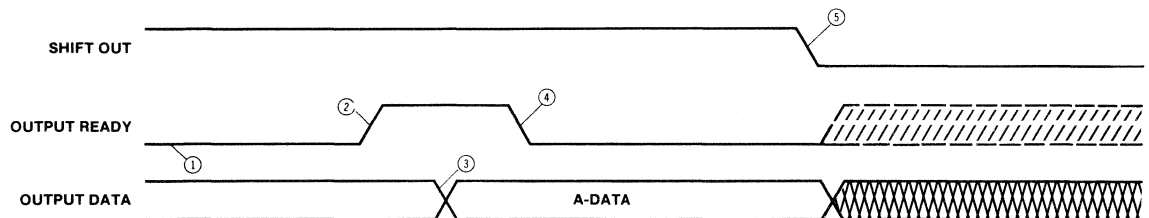
**Figure 7. The Mechanism of Shifting Data Out of the FIFO**

- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
- ③ Output Ready goes LOW.
- ④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- ⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.



**Figure 8.  $t_{PT}$  and  $t_{OPH}$  Specification**

- ① FIFO initially empty.



**Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH**

- ① Word 63 is empty.
- ② Output Ready goes HIGH indicating arrival of the new data.
- ③ New data (A) arrives at the outputs (word 63).
- ④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- ⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

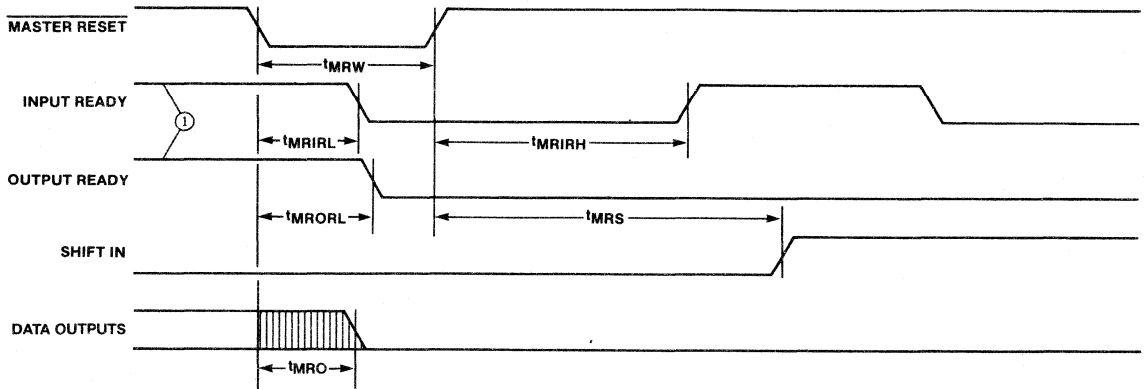


Figure 10. Master Reset Timing

① FIFO is partially full.

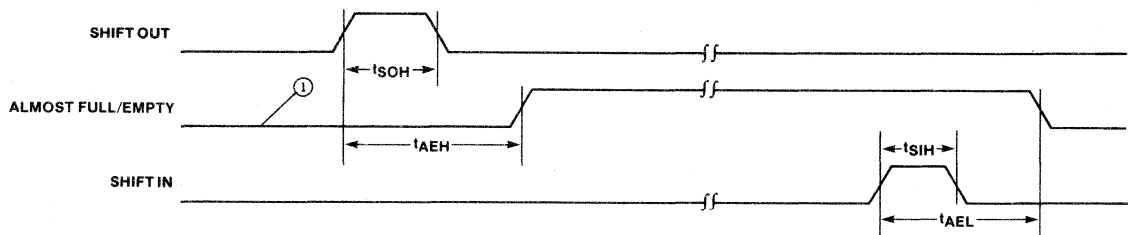


Figure 11.  $t_{AEH}$ ,  $t_{AEL}$  Specifications

① FIFO contains 9 words (one more than almost empty).

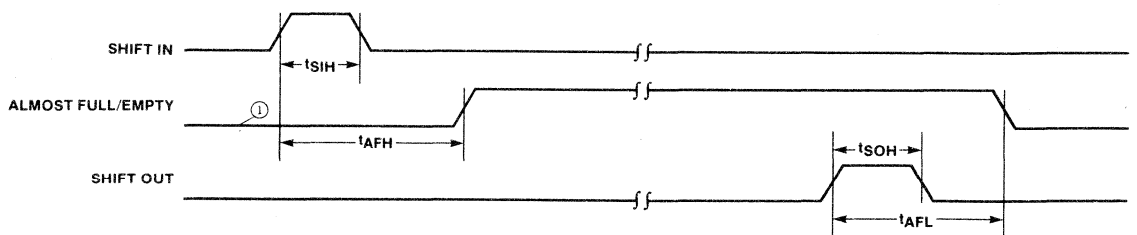


Figure 12.  $t_{AFH}$ ,  $t_{AFL}$  Specifications

① FIFO contains 55 words (one short of almost full)

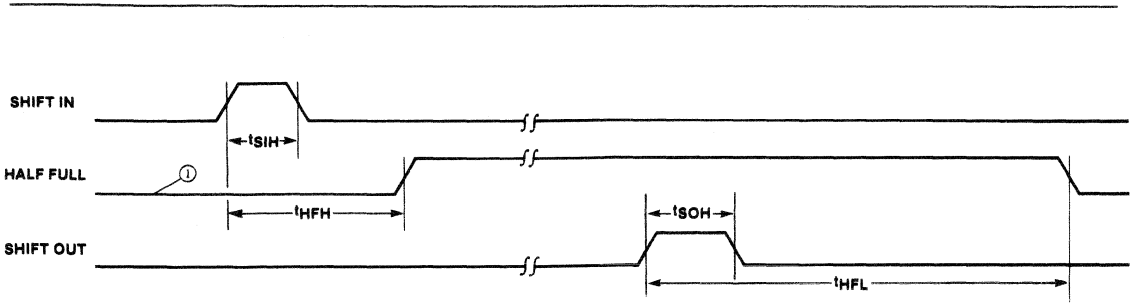


Figure 13.  $t_{HFL}$ ,  $t_{HFH}$  Specifications

① FIFO contains 31 words (one short of half full).

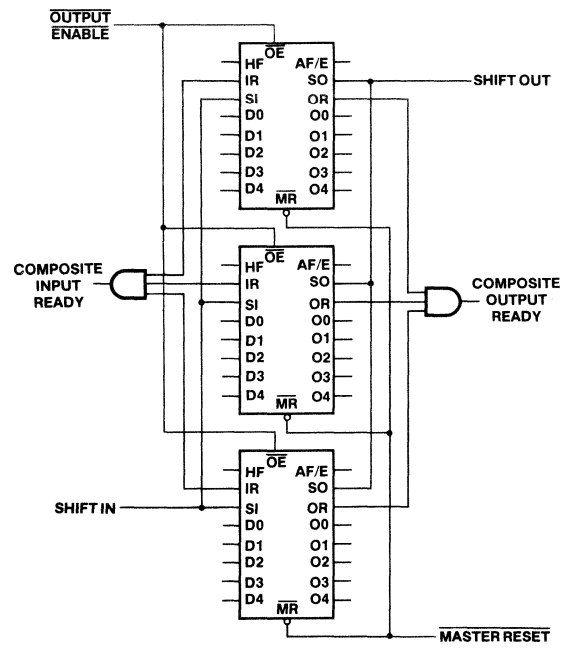


Figure 14. 64x15 FIFO with 67413A/67413

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall through times of the FIFOs.

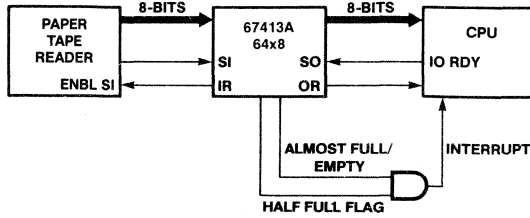
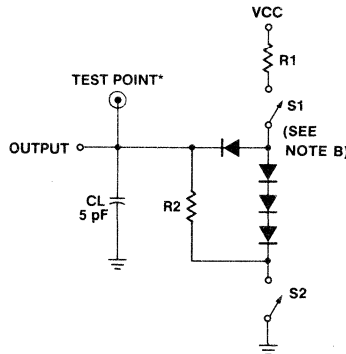


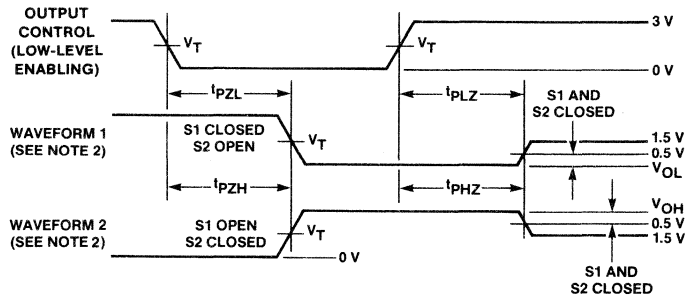
Figure 15. Application for 67413A "Slow and Steady Rate to Fast 'Blocked Rate' "

Note: Cascading the FIFO's in word width is done by ANDING the IR and OR as shown in Figure 14.

### Three-State Test Load



### Design Test Load



Enable and Disable

- Notes:
- A. All diodes are 1N916 or 1N3064.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
  - D. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.





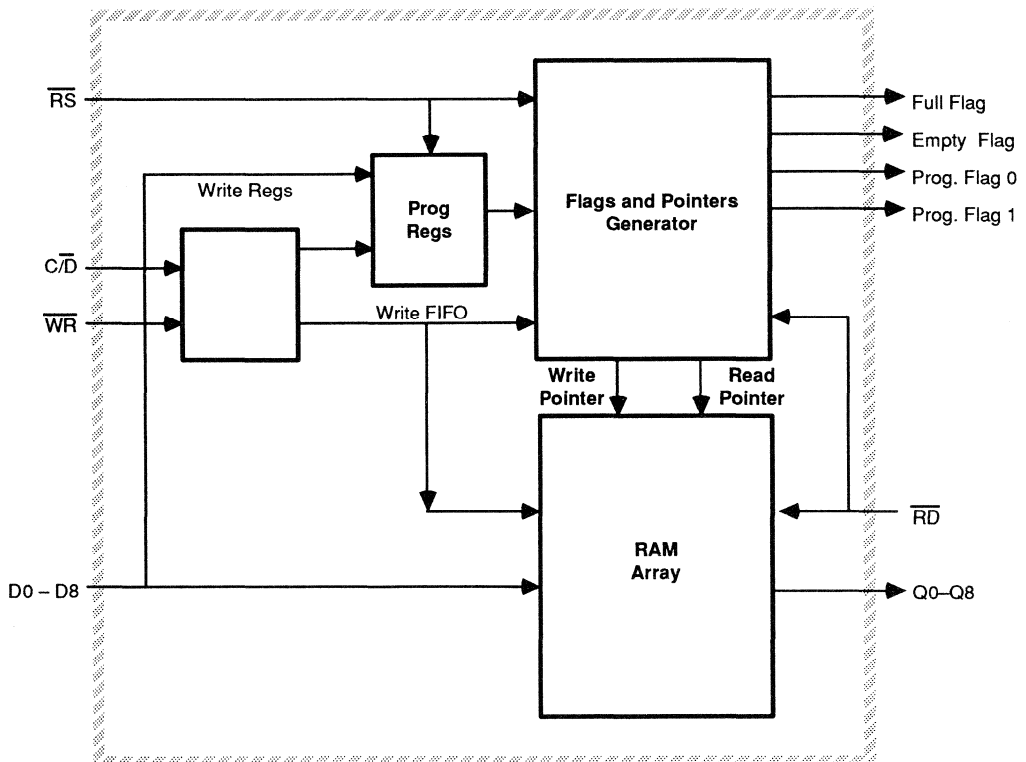
# Am4601

## Programmable-Flags, 512 x 9 FIFO

### DISTINCTIVE CHARACTERISTICS

- Two programmable flags; programmable from 1 to 511 in increments of one
- Full and empty flags
- 45nSec read and write cycle-time
- CMOS part with TTL-compatible I/O
- RAM-based architecture; short fallthrough time delays
- Programmable polarity for all the flags
- Identical Data, WR, RD pinout as standard Am7201 FIFO
- 28 Pin, 300 mil plastic dip
- 32 pin, PLCC

### BLOCK DIAGRAM



11684-001A

## GENERAL DESCRIPTION

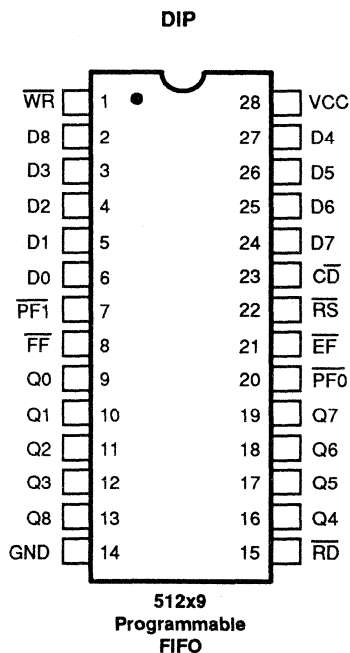
The Am4601 is a RAM-based CMOS register programmable FIFO (PFIFO) that is 512 words deep with 9-bit wide words. It is expandable to create wider words.

This programmable FIFO (PFIFO) can accept data and output data asynchronously and simultaneously at data rates from 0 to 22 MHz. Status flags are provided to signify empty and full, plus two programmable flags which can be programmed from 1 to 511 words in increments

of one. Programmable polarity is available for all flags. Programmable depth is supported for applications requiring a programmable digital delay line.

The PFIFO is useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am4601 useful in communication, image processing, mass storage, DSP and printing systems.

## CONNECTION DIAGRAM



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## FUNCTIONAL DESCRIPTION

The Am4601 is a 512 x 9 RAM-based, CMOS Programmable FIFO (PFIFO) designed with three programmable features. (See block diagram.) The RAM-based PFIFO stores the data written into them in a sequential pattern.

The PFIFO offers two operational modes. The first mode resembles its counterpart Am7201, a standard, asynchronous 512 x 9 FIFO. The second is a programming mode, where two flags, the word depth and flag polarities can be register programmed to allow the system designer to optimize the system performance. The operational mode is determined by the use of the Command/Data (C/D) input pin.

The RAM array has dedicated write and read address pointers. The Empty Flag prevents reading while empty, a data underflow condition. While the Full Flag prevents writing while full, a data overflow condition.

In the programming mode, input data is written into a group of registers whose contents control the three programming features. Two dedicated programmable flags can be set at any location from 1 to 511, in increments of one. These two flags could, for example, be used to indicate Almost Empty or Almost Full conditions. The polarity of all flags (two programmable flags, Empty and Full flags) can be independently programmed to be active-low or active-high. The FIFO depth can also be programmed, in conjunction with the programmable flags to any depth of less than 512 words deep. The programming registers are only accessible if the FIFO is empty.

The Master Reset ( $\bar{RS}$ ) sets the FIFO to Empty. The  $\bar{RS}$  will reset the write and read pointers and the registers' pointer to address zero. All of the control bits in the register will reset to a default value. After  $\bar{RS}$  the user may write data to the FIFO while the registers are in their default values or program the registers before writing data.

---

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, VCC	-0.5 V to +7.0V
Input voltage	-0.5 to VCC +0.5V
Operating temperature	0° C to +70° C
Storage temperature	-55° C to +150° C
Power dissipation	1.0 W
D.C. output current	50 mA

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

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## OPERATING RANGES

### Commercial Devices

Ambient Temperature ( $T_A$ )	0 to +75° C
Supply voltage (Vcc)	+4.5 to +5.5V

# 67417

## Serializing First-In First-Out (FIFO) 64 x 8/9 Memory

### Features/Benefits

- High-speed 28-MHz serial shift-in/shift-out rate
- 10-MHz parallel shift-in/shift-out rate
- Three-state outputs with Hi-current drive
- Cascadable at parallel port only
- Half-full flag (32 or more)
- Selectable 64x8 or 64x9 FIFO configuration thus providing "frame mark bit"

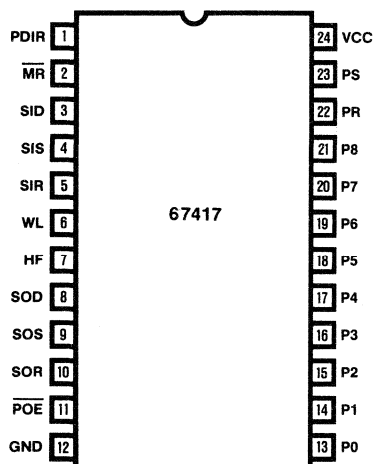
### Typical Applications

- LAN equipment
- Data communication
- Office automation
- Microcomputers
- Minicomputers
- Disk/tape controllers

### Description

The 67417 is a serializing/deserializing FIFO. This FIFO, the first one of its type in the industry, is organized 64 words x 8/9 bits wide. Like traditional Monolithic Memories' FIFOs it is cascadable, but only at the parallel port.

### Pin Configuration



### Ordering Information

Part Number	Package	Temp	Description
67417	CD 024	Com	64x8/9

In addition, the device has the ability to connect directly to a system bus. These features make it a complete "sub-system on a chip."

The FIFO basically has three modes of operation;

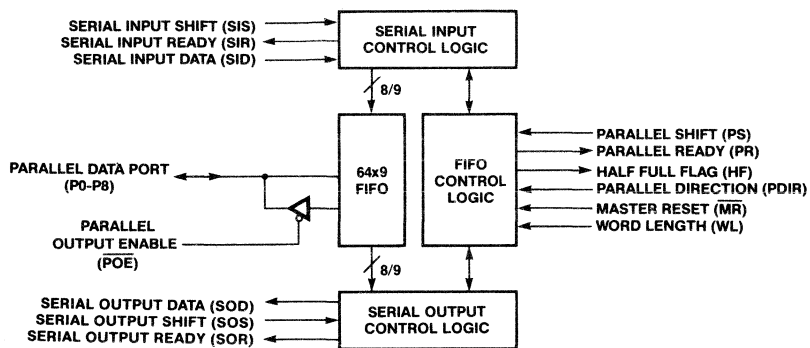
1. Serial in to parallel out
2. Parallel in to serial out
3. Serial in to serial out (requires non-standard logic level on PDIR).

In the first mode, serial data can be accepted at up to 28 MHz and the FIFO outputs parallel data at up to 10 MHz. Similarly, in the alternate mode parallel data can be transformed into serial data. Please refer to appendix for detailed description.

### Pin Names

P0-P8	Parallel Data
PS	Parallel Shift In/Out
PR	Parallel Input/Output Ready
$\overline{\text{POE}}$	Parallel Output Enable
SID	Serial Input Data
SIS	Serial Input Shift
SIR	Serial Input Ready
SOD	Serial Output Data
SOS	Serial Output Shift
SOR	Serial Output Ready
PDIR	Parallel Port Direction
WL	Word Length
$\overline{\text{MR}}$	Master Reset
HF	Half Full Flag
VCC	VCC
GND	Ground

## Block Diagram



## Absolute Maximum Ratings

Supply voltage $V_{CC}$ .....	-0.5 V to 7 V
Input voltage .....	-1.5 V to 7 V
Off-state output voltage .....	-0.5 V to 5.5 V
Storage temperature .....	-65° to +150°C

## Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL			UNIT
			MIN	TYP	MAX	
$V_{CC}$	Voltage		4.75	5	5.25	V
$T_A$	Operating free-air temperature		0		75	°C
<b>SERIAL INPUT PARAMETERS</b>						
$f_{SIN}$	Max. Serial Shift-In Rate	1			28	MHz
$t_{SISH}$	Serial Shift-In HIGH time	1	23			ns
$t_{SISL}$	Serial Shift-In LOW time	1	12			ns
$t_{SIDS}$	Serial Input Data Setup time	1	14			ns
$t_{SIDH}$	Serial Input Data Hold time	1	0			ns
$t_{SIRHS}$	Recovery Time Serial Input Ready † to Serial Input Shift †	1	0			ns
<b>SERIAL OUTPUT PARAMETERS</b>						
$f_{SOUT}$	Max. Serial Shift-Out Rate	1			28	MHz
$t_{SOSH}$	Serial Shift-Out HIGH time	3	15			ns
$t_{SOSL}$	Serial Shift-Out LOW time	3	15			ns
$t_{ORHS}$	Recovery time Serial Output Ready † to Serial Output Shift †	3	5			ns
<b>WORD LENGTH PARAMETERS</b>						
$t_{SWL}$	Setup SIS, SOS	1,3	18			ns
$t_{HWL}$	Hold SIS, SOS	1,3	3			ns
<b>PARALLEL PORT PARAMETERS</b>						
$f_p$	Parallel shift-in/shift-out rate	8			10	MHz
$t_{PSH}$	Parallel Shift-In/Out HIGH time	5/8	30			ns
$t_{PSL}$	Parallel Shift-In/Out LOW time	5/8	30			ns
$t_{PIDS}$	Parallel Input Data Setup time	5	-5			ns
$t_{PIDH}$	Parallel Input Data hold time	5	35			ns
$t_{PDIRSL}$	Shift LOW to parallel direction transition	14	50			ns
$t_{PDIRSH}$	Parallel direction transition to Shift HIGH	14	50			ns
$t_{PRHS}$	Parallel Ready † to Parallel Shift Low	10/11	30			ns
<b>MASTER RESET PARAMETER</b>						
$t_{MRW}$	Master Reset LOW time	12/13	40			ns

## Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL			UNIT
			MIN	TYP	MAX	
<b>SERIAL INPUT PARAMETERS</b>						
t <sub>SIRL</sub>	Serial Input Shift ↑ to Serial Input Ready LOW	2			23	ns
t <sub>SIHFH</sub>	Serial Input Shift ↑ to Half-Full Flag HIGH	7			1.3	μs
<b>SERIAL OUTPUT PARAMETERS</b>						
t <sub>SORL</sub>	Serial Output Shift ↑ to Serial Output Ready LOW	4			23	ns
t <sub>SOD</sub>	Serial Output Shift ↑ to Serial Output data	3			23	ns
t <sub>ODRH</sub>	Serial Output Data valid to Serial Output Ready HIGH	3	0	25		ns
t <sub>SOHFL</sub>	Serial Output Shift ↑ to Half-Full LOW	7			1.3	μs
<b>PARALLEL INPUT/OUTPUT PARAMETERS</b>						
t <sub>PSPRL</sub>	Parallel Shift ↑ to Parallel Ready LOW	5/8			65	ns
t <sub>PSPRH</sub>	Parallel Shift ↓ to Parallel Ready HIGH	5/8/10			80	ns
t <sub>PSHFH</sub>	Parallel Shift-In ↓ to Half-Full HIGH	6			1.3	μs
t <sub>PSHFL</sub>	Parallel Shift-Out ↓ to Half-Full LOW	9			1.3	μs
<b>PARALLEL OUTPUT PARAMETERS</b>						
t <sub>PODH</sub>	Minimum Parallel Shift ↓ to Output data	8	20			ns
t <sub>POD</sub>	Maximum Parallel Shift ↓ to Output data	8			60	ns
t <sub>PODV</sub>	Minimum Output data valid to parallel ready HIGH	8	0	15		ns
<b>OTHER PARAMETERS</b>						
t <sub>PT</sub>	Fall-through time	10/11/16/17			2.6	μs
t <sub>IPH</sub>	Parallel Input Ready pulse HIGH	11	30			ns
t <sub>OPH</sub>	Parallel Output Ready pulse HIGH	10	30			ns
t <sub>MRO</sub>	Master Reset ↓ to Data Out LOW	12			65	ns
t <sub>MRSIRL</sub>	Master Reset ↓ to Serial Input Ready LOW	12			40	ns
t <sub>MRSIRH</sub>	Master Reset ↑ to Serial Input Ready HIGH	12			40	ns
t <sub>MRPRL</sub>	Master Reset ↓ to Parallel Ready LOW	12/13			40	ns
t <sub>MRPRH</sub>	Master Reset ↑ to Parallel Ready HIGH	13			30	ns
t <sub>MRSORL</sub>	Master Reset ↓ to Serial Output Ready LOW	13			40	ns
t <sub>MRHFL</sub>	Master Reset ↓ to Half-Full LOW	12/13			60	ns
t <sub>PDIROR</sub>	Parallel Direction change to new Output Ready	14			60	ns
t <sub>PDIROD</sub>	Parallel Direction change to Output data valid	14			60	ns
t <sub>PDIRPZ</sub>	Parallel Direction change to Parallel Output data Hi-Z	14			35	ns
t <sub>PDIRSZ</sub>	Parallel Direction changes to Serial Output-data Hi-Z	14			80	ns
t <sub>PZX</sub>	Output enable time POE to P0-8	15			30	ns
t <sub>PXZ</sub>	Output disable time POE to P0-8	15			35	ns

## Electrical Characteristics Over Operating Conditions

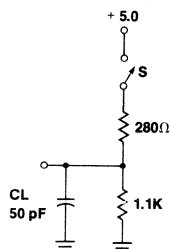
SYMBOL	PARAMETER	TEST CONDITIONS		COM			UNIT	
				MIN	TYP	MAX		
$V_{IL}$	Low-level input voltage					0.8†	V	
$V_{IH}$	High-level input voltage					2†	V	
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.5	V	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.4	mA	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4 \text{ V}$			0.1	mA	
$I_I$	Maximum input current	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$			0.4	mA	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	Data Outputs P0-P8, SOD	$I_{OL} = 24 \text{ mA}$	0°C-75°C	0.58	V	
					25°C	0.55		
			All other outputs	$I_{OL} = 16 \text{ mA}$	0°C-75°C	0.5		
				$I_{OL} = 8 \text{ mA}$		0.5		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -3 \text{ mA}$			2.4	V	
$I_{OS}$	Output short-circuit current*	$V_{CC} = \text{MAX}$	$V_O = 0 \text{ V}$			-20	-90	mA
$I_{LZ}$	Off-state output current*	SOD P0 to P8	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$		-100	$\mu\text{A}$	
$I_{HZ}$				$V_O = 2.4 \text{ V}$		100	mA	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$				350	mA	
$O_V$	PDIR non-standard over voltage	Serial-In, Serial-Out				10	16	V

\* Not more than one output should be shorted at a time and duration of the short circuit not exceed one second.

† This is an absolute voltage with respect to device GND (pin 12) and includes all overshoots due to test equipment.

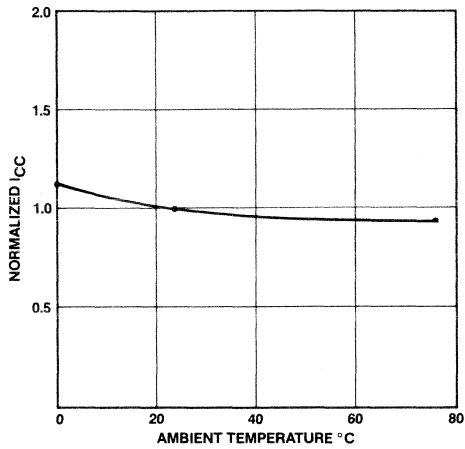
## Test Waveforms

TEST	S = OPEN	S = CLOSED	OUTPUT WAVEFORM-MEAS-LEVEL
All $t_{PD}$		All $t_{PD}$	
$t_{PXZ}$	$t_{PHZ}$	$t_{PLZ}$	
$t_{PZX}$	$t_{PZH}$	$t_{PZL}$	

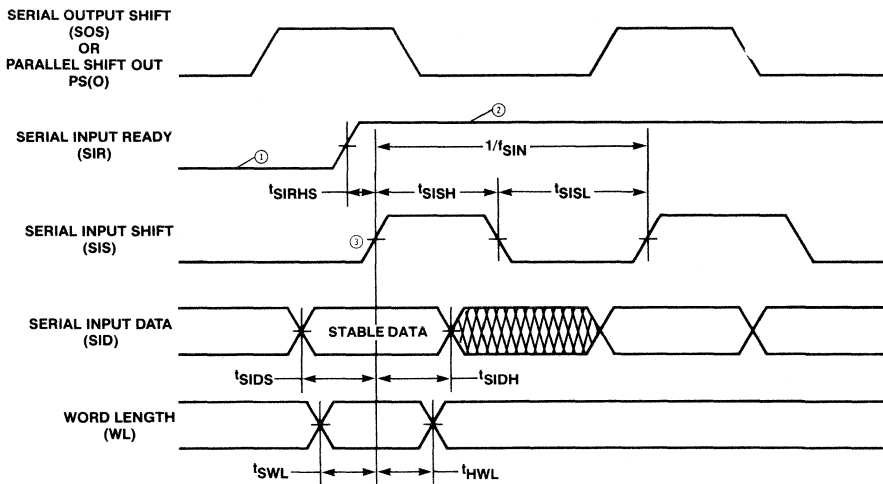




# ICC VS Temperature

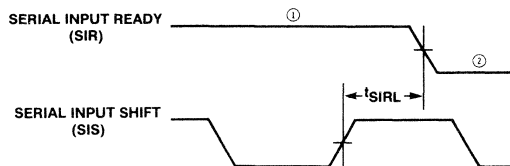


## Definition of Waveforms



- ① FIFO is full.
- ② Shift-out (serial or parallel) is asserted, SIR goes High.
- ③ SIS can be asserted  $t_{SIRHS}$  after serial input ready changes from low-to-high.

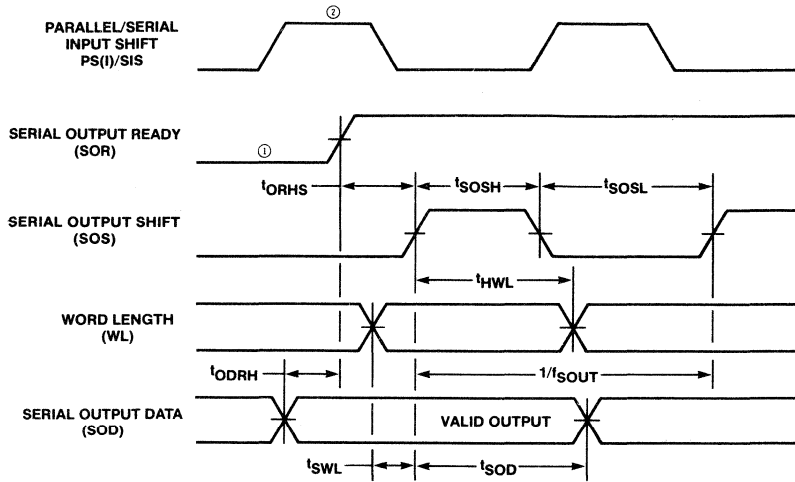
Figure 1. Serial Input Timing



- ① FIFO is not full.
- ② FIFO is full

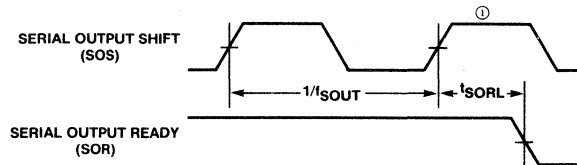
Figure 2. FIFO Full Specification ( $t_{SIRL}$ )

## Definition of Waveforms (cont'd)



- ① FIFO is empty, output ready remains Low and shift-out cannot be applied.
- ② After a word is shifted in, output ready goes High and shift-out can be applied.
- ③ The first serial bit is P0.

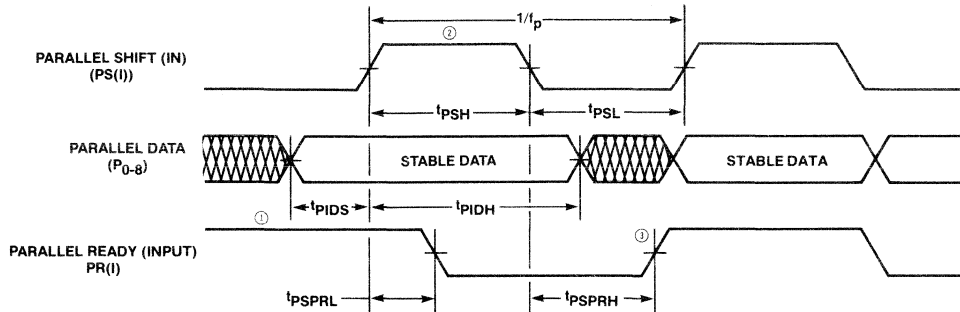
Figure 3. Serial Output Timing



- ① After the last shift-out, output ready goes Low indicating FIFO is empty.

Figure 4. FIFO Empty Specifications ( $t_{SORL}$ ),

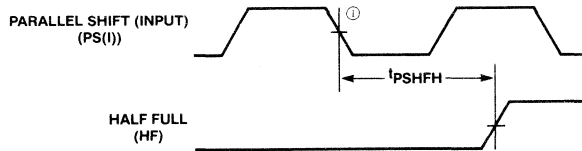
## Definition of Waveforms (cont'd)



NOTE:  $P_{DIR} = \text{High}$  for the mode parallel-in to serial-out. Parallel ready is an output flag from the FIFO indicating that a word can be loaded into the FIFO.

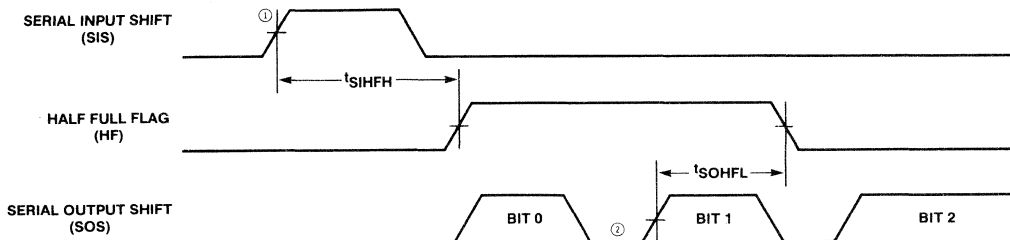
- ① FIFO is not full and ready for input.
- ② PS (In) is asserted, shifting in parallel data P0-8.  
PR (In) goes Low indicating parallel port is in use and no longer ready.  
PR (In) will remain Low as long as PS (In) remains High.
- ③ PS (In) has gone Low, allowing recent word to propagate through FIFO, PR (In) returns High when ready for more input.

Figure 5. Parallel Input Shift Timing



- ① for  $P_{DIR} = \text{High}$ , the direction is parallel-in to serial-out. After the 32nd shift-in, the half-full flag is set to High, and remains High, indicating the presence of 32 or more words.

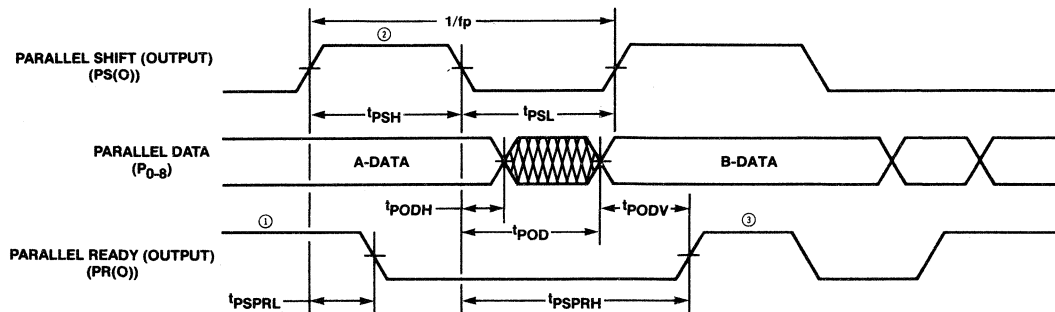
Figure 6. Half-full Flag Specifications on Parallel ( $t_{PSHFH}$ )



- ① When there are 31 words in the FIFO, the next shift-in on the 32nd word sets the half-full flag (HF) High indicating that there are 32 or more words.
- ② As soon as one word is partially shifted out, HF goes Low indicating there are less than 32 words.

Figure 7. Half-full Flag Specification on Serial Operation ( $t_{SIHFH}$ ,  $t_{SOHFL}$ )

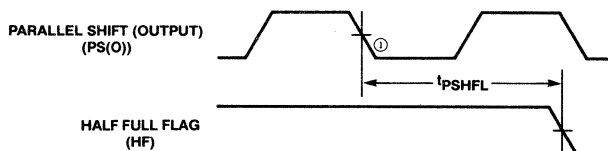
## Definition of Waveforms (cont'd)



NOTE: For above conditions  $P_{DIR} = \text{Low}$  indicating that the direction is from serial-in to parallel-out. Thus parallel ready indicates the output status.

- ① FIFO is not empty and at least one word is valid and ready at P0-8 outputs.
- ② PS (Out) is asserted, shifting out parallel data. Data remains valid, but: PR (Out) goes Low to indicate parallel port is in use and no longer ready. PR (Out) will remain Low as long as PS (Out) remains High.
- ③ PS (Out) has gone Low, allowing data word to be shifted out. Next data word appears at output and PR (Out) is asserted to indicate valid data ready.

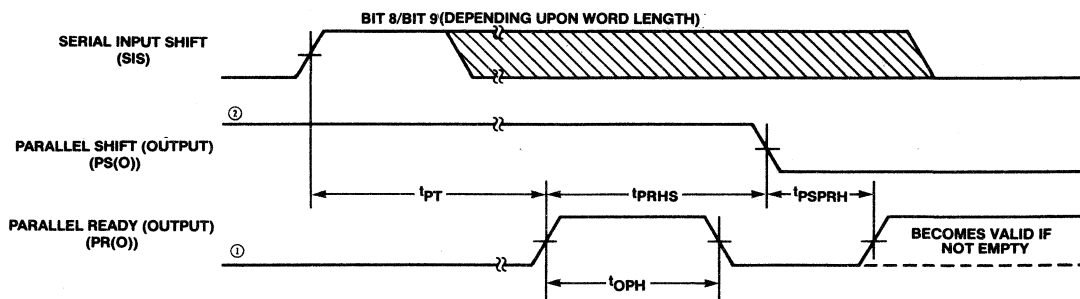
**Figure 8. Serial-in to Parallel-out Specifications ( $t_{POD}$ ,  $t_{PODH}$ ,  $t_{ODV}$ )**



NOTE: For  $P_{DIR} = \text{Low}$  the direction is serial-in to parallel-out.

- ① When a word is shifted out and the half-full flag goes Low, 31 words or less are in the FIFO.

**Figure 9. Half-full Flag Specification on Parallel Shift-out ( $t_{PSHFL}$ )**

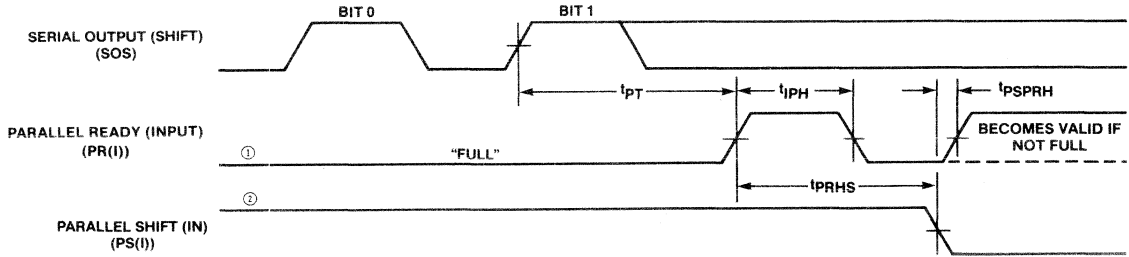


NOTE:  $P_{DIR} = \text{Low}$  indicating serial-in to parallel-out.

- ① FIFO initially empty.
- ② PS (Out) held High.

**Figure 10.  $t_{PSPRH}$ ,  $t_{PT}$ ,  $t_{OPH}$  Specifications (Serial Input Mode)**

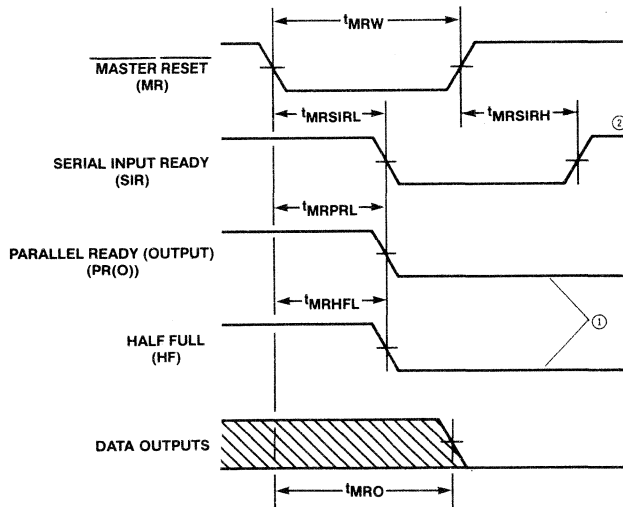
## Definition of Waveforms (cont'd)



NOTE:  $P_{DIR} = \text{High}$  (parallel-in to serial-out).

- ① FIFO is full.
- ② PS (I) held High.

Figure 11. Fall-through Specifications

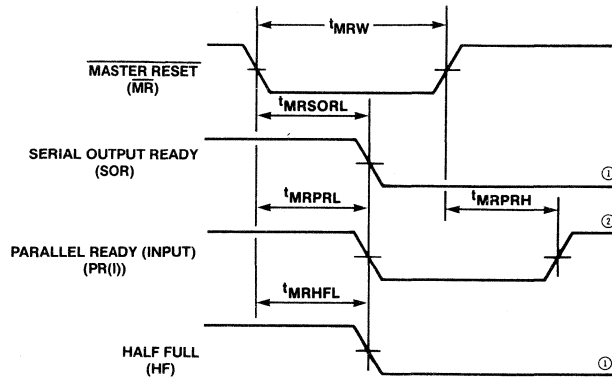


NOTE:  $P_{DIR} = \text{Low}$ .

- ① PR (O) and HF go Low.
- ② After  $\overline{MR}$  goes High, SIR goes High.

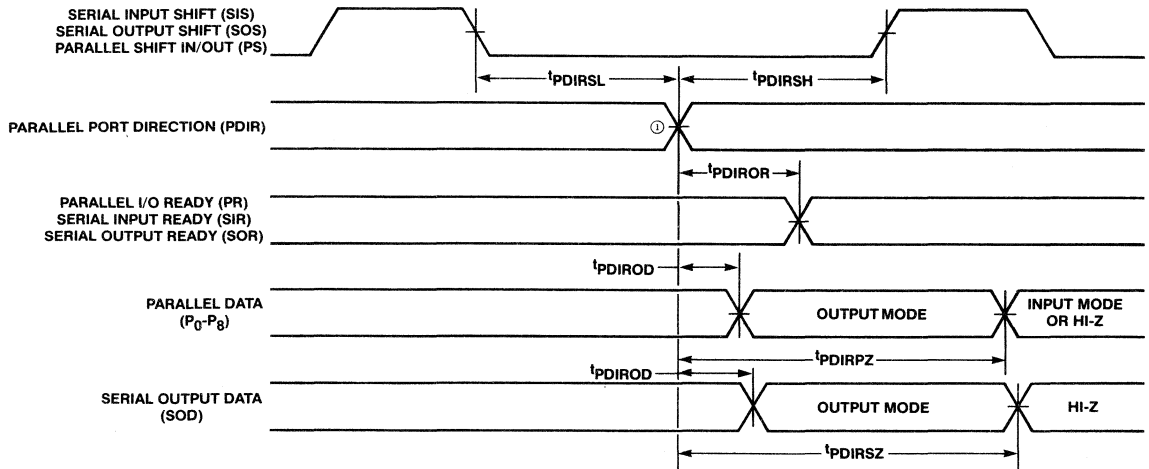
Figure 12. Master Reset Timing Serial-in to Parallel-out

## Definition of Waveforms (cont'd)



NOTE: PDIR = High.  
 ① SOR and HF go Low.  
 ② After MR goes High, PR(I) goes High.

Figure 13. Master Reset Timing (Parallel-in to Serial-out)



NOTE: When the FIFO is used as a stack, change the port direction before the FIFO is full; otherwise, data may be lost.

Figure 14. PDIR Transition Parameters

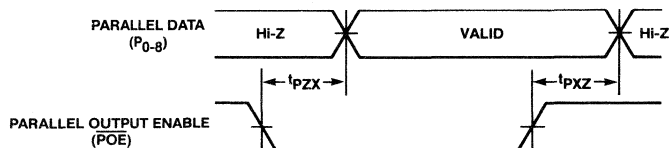


Figure 15. Parallel Port Enable and Disable Timing

## Definition of Waveforms (cont'd)

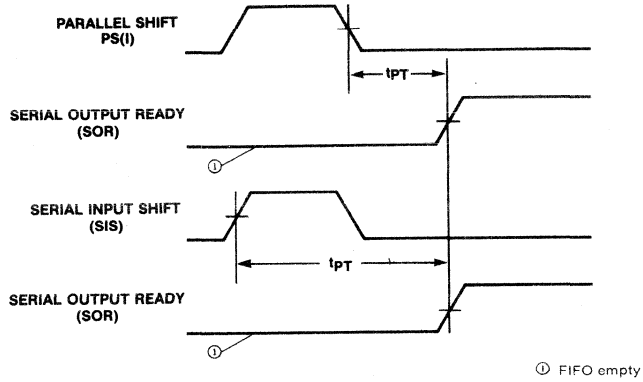


Figure 16.  $t_{PT}$  Specification (Shift-in to Serial Output Ready)

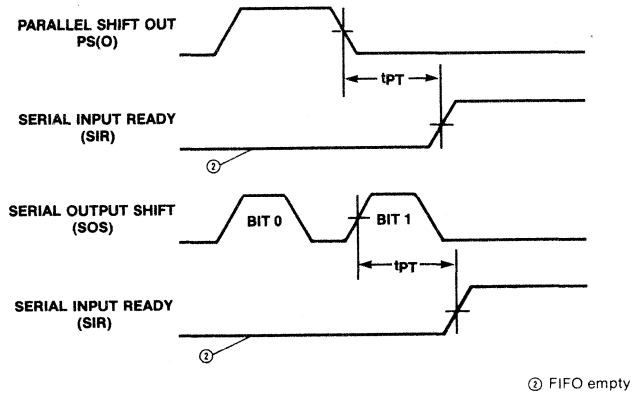
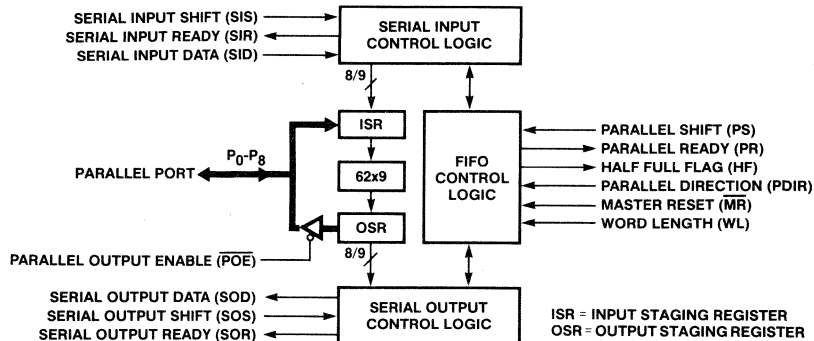


Figure 17.  $t_{PT}$  Specification (Shift-in to Serial Input Ready)

## Appendix Detailed Functional/Description for 67417

The 67417 is a serializing FIFO intended as a one-chip solution for data buffering and serializing/deserializing. It can be successfully used for interfacing parallel-format computing equipment to serial-format data communications and mass-memory equipment. The 67417 is a word-oriented device. It is meant to function with complete 8- or 9-bit words of data.



Basically the major internal subsystems of the 67417 are:

- (i) The serial input port
- (ii) The serial output port
- (iii) The parallel port
- (iv) The FIFO control logic and
- (v) The cell array

### Serial Port

The two serial ports (input and output) are entirely separate which allows a high-speed data rate of 28 MHz. These serial ports do not share data pins, control pins, or internal circuits. However, since the serial output data is a three-state output, the serial data ports could be connected together in the normal serial-parallel operation mode with separate SOR and SIR status signals.

The serial input port interface consists of the Serial Input Ready (SIR) output, Serial Input Data (SID) input, and the Serial Input Shift (SIS) clock input. Unlike the analogous SI and IR signals on the 67401/2, SIS and SIR do not accomplish a "handshake" with the rest of the logic of the system which incorporates the 67417; rather SIR is asserted whenever the 67417 is still capable of receiving at least one more bit. SIS is a positive edge-triggered input which sequences the serial input control logic. This logic in turn controls SIR and the 8/9-bit Input Staging Register (ISR).

The serial output port interface is the dual of the above, with a Serial Output Data (SOD) output, a Serial Output Shift (SOS) clock input, and a Serial Output Ready (SOR) status output. SOR is asserted whenever at least one more bit is available at the output. SOS is a positive edge-triggered input which sequences the 8/9-bit Output Staging Register (OSR). Serial Output Data is automatically three-stated whenever the serial output port is

### Parallel Port

This is a fully bidirectional port, and it operates at a more conservative data rate of 10 MHz. The input-staging register (ISR) internally controls the parallel input data port bus signals. Likewise the OSR internally controls the parallel output data port. The ISR data outputs drive the parallel data inputs to the cell array, and the OSR inputs are likewise driven by the final parallel data stage of the cell array

disabled (during Master Reset) and PDIR = Low. The parallel port is controlled by Parallel Shift (PS) input and Parallel Direction Input (PDIR). Parallel Ready (PR) is the handshake/status output. At the Parallel Port PS and PR do accomplish a handshake with the outside world as SI, IR, SO and OR on the 67401/2.

### Modes of Operation

There are three modes in which the 67417 can operate

- (i) Parallel-in to serial-out
- (ii) Serial-in to parallel-out and
- (iii) Serial-in to serial-out.

In the parallel-in to serial-out mode, PDIR = HIGH. Thus Parallel Shift (PS) acts as a Shift In (SI) and similarly, Parallel Ready (PR) as Input Ready (IR). The first bit shifted out of the serial port will be bit 0 of the parallel word input.

Similarly for serial-in to parallel-out mode, PDIR = LOW, and Parallel Shift (PS) acts as a Shift Out (SO) and Parallel Ready (PR) as Output Ready (OR). The first bit shifted into the serial port will be bit 0 of the parallel word output.

If the direction mode for a particular application of the 67417 is not intended to change during system operation, the PDIR input should be strapped to a logic LOW or HIGH.

In the serial-in to serial-out mode, PDIR = 10 V minimum.

The parallel port does not function during this mode and is three-stated. The direction operating mode should not be changed if the FIFO is FULL otherwise stored data will be lost.

### Cell Array

The 67417 cell array can function *either* as a 64x8 FIFO (with the 9th bit padded to a zero) or as a 64x9 FIFO, according to the setting of the word length (WL) control input. Like the PDIR

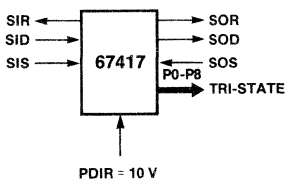


control input, WL can be switched at electronic speeds during system operations; but if the word length of a particular 67417 is *never* to change during system operation, WL for that part can be strapped to ground or  $V_{CC}$ .

It is a permissible 67417 mode of operation to almost fill the FIFO (there should be at least two empty locations) with WL set to 8-bit operation, then switch WL to 9-bit operation (WL = HIGH) to load one more word plus a frame marker in the last bit, and then switch PDIR and unload the 67417 in a 9-bit mode. This sequence of operations has the effect of providing a "frame marker bit" in the ninth bit of the last word loaded. The corresponding 9th bits will have been zeroed by the 67417 internal logic for all the other words in the frame since they were loaded while the 67417 was operating as an 8-bit device.

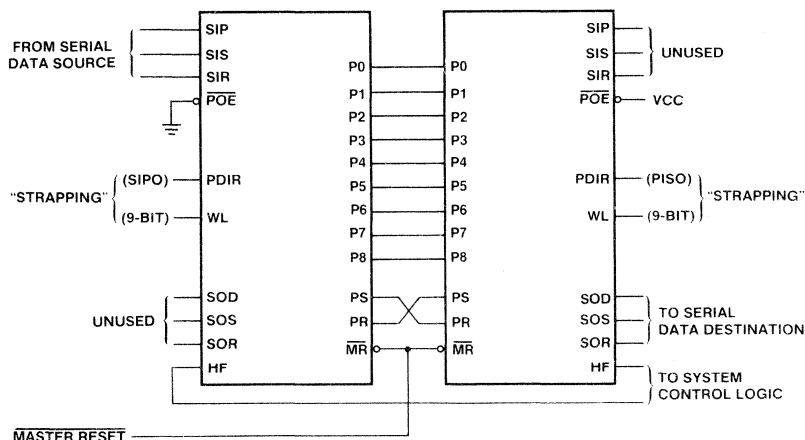
It is, however, the system designer's responsibility to avoid changing PDIR inputs when only part of an 8- or 9-bit word has been received or transmitted. In general, if such a change occurs, the part in general will try to add zero bits to pad out the impacted word to assume full length.

## Applications



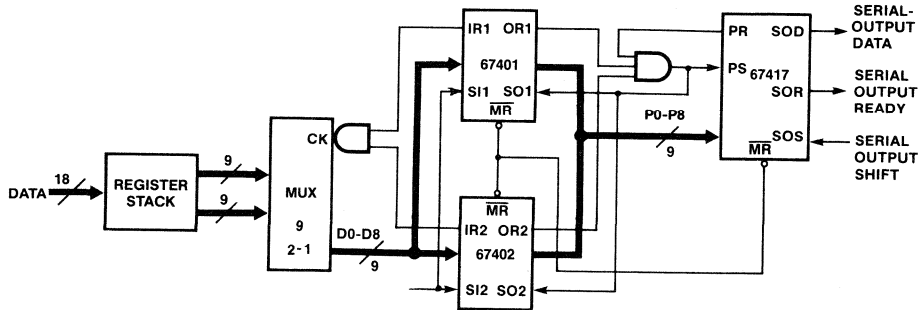
NOTE: It can shift in data serially in the multiples of 8- or 9-bit according to WL.

Figure 18. 512/576x1 Serial-in to Serial-out Mode



\* SIPO = Serial-in to Parallel-out.  
\*\* PISO = Parallel-in to Serial-out.

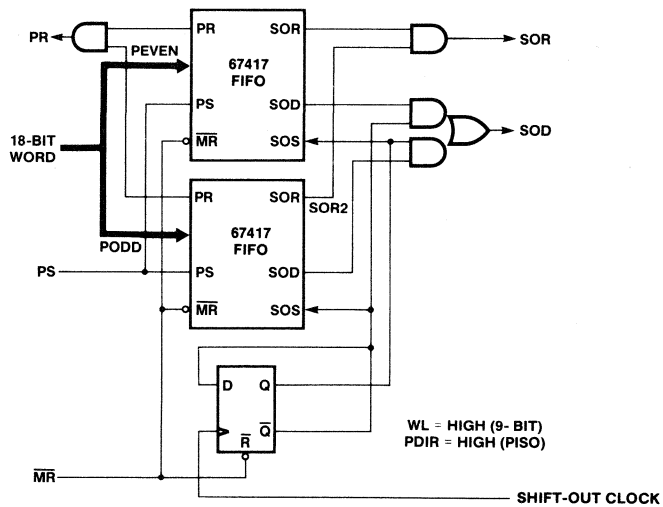
Figure 19. Cascading of Two 'S417s for Serial-in to Serial-out Operation as a 128x9 (1152x1) FIFO



**Figure 20. An Example of an Expansion Scheme for a 64x18 Parallel-to-Serial FIFO**

An 18-bit data word is multiplexed into the two 67401/2 FIFOs. Since the 67417 FIFO is cascadable at the parallel port only, two

67401/2 FIFOs were used along with the 67417 to obtain the appropriate organization.



**Figure 21. Another Example of an Expansion Scheme for a 64x18 Parallel-in to Serial-out FIFO**  
Two 67417 FIFOs Are Used to Implement a 64x18 Parallel-in to Serial-out FIFO

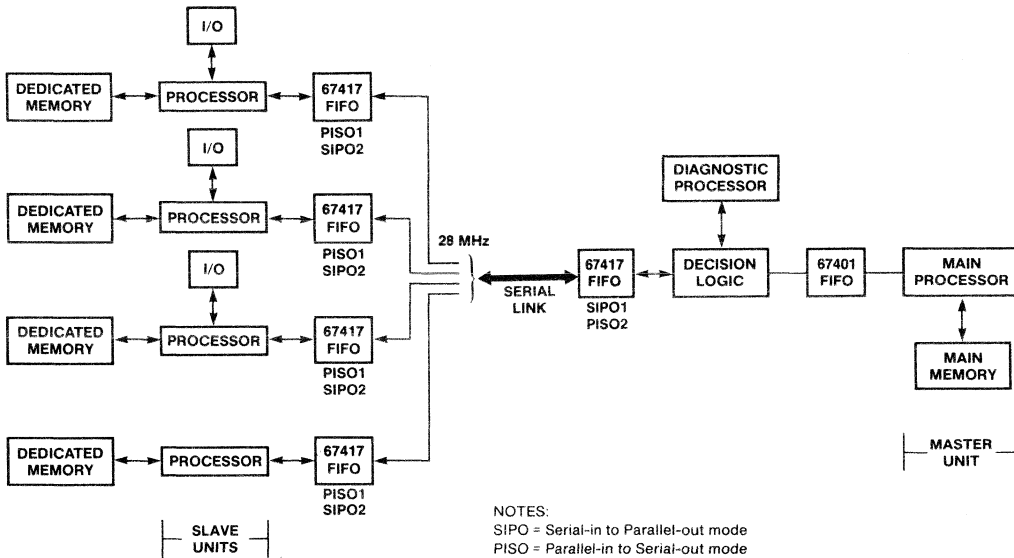


Figure 22. A Multiprocessing System

Each processor unit on the left has its own communication interface which consists of a serializing FIFO. The serial data link can operate in either direction 1 or direction 2 which is decided by the Decision logic. In direction 1 either of the slave units send the data to the master over the serial link, with its respective 67417 operating in parallel-in to serial-out mode (PISO1). While

the 67417 for the master unit operates in serial-in to parallel-out mode (SIPO1). The direction 2 has the FIFOs (67417) operating in the reverse direction from the above case. Decision logic determines the priority of the slave processors to use the serial link.

# 674219

## FIFO RAM Controller

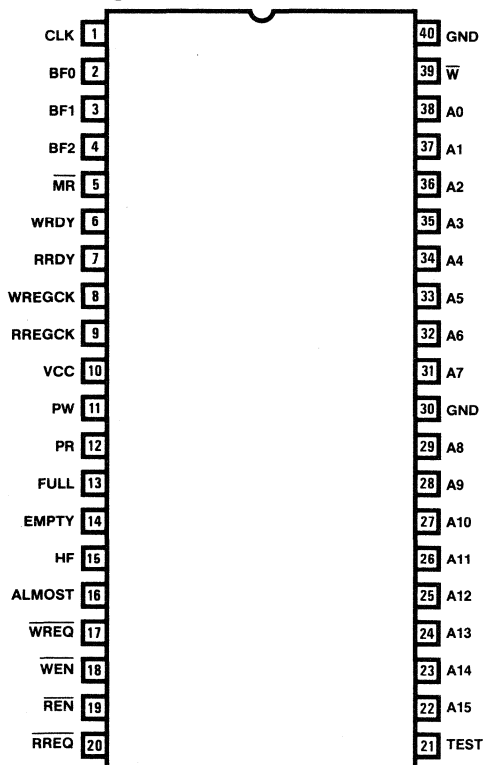
### Features/Benefits

- High-speed, no fall-through time
- Deep FIFOs—16-bit SRAM address
- Arbitration read/write
- Control signals for data latching
- Full, Half-Full, Empty, Almost flags for buffer sizes from 512 to 64 K
- Three-state outputs

### Applications

- LAN equipment
- Data communication
- Disk/tape controllers
- Host-to-dedicated-processor interface

### Pin Configuration



### Ordering Information

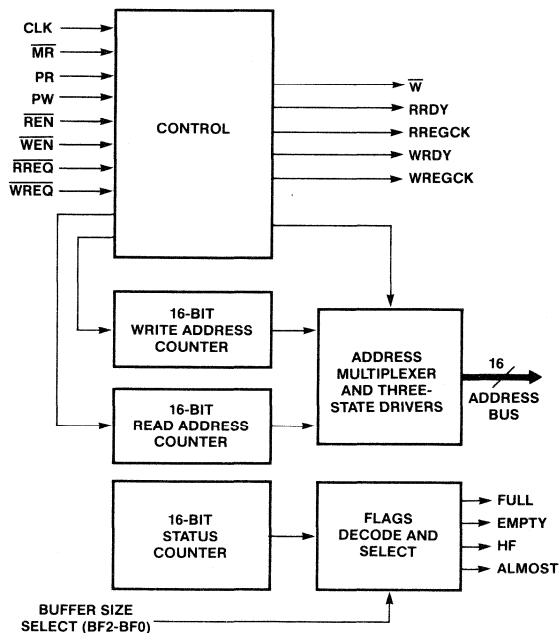
Part Number	Package		Temperature
	Pins	Type	
674219	40	CD 040	Com

### Description

The 674219 FIFO RAM Controller provides addressing control, status, and arbitration for a static RAM array used as a First-In-First-Out (FIFO) buffer. The sixteen address lines can address a FIFO buffer area ranging from 512 to 65,536 static RAM words. Control signals including W (the write enable signal for the static RAMs), handshaking signals for the read and write ports, and strobes for external data latching.

The 674219 allows single-port static RAMs to resolve read and write request conflicts according to priority rules selected via the Priority-on-Read (PR) and Priority-on-Write (PW) inputs. If priority is given to either port, or if only one port is used, the maximum data rate through that port is 10 MHz.

### Block Diagram



## Definition of Terms

**LATCHED** A request has been received by the 674219 on one of its ports. The request has been internally latched, but not sampled.

**SAMPLED** The state of a latched request when it has been internally synchronized.

**PROCESSED** A decision to perform a sampled request.

**PERFORMED** When the processed request is executed as a memory cycle.

**PENDING REQUEST** A sampled request that has been held until the FIFO completes its current operation(s).

**WRITE DATA PORT** The register(s) where the system places the data that is to be written into the FIFO.

**READ DATA PORT** The register(s) where the system reads the FIFO data.

**WRITE DATA REGISTER** The register(s) which serves as the data input to the FIFO.

**READ DATA REGISTER** The register(s) where the FIFO leaves the read data for the system to take.

## Architecture

The 674219 FIFO RAM Controller, together with an array of static RAMs and two registers, comprises a First-In-First-Out (FIFO) memory. (See Figure 1.)

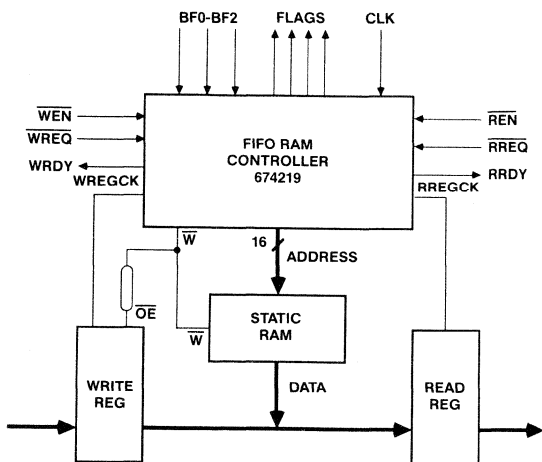


Figure 1. 57/674219 In and Implementation of a FIFO Buffer

The 674219 provides addresses and control signals to the static RAMs, and interfaces with the system via a write port, a read port, and status flags. The 674219 includes three 16-bit counters: a write-address counter, a read-address counter, and a status counter. The status flags are generated as a function of the state of the status counter and the buffer length selected. The write port has a Write REQuest (WREQ) input, a Write ENable (WEN) input, and a Write ReaDY (WRDY) output. The read port has a Read REQuest (RREQ) input, a Read ENable (REN) input, and a

Read ReaDY (RRDY) output. Two priority-control inputs, Priority-on-Write (PW) and Priority-on-Read (PR), determine the priority rules by which the 674219 arbitrates between simultaneous read and write requests. The 674219 provides two clock signals (RREGCK, WREGCK) to the Read Data Register and the Write Data Register, as well as a Write signal (W) to be connected to the Write Enable (WE) inputs of the static RAMs. Sixteen address outputs provide the read and write addresses to the static RAMs. When both REN and WEN are HIGH, the address outputs go into high-impedance (Hi-Z) state, so that the static RAMs can be accessed externally.

A Master Reset ( $\overline{MR}$ ) input allows initializing the part by clearing the three counters and presetting the flags. (See Table 1.)

FLAG	CONDITION
Empty	High
Full	Low
Almost	High
Half	Low

Table 1. Condition of Flags After Master Reset

## Pin Definitions

**VCC** 5.0 V  $\pm$  10%

**GND** Ground

**CLK** CLOCK—Controls synchronous operation of the device. All requests are sampled internally on every other LOW-to-HIGH transition of the clock. These transitions are called sampling clock edges. The first sampling clock edge is the first LOW-to-HIGH transition of the clock after master reset.

**BF2-BF0** BUFFER SIZE CONTROLS—Determine the desired buffer size. (See Table 3.) Setting the buffer size is essential for correct operation of the status flags.

**MR** MASTER RESET—Clears all counters when LOW. The first LOW-to-HIGH transition of the clock, following a LOW-going Master Reset pulse, is the first sampling clock edge; the first request to be serviced is a write request. (See Figure 7.)

**A15-A0** ADDRESS OUTPUTS—Three-state outputs which provide a read address when  $\overline{W}$  is HIGH, or a write address when  $\overline{W}$  is LOW. A15-A0 are in the Hi-Z state only when both  $\overline{REN}$  and WEN are HIGH.

**TEST** An input used during manufacturing final test. For normal operation, TEST should be tied to GND.

**W** WRITE CONTROL—Used to control the SRAM arrays Write Enable pin and to output enable the write data register.

**WREQ** WRITE REQUEST—A LOW-going pulse on this pin requests a write to the FIFO. A write request can only be latched if the write port is enabled ( $\overline{WEN}$  is LOW), and the previous write request has been processed (WRDY is HIGH).

**RREQ** READ REQUEST—A LOW-going pulse on this pin requests a read from the FIFO. A read request can only be latched if the read port is enabled ( $\overline{REN}$  is LOW), and the previous read request has been processed (RRDY is HIGH).

**WEN** WRITE ENABLE—When this input is HIGH, all write requests are ignored. When  $\overline{WEN}$  is LOW and WRDY is HIGH, a write request ( $\overline{WREQ}$  = LOW-going pulse) will be latched by the 674219. If both  $\overline{WEN}$  and  $\overline{REN}$  are HIGH, the address outputs A15-A0 go into the Hi-Z state, permitting external access to the SRAM array.

**REN** READ ENABLE—When this input is HIGH, all read requests are ignored. When  $\overline{REN}$  is LOW and RRDY is HIGH, a read request ( $\overline{RREQ}$  = LOW-going pulse) will be latched by the 674219. If both  $\overline{WEN}$  and  $\overline{REN}$  are HIGH, the address outputs A15-A0 go into the Hi-Z state, permitting external access to the SRAM array.

**PW, PR** WRITE PRIORITY and READ PRIORITY—These two inputs determine the rules governing the arbitration between write and read requests. (See Table 2.) *These inputs must not both be HIGH simultaneously.*

**WRDY** WRITE READY—When this output is HIGH, and  $\overline{WEN}$  is LOW, a write request may be sent to the  $\overline{WREQ}$  pin.

WRDY goes LOW on the sampling clock edge which samples the write request. WRDY will go HIGH on the non-sampling clock edge which starts the write cycle. WRDY will stay LOW if the FIFO is full.

Write requests should be made only when WRDY is HIGH.

**RRDY** READ READY—When this output is HIGH, and  $\overline{REN}$  is LOW, a read request may be sent to the  $\overline{RREQ}$  pin.

RRDY goes LOW on the sampling clock edge which samples the read request. RRDY will go HIGH on the non-sampling clock edge which starts the read cycle. RRDY will stay LOW if the FIFO is empty.

Read requests should be made only when RRDY is HIGH.

**WREGCK** WRITE REGISTER CLOCK—This output is used to clock the write data register.

**RREGCK** READ REGISTER CLOCK—This output is used to clock the read data register.

**EMPTY** EMPTY FLAG—When HIGH, indicates that the FIFO is empty. Read requests are not permitted when the FIFO is EMPTY.

**FULL** FULL FLAG—When HIGH, indicates that the FIFO is full. Write requests are not permitted when the FIFO is FULL.

**HF** HALF-FULL FLAG—When HIGH, indicates that the FIFO has half, or more, of its locations occupied.

**ALMOST** ALMOST FLAG—When HIGH, indicates that one of the following conditions exists:

1. The FIFO is almost empty (less than sixteen words in the FIFO), if ALMOST is HIGH and HF is LOW.
2. The FIFO is almost full (sixteen or less locations are available) if ALMOST is HIGH and HF is HIGH.

## Requests, Arbitration and Data Capture

A clock, supplied via the CLK input of the 57/674219, generates the internal sequence of events which constitutes a single FIFO operation. The read and write ports recognize and latch read and write requests asynchronously, provided that the respective enable ( $\overline{REN}$  or  $\overline{WEN}$ ) is LOW, and the request window setup time is observed.

The FIFO write operation is as follows (see Figure 2):

**Stage 1** A write request is sent to the 674219 by a LOW-going pulse on the  $\overline{WREQ}$  pin.

**Stage 2** The write request is latched internally, asynchronous to the clock.

**Stage 3** WRDY goes LOW on the sampling clock edge that latched the request to indicate to the system that the request has been latched and synchronized internally. WRDY also indicates to the system that the write port is no longer accepting write requests. In order to guarantee that a request is properly synchronized, the request must not occur during the window stated by the tWRQC specifications.

**Stage 4a** Regardless of whether the write cycle is started or not, WREGCK will go HIGH for one clock cycle on the non-sampling clock edge that follows WRDY going LOW. The transition from LOW-to-HIGH on the WREGCK pin clocks data into the write data port, reading the data for writing to the SRAM.

**Stage 4b** A decision to wait, or to perform the write cycle is made based on the following:

**Case 1** If read priority is set, the 674219 will process all pending read requests first. The write cycle will be delayed until all of the read cycles have been performed. Then, and only then, will the pending write cycle be performed.

**Case 2** If write priority is set, regardless if there is a pending read request or not, the write cycle will start on the next non-sampling clock edge that follows WRDY going LOW. If there was a pending read request, the read cycle will not be started until the write cycle has been completed.

**Case 3** If no priority is set, and there is no pending read request, the FRC will start the write cycle on the next non-sampling clock edge that follows WRDY going LOW.

**Case 4** If no priority is set, and there are simultaneous requests (i.e., a read request and a write request have both been latched before the same sampling clock edge), the FIFO will decide which is to be processed first according to the following:

If the last case of simultaneous requests (with no priority) performed a read cycle first, the write request will be processed first, followed by the read request.

If the last case of simultaneous requests (with no priority) performed a write cycle first, the read request will be processed first, followed by the write request.

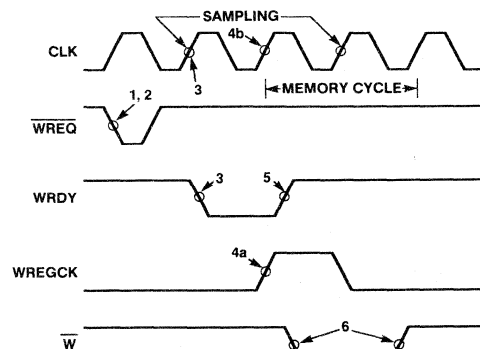


Figure 2. The Stages of a FIFO Write Operation

**Stage 5** WRDY will go HIGH on the non-sampling edge that starts the write cycle.

**Stage 6** Once a request has been granted, the memory cycle takes place over two clock cycles, starting with the non-sampling clock edge on which the request is granted (WRDY going from LOW-to-HIGH). The Write line ( $\bar{W}$ ) goes LOW at tCWL after the clock edge starting the memory cycle and stays low until tCWH after the clock edge terminating the memory cycle.

**The FIFO read operation is as follows** (see Figure 3):

**Stage 1** A read request is sent to the 674219 by a LOW-going pulse on the RREQ pin.

**Stage 2** The read request is latched internally, asynchronous to the clock.

**Stage 3** RRDY goes LOW on the sampling clock edge that latched the request to indicate to the system that the request has been latched and synchronized internally. RRDY also indicates to the system that the read port is no longer accepting read requests. In order to guarantee that a request is properly synchronized, the request must not occur during the window stated by the tRRQC specifications.

**Stage 4** A decision to wait, or to perform the read cycle is made based on the following:

**Case 1** If write priority is set, the 674219 will process all pending write requests first. The read cycle will be delayed until all of the write cycles have been performed. Then, and only then, will the pending read cycle be performed.

**Case 2** If read priority is set, regardless if there is a pending write request or not, the read cycle will start on the next non-sampling clock edge that follows RRDY going LOW. If there was a pending write request, the write cycle will not be started until the read cycle has been completed.

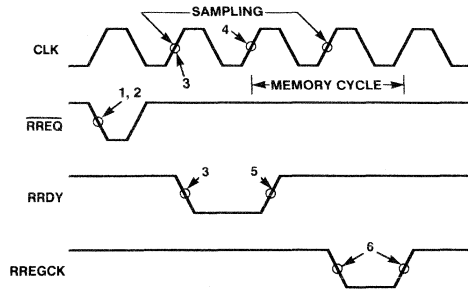
**Case 3** If no priority is set, and there is no pending write request, the FRC will start the read cycle on the next non-sampling clock edge that follows RRDY going LOW.

**Case 4** If no priority is set, and there are simultaneous requests (i.e., a read request and a write request have both been latched before the same sampling clock edge), the FIFO will decide which is to be processed first according to the following:

1. If the last case of simultaneous requests (with no priority) performed a read cycle first, the write request will be processed first, followed by the read request.
2. If the last case of simultaneous requests (with no priority) performed a write cycle first, the read request will be processed first, followed by the write request.

**Stage 5** RRDY will go HIGH on the non-sampling edge that starts the write cycle.

**Stage 6** Once a request has been granted, the memory cycle takes place over two clock cycles, starting with the non-sampling clock edge on which the request is granted (RRDY going from LOW-to-HIGH). Read REGISTER Clock (RREGCK) goes LOW for one clock cycle, starting with the sampling edge that occurred within the read memory cycle. RREGCK clocks data from the SRAM array to the read data port on the LOW-to-HIGH transition, which terminates the read cycle.



**Figure 3. The Stages of a FIFO Read Operation**

## Priority

Two input signals, Priority-on Read (PR) and Priority -on-Write (PW), determine the arbitration rule which sequences the read and write cycles, for various cases as follows: (see Table 2):

PW	PR	PRIORITY
0	0	No priority
0	1	Priority on READ
1	0	Priority on WRITE
1	1	(Not allowed)

**Table 2. Priority Encoding**

### No-Priority Case

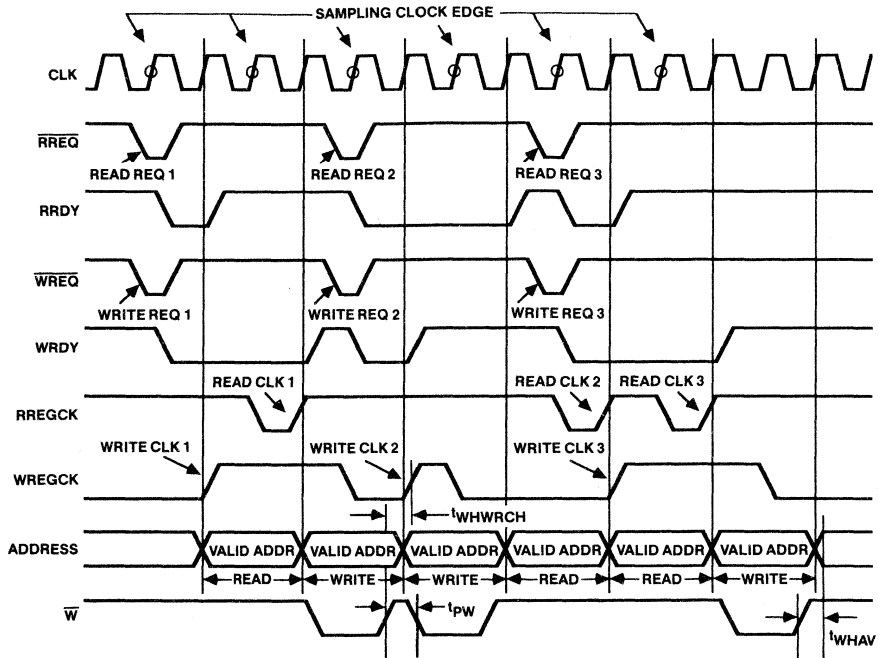
If no priority is selected (PR = PW = LOW), each request is processed in the order it came into the FRC.

If no priority is set and both a read and write request are latched before the same sampling clock edge, the 674219 will perform read and write cycles alternately. (See Figure 4.)

### Write Priority Case

If write priority is selected (PR = LOW, PW = HIGH) write requests are always processed before read requests (assuming that the requests meet the setup time).

If write priority is set and both a read and write request are latched before the same sampling clock edge, (i.e., a simultaneous request), the write cycle will take place first. If, before the next sampling clock edge, another write request is latched, another write cycle will take place, and the pending read request will not be processed. Only when the sampling clock edge encounters no further write requests will the pending read request be processed. At this time the read cycle will start and the RRDY output will go HIGH. (See Figure 5.)



- Notes: 1. Assumes not at FULL and not at EMPTY.  
 2. Assumes last case of simultaneous requests processed a write first.

Figure 4. Operation With No Priority

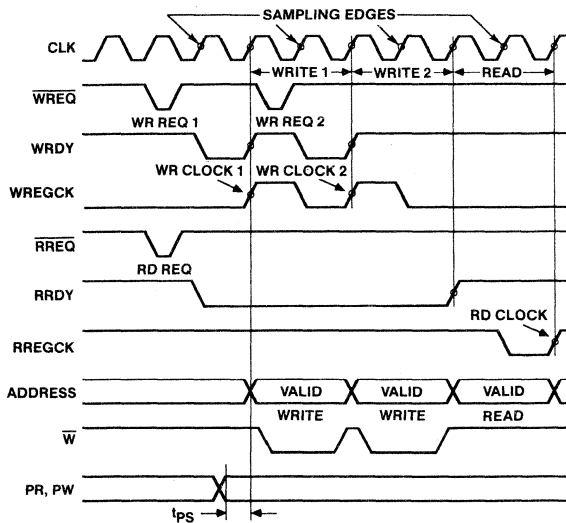


Figure 5. Operation With Write Priority



## Read Priority Case

If read priority is selected (PR = HIGH, PW = LOW) read requests are always processed before write requests assuming that the requests meet the setup time).

If read priority is set and both a read and write request are latched before the same sampling clock edge, (i.e., a simultaneous request), the read cycle will take place first. If, before the next sampling clock edge, another read request is latched, another read cycle will take place and the pending write request will not be processed. Only when the sampling clock edge encounters no further read requests will the pending write requests be processed. At this time, the write cycle will start and the WRDY output will go HIGH. (See Figure 6.)

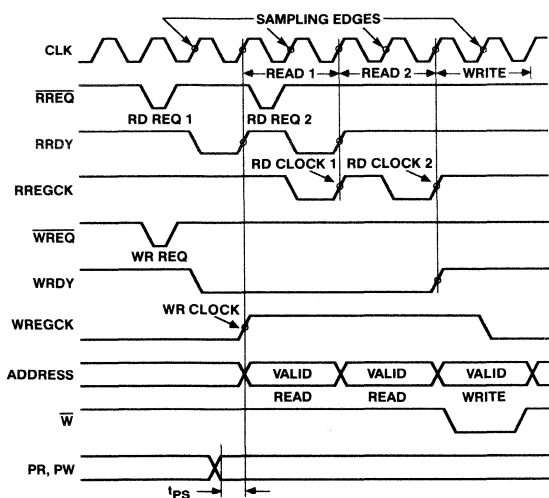


Figure 6. Operation With Read Priority

## Buffer Length

A three-bit input control field, BF2-0, selects the buffer length ("depth") of the FIFO. Any power of 2 from 512 to 65,536 may be chosen as the buffer length. (See Table 3.)

BF2	BF1	BF0	BUFFER SIZE
0	0	0	512
0	0	1	1024
0	1	0	2048
0	1	1	4096
1	0	0	8192
1	0	1	16384
1	1	0	32768
1	1	1	65536

Table 3. Buffer Length

## Status Flags

The flags are generated as a function of the buffer length, selected via inputs BF2-BF0, and the state of the status counter. The status flags are:

**EMPTY** When HIGH, the EMPTY flag indicates that the FIFO is empty. The EMPTY flag goes HIGH on the first sampling clock edge during the memory cycle which empties out the FIFO.

**FULL** When HIGH, the FULL flag indicates that the FIFO is full, and no more data can be written into it until a read cycle takes place. The FULL flag goes HIGH on the first sampling clock edge during the memory write cycle which fills up the FIFO.

**HF** When HIGH, the Half-Full flag indicates that the FIFO is filled to half its depth, or more.

**ALMOST** When HIGH, the ALMOST flag indicates that one of the following conditions exists:

1. The FIFO is almost empty (less than sixteen words in the FIFO), if ALMOST is HIGH and HF is LOW.
2. The FIFO is almost full (sixteen or less locations are available) if ALMOST is HIGH and HF is HIGH.

The flags Master Reset to the states shown in Table 1.

## First Write Cycle (After a Master Reset or When FIFO is Empty)

The first LOW-to-HIGH clock edge, following Master Reset ( $\overline{MR}$ ) going LOW-to-HIGH, is the first sampling clock edge. The sampling clock edge occurs every other positive-going transition of the clock. The LOW pulse on  $\overline{MR}$  clears the three internal 16-bit counters (status, read and write). The FIFO is set to the EMPTY state, and no read requests are allowed (RRDY = LOW).

After an interval of at least  $t_{MRS}$  after  $\overline{MR}$  goes HIGH, a LOW-going pulse on the WREQ pin tells the 674219 that a write to the FIFO is requested. The write request is latched by the write port, provided that  $\overline{WEN}$  is LOW. (See Figure 7.) The following sampling clock edge samples the request, and causes WRDY to go LOW. WRDY goes HIGH again on the next (non-sampling) positive clock edge, regardless of priority. The write cycle takes place over two clock periods, starting on the positive non-sampling clock edge following the sampling clock edge which brought WRDY HIGH. The data is clocked into the external Write Data Register on the same non-sampling clock edge, and into the external Read Data Register on the second sampling clock edge, to allow minimal fall-through time. (See again Figure 7.) EMPTY will go LOW to indicate that there is valid data in the FIFO. RRDY goes HIGH indicating that there is data to be read from the FIFO. The same sequence of events occurs for the first write request that is initiated when the FIFO is empty.

## Methodology for Reading

In order to maintain a consistent system level architecture, the 674219 has been constructed such that the system should read the data port *before* a read request is sent. (See Figure 8.)

This ability allows the FIFO a zero fall-through time on all cycles. The system is able to get the data from the FIFO right away, without having to wait for the FRC to perform a read cycle of the SRAMs.

On the read port, a positive-going edge of RREGCK signals to the system that the read data register is being updated. The system should read the data first and then send a request to obtain the next word from memory to the read data register.

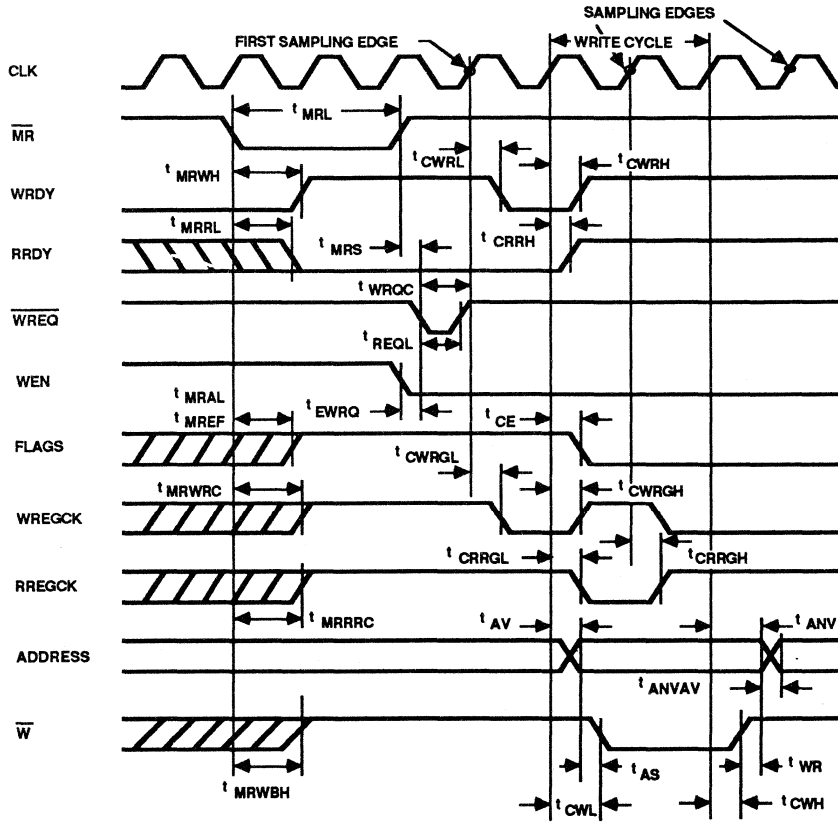


Figure 7. First Write After Master Reset or When FIFO Is Empty

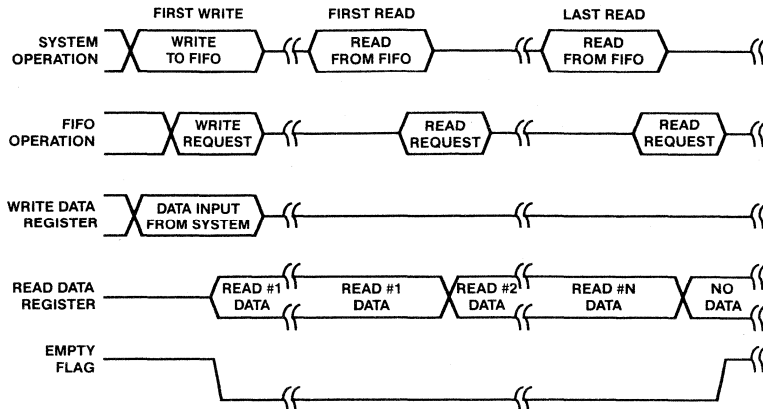


Figure 8. Methodology for Reading From the FIFO

## Write Cycle (Figure 9)

A write request, indicated by a LOW-going pulse on the  $\overline{WREQ}$  pin, is latched by the 674219, provided that  $\overline{WEN}$  is LOW and WRDY is HIGH. The request is sampled internally on the sampling clock edge. WRDY goes LOW on the same sampling clock edge, to indicate to the system that a write request has been latched and synchronized internally. In addition, WREGCK will go HIGH for one clock cycle on the non-sampling clock edge that follows WRDY going LOW, regardless of whether the write request is processed. The write request will be processed only if one of the following sets of conditions is true:

1. Write Priority has been selected.

If write priority has been selected, the FRC will process all write requests before any pending read requests.

2. No read request has been latched.

If no read request has been latched, regardless of priority, the FRC will process the write request immediately and will start the write memory cycle on the non-sampling clock edge that follows WRDY going LOW.

3. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the read request first.

In this case, the 674219 will process the write request first, and then process the read request.

4. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the write request first.

In this case the 674219 will process the read request first, and then process the write request.

Once the write request has been processed, a write cycle takes place over two clock cycles starting with the non-sampling clock edge on which WRDY goes HIGH.  $\overline{W}$  will go LOW,  $t_{CWL}$  after the start of the write cycle.  $\overline{W}$  is used to Write Enable the SRAM array and to Output Enable the write data register. Two clocks later ( $t_{CWH}$ )  $\overline{W}$  will go HIGH again, terminating the write cycle.

In order to avoid the bus contention inherent in shared-I/O memory systems, a delay line and an OR gate may be required (see Memory Interface Design Guidelines).

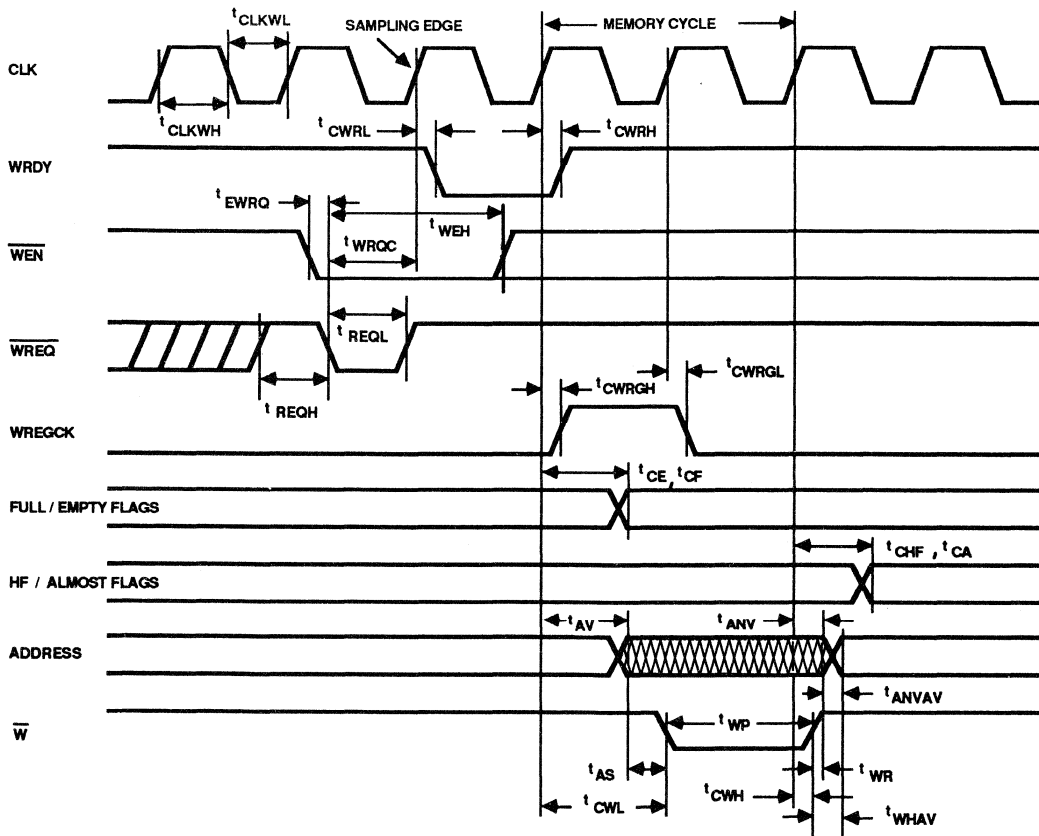


Figure 9. Write Cycle Timing

## Read Cycle (Figure 10)

A read request, indicated by a LOW-going pulse on the  $\overline{\text{RREQ}}$  pin, is latched by the 674219, provided that  $\overline{\text{REN}}$  is LOW and  $\text{RRDY}$  is HIGH. The request is sampled internally on the sampling clock edge.  $\text{RRDY}$  goes LOW on the same sampling clock edge to indicate to the system that a read request has been latched and synchronized internally. The read request is processed only if one of the following sets of conditions is true:

1. Read Priority has been selected.

If read priority has been selected, the FRC will process all read requests before any pending write request.

2. No write request has been latched.

If no write request has been latched, regardless of priority, the FRC will process the read request immediately and will start the read memory cycle on the non-sampling clock edge that follows  $\text{RRDY}$  going LOW.

3. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous

request), and in the last case of a simultaneous request, the FRC processed the write request first.

In this case, the 674219 will process the read request first.

4. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the read request first.

In this case, the 674219 will process the write request first, and then process the read request.

Once the read request has been processed, a read cycle takes place over two clock cycles starting with the non-sampling clock edge on which the  $\text{RRDY}$  goes HIGH.  $\text{RREGCK}$  goes LOW on the next sampling clock edge, stays LOW for one clock cycle, and goes HIGH on the following non-sampling clock edge, thus clocking the data which appears at the SRAM array's data outputs into the Read Data Register.  $\text{RREGCK}$  going HIGH terminates the read cycle.

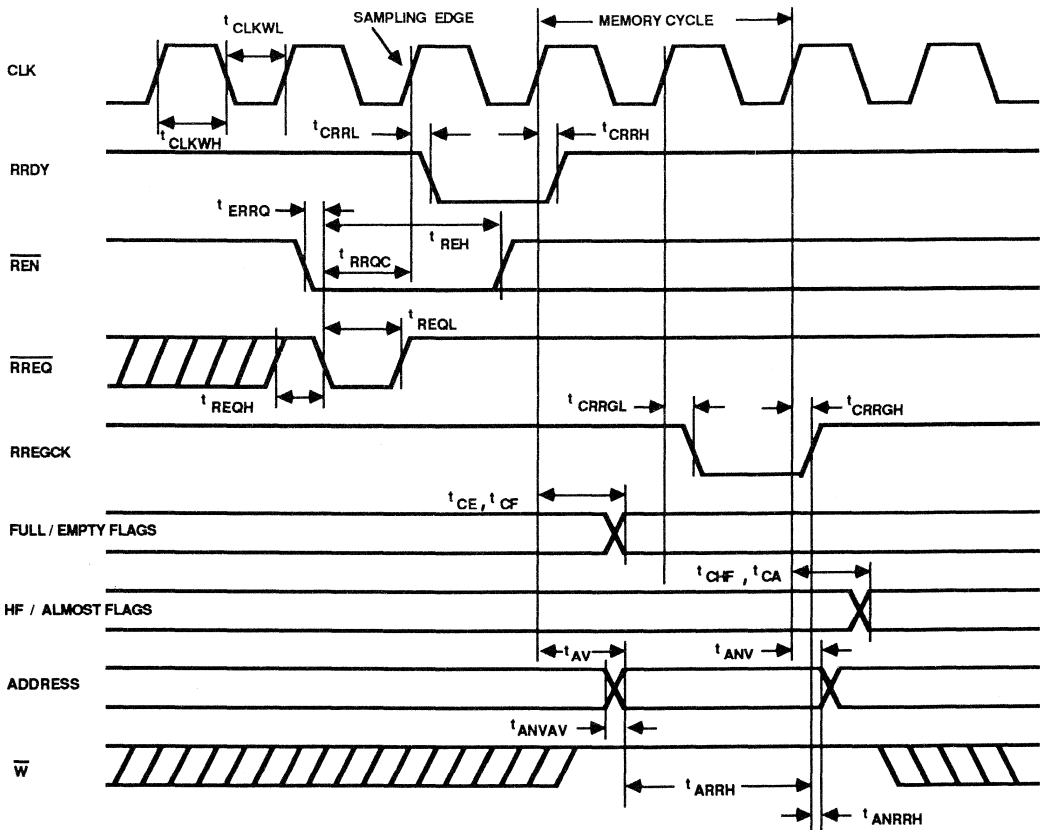


Figure 10. Read Cycle Timing

# Memory Interface Design Guidelines

## Introduction

The purpose of the memory interface design guideline is to aid the engineer in interfacing the 674219 FIFO RAM Controller (FRC) to an array of static RAMs. This guideline will be broken down into three separate sections. The first section is a timing analysis of the read cycle. The second section is a timing analysis of the write cycle. The final section will guide the designer through a real design.

Figure 11 shows a typical SRAM interface schematic.

## Section One: Read Cycle Timing Analysis

Figure 12 shows the basic timings which are critical to the read cycle. Some of these parameters apply to the FRC, some to the SRAM array, and others to external logic. For convenience, these parameters are broken up below:

### FRC Parameters:

$t_{AV}$  Clock to Address Valid Time  
 $t_{ANV}$  Clock to Address Not Valid Time

### SRAM Parameters

$t_{RC}$  Read Cycle Time  
 $t_{ACS}$  Chip Select Access Time  
 $t_{AA}$  Address Access Time  
 $t_{OH}$  Output Data Hold Time from Address Change  
 $t_{HZ}$  Chip Deselect to Output in High-Z

### External Logic:

#### Chip Select Decoder Parameters:

$t_{DECODE}$   $t_{PD}$  through Decoder

#### Read Data Register Parameters:

$t_S$  Data Setup Time  
 $t_H$  Data Hold Time

### Other Parameters (See Text):

$t_{RDREGH}$  Clock to RDCLK High [RDCLK is the clock input of the Read Data Register]

(This parameter is normally  $t_{CORRGH}$  of the FRC)

There are six separate equations which must each be met in order to determine what speed of SRAM the designer will need. It is assumed that the user has already specified a speed of operation and the external components needed. The equations listed can be used at any frequency, up to a maximum of a 20-MHz clock rate.

Since every read cycle consists of two physical clock cycles, all equations are with respect to  $2T$  ( $2 \times$  Cycle Time).

The first equation which should be satisfied is the read cycle time ( $t_{RC}$ ). This identifies what speed SRAM is required. The equation is based on the total time that the address is valid minus the decoder time. Since the decoder has some minimum skew on the negating edge, this time is ADDED to the equation. The equation thus becomes:

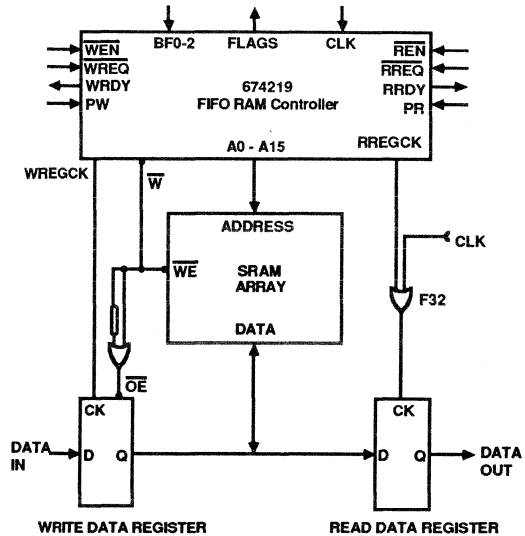


Figure 11. A Typical SRAM Interface

### Equation 1-1

$$t_{RC} \leq 2T - t_{DECODE(max)} + t_{DECODE(min)} - t_{ANVAV(max)}$$

The access time must be looked at next. There are actually two separate equations that help determine the access time.

Equation 1-2 determines the address access time ( $t_{AA}$ ).  $t_{AA}$  is based on the time that the address is valid before the read register gets clocked. The equation takes into account the setup time of the read data register ( $t_S$ ) as well. The equation is:

### Equation 1-2

$$t_{AA} \leq 2T - \text{MAX}(t_{AV} - t_{RDREGH}) - t_S(\min)$$

Where  $\text{MAX}(t_{AV} - t_{RDREGH})$  is the maximum difference between  $t_{AV}$  and  $t_{RDREGH}$

Equation 1-3 determines the chip select access time ( $t_{ACS}$ ). This time is based on the time the address is valid before the read register gets clocked MINUS the maximum skew through the chip select decoder. This is done to ensure that the decoder delay is taken into consideration. Again, the read register setup time is considered. The modified equation thus becomes:

### Equation 1-3

$$t_{ACS} \leq 2T - t_{DECODE(max)} - \text{MAX}(t_{AV} - t_{RDREGH}) - t_S(\min)$$

Where  $\text{MAX}(t_{AV} - t_{RDREGH})$  is the maximum difference between  $t_{AV}$  and  $t_{RDREGH}$

The next two equations take into consideration the read data hold time with respect to the address ( $t_{OH}$ ), and the chip deselect to data outputs in High-Z time ( $t_{HZ}$ ). We will consider the more critical  $t_{OH}$ .  $t_{OH}$  can easily be determined by comparing the data hold time PLUS the clock to address not valid ( $t_{ANV}$ ) time with the sum of the clock to RDCLK HIGH time ( $t_{RDREGH}$ ) and the data register hold time ( $t_H$ ). The equation for this becomes:

**Equation 1-4**

$$t_{OH(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_H(min)$$

If the SRAM has an extraordinarily long read data hold time ( $t_{OH}$ ), the above equation must be modified to include the now more critical chip deselect to data outputs in High-Z time ( $t_{HZ}$ ). This is done by simply substituting  $t_{HZ}$  for  $t_{OH}$ . The modified equation is:

**Equation 1-5**

$$t_{HZ(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_H(min)$$

In addition to the above equations, one more is necessary in certain cases. In Figure 12, the read cycle is shown. At the very end of a read cycle, the read data register is clocked. The normal clocking signal for the FRC is RREGCK. Since the read data register's clock is normally connected to RREGCK, if RREGCK goes HIGH after the data from the SRAMs goes away, the data will be lost. This is only true if the SRAMs have a low  $t_{OH(min)}$ . Normally, in all of the above equations, the clock to RREGCK HIGH ( $t_{CRRGH}$ ) is substituted in place of  $t_{RDREGH}$ . In the cases where a low  $t_{OH}$  does not guarantee the data will be properly clocked, the user has another alternative.

By adding an external OR gate between the clock and RREGCK, the user can effectively shorten  $t_{CRRGH(max)}$ . The gate

"ANDs" the active LOW RREGCK with the clock when it is LOW. This produces an active LOW output signal called RDCLK (see Figure 12). This will bring the edge of read register clock into specification for any  $t_{OH}$ , even one of zero. Figure 11 shows a typical example of a SRAM interface, including this gate, should it be necessary.

Because the OR gate inherently has some delay, an equation is necessary to calculate the new  $t_{CRRGH}$ . (This "new" parameter is called  $t_{RDREGH}$ ). It should be noted that if the designer finds it necessary to implement this logic, due to a low  $t_{OH}$ , he/she must replace the  $t_{RDREGH}$  in Equation 1-1 through 1-5 with the result from the following equation, rather than the normal  $t_{CRRGH}$ . The equation for the gate is:

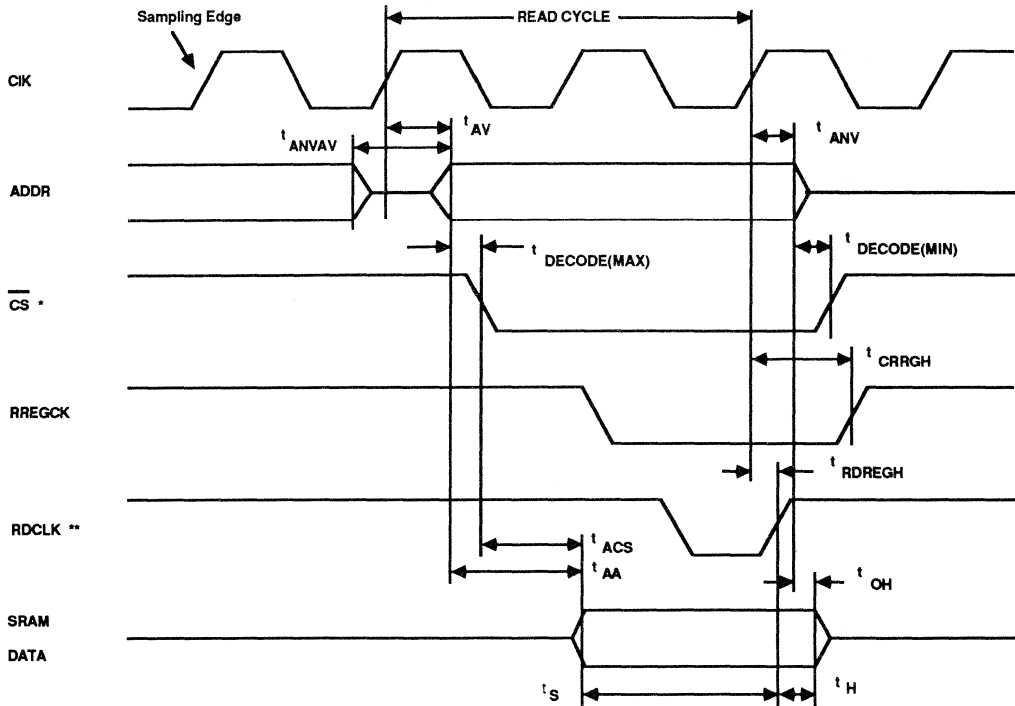
**Equation 1-6**

$$t_{RDREGH(max)} = t_{PDOR(max)}$$

Where  $t_{PDOR(max)}$  is the maximum  $t_{PD}$  through the OR gate.

Since the clock will bring RDCLK low some  $t_{PDOR(max)}$  later, the setup time of the read data register is automatically achieved.

The above equations complete the timing analysis for a read cycle. Once the user has gone through both the read and write cycle timings, an appropriate Static RAM may be chosen.



\* CS to the Static RAM bank  
 \*\* Actual clock input to the Read Data Register. This may be the same as RREGCK or may be the output of the OR-gate shown in Figure 1

Figure 12. Read Cycle Timing

## Section Two: Write Cycle Timing Analysis

Figure 13 shows the basic timings which are critical to the write cycle. Some of these parameters apply to the FRC, some to the Static RAM array, and others to external logic. The parameters that are unique to the write cycle will be summarized below:

### FRC Parameters:

$t_{PW}$	Write Pulse Width HIGH
$t_{WHAV}$	$\overline{W}$ HIGH to Address Valid
$t_{ANVAV}$	Address Not Valid to Address Valid
$t_{WHWRCH}$	$\overline{W}$ HIGH to WREGCK HIGH

### SRAM Parameters

$t_{WC}$	Write Cycle Time
$t_{AW}$	Address Valid to End of Write
$t_{CW}$	CS to End of Write
$t_{WP}$	$\overline{WE}$ Pulse Width LOW
$t_{DW}$	Data Valid to End of Write
$t_{WZ}$	$\overline{WE}$ LOW to Outputs in High-Z

### External Logic:

#### Write Data Register Parameters:

$t_{PZ}$	$\overline{OE}$ to Outputs in Low-Z
$t_{CP}$	Clock to Outputs Valid

### Other Parameters (See Text):

$$t_{WOE} = t_{DLY(max)} + t_{ORSKEW(max)}$$

There are six equations which must determine the write cycle specifications for the Static RAM. It is assumed that the user has already selected the frequency of operation and the external components needed for his/her system.

Since every write cycle consists of two physical clock cycles, all equations are with respect to  $2T$  ( $2 \times$  Cycle Time).

The first equation which should be looked at is the write cycle time ( $t_{WC}$ ). This equation will determine what speed of SRAM is required for proper operation. This parameter is the same as the total time that the address is valid. This is calculated with the following equation:

#### Equation 2-1

$$t_{WC} \leq 2T - t_{ANVAV(max)}$$

There are three basic areas to be looked at once the write cycle time has been determined. The first is the access time of the SRAM. There are two separate equations in this area.

The first parameter to be analyzed is the time from address valid to the end of write ( $t_{AW}$ ). This parameter can be calculated by taking the total write cycle time ( $2T$ ) and subtracting from it, the time from  $\overline{W}$  going HIGH to the next address becoming valid. The equation is:

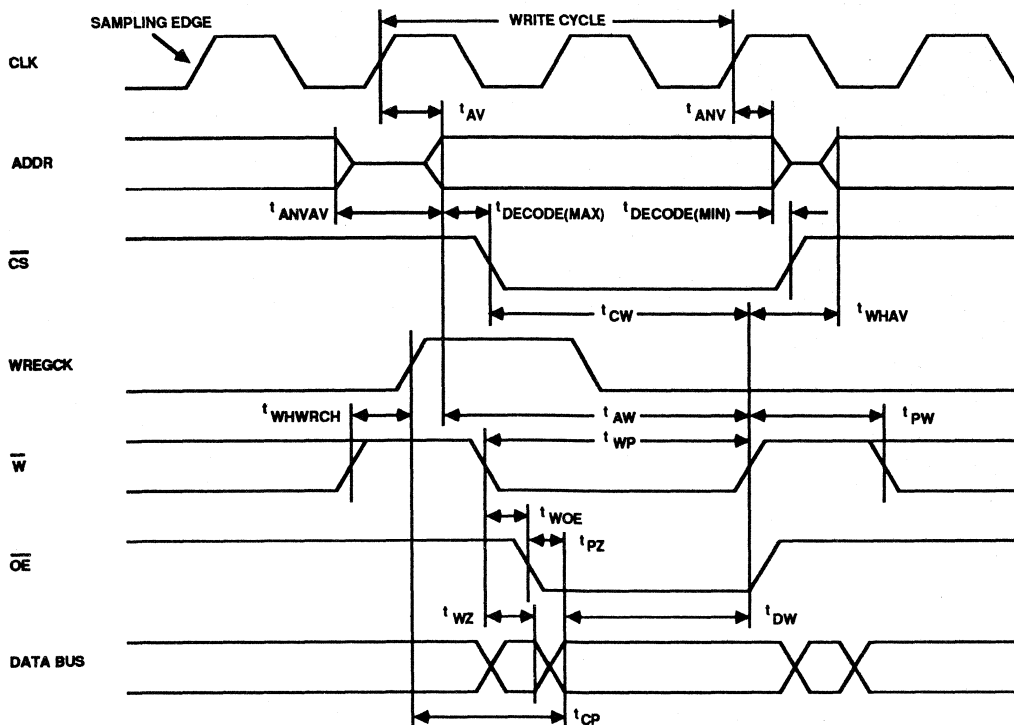


Figure 13. Write Cycle Timing

### Equation 2-2

$$t_{AW} \leq 2T - t_{WHAV}(\max)$$

The designer must also check the chip select to end of write time ( $t_{CW}$ ). This is often more critical than  $t_{AW}$  in determining which SRAM to use in the system. The  $t_{CW}$  parameter can be obtained in the same way as  $t_{AW}$  except that the decode time is also included in the equation. The modified equation is:

### Equation 2-3

$$t_{CW} \leq 2T - t_{WHAV}(\max) - t_{DECODE}(\max)$$

In addition to the various access times of the write cycle, the user must next look at the pulse width of the write signal ( $t_{WP}$ ). This is basically the difference between  $2T$  and the FRC's write time HIGH ( $t_{PW}$ ). The equation is:

### Equation 2-4

$$t_{WP} \leq 2T - t_{PW}(\max)$$

The last area that needs to be analyzed is the data setup time of the SRAM. The data setup time is specified as the time data is valid before write goes HIGH ( $t_{DW}$ ).

There are three separate equations which determine the required  $t_{DW}$  of the SRAM.

The write register has a certain propagation delay from its clock input pulse before the data becomes valid. Data must be valid at least  $t_{DW}$  before  $\overline{WE}$  goes HIGH or it will be lost. The equation takes into account the clock to output time ( $t_{CP}$ ) of the write register. The equation is:

### Equation 2-5

$$t_{DW} \leq 2T - t_{CP}(\max) - t_{WHWRCH}(\max)$$

The write data register is enabled by the  $\overline{W}$  signal of the FRC. The register takes some minimum time before it enables its outputs from the High-Z state ( $t_{PZ}$ ).

The SRAMs have some maximum time in which they disable their outputs when the  $\overline{WE}$  signal goes LOW. This parameter is the time from  $\overline{WE}$  LOW to the data outputs in High-Z ( $t_{WZ}$ ).

If  $t_{WZ}(\max)$  is greater than  $t_{PZ}(\min)$ , bus contention will result. To counter this problem a delay must be introduced between the  $\overline{W}$  signal of the FRC and the  $\overline{OE}$  input of the write data register. In addition, an OR gate is used to bring  $\overline{OE}$  HIGH shortly after  $\overline{W}$  goes HIGH. This is illustrated in Figure 11.  $t_{WOE}(\max)$  is the total delay between  $\overline{W}$  going LOW and  $\overline{OE}$  going LOW. It is calculated by the following equation:

### Equation 2-6

$$t_{WOE}(\max) = t_{DLY}(\max) + t_{PDOR}(\max)$$

Where  $t_{DLY}(\max)$  is the maximum delay through the delay line.

$t_{PDOR}(\max)$  is the maximum propagation delay through the OR gate.

Equation 2-5 dictated the  $t_{DW}$  based on the clock to output time of the register. In most cases though, this time is automatically guaranteed. Since the data will not be valid (Low-Z) until some  $t_{PZ}$  after  $\overline{OE}$  goes LOW, even though it has been clocked properly, a new equation is necessary to determine the  $t_{DW}$  of the SRAM. This equation must take into account the delay that was added in to prevent bus contention. It must also take into

account the  $t_{PZ}$  time of the register. The equation is very similar to Equation 2-5 with those exceptions. The equation thus becomes:

### Equation 2-7

$$t_{DW} \leq 2T - t_{PW}(\max) - t_{PZ}(\max) - t_{WOE}(\max)$$

One additional equation is required to determine the delay line required to prevent bus contention. The equation for the delay line takes into account the maximum  $t_{PD}$  through the OR gate. The equation is based on the  $t_{WZ}$  of the SRAM and the  $t_{PZ}$  of the write data register. The equation is:

### Equation 2-8

$$t_{DLY}(\min) = t_{WZ}(\max) - t_{PZ}(\min) - t_{OR}(\min)$$

The above equations complete the timing analysis of the write cycle. Once the user has gone through both the read and write cycle timings, an appropriate Static RAM may be chosen.

## An Example Interface

In order to determine any Static RAM parameters, the user must know several things. He/she must identify the frequency of operation, the read and write data registers, the chip select decoder, and any other logic which may be necessary.

As an example, assume that a 5-MHz data throughput is desired. This will allow a 10-MHz all read or all write data rate. This data rate dictates a 20-MHz clock speed for the FRC.

For worst case design, assume that the selected SRAM has a  $t_{OH}$  of zero. Since  $t_{OH} = 0$  ns, there must be an external OR-gate to clock the read register. In addition, assume that the selected SRAM has a  $t_{WZ}(\max) \leq 20$  ns.

In order to resolve any bus contention a delay line and another OR gate will be added.

74F series parts are used to keep the design clean. It should be noted that the user can use any kind of logic. Because of the particular worst case SRAM parameters that were chosen, this design contains the maximum number of parts that are required for any design.

Given the above considerations, this 20-MHz design requires the following parts:

### Parts List:

<u>QTY</u>	<u>PART</u>	<u>DESCRIPTION</u>
1	674219	FIFO RAM Controller
1	74F138	Address Decoder
2	74F374	8-bit Register
1	74F32	OR-Gate
1	20 ns $\pm$ 10%	Delay Line

The following is a step-by-step analysis of the read and write equations to determine the required SRAM parameters. The equations will also show the delay line needed to avoid bus contention.



## Read Equations:

### Equation 1-1

$$t_{RC} \leq 2T - t_{\text{DECODE(max)}} + t_{\text{DECODE(min)}} - t_{\text{ANVAV(max)}}$$
$$\begin{array}{cccc} 100 - 9.0 & + 3.0 & - 12 & \\ \text{[FRC]} & \text{[F138]} & \text{[FRC]} & \end{array}$$

$$t_{RC} \leq 82.0 \text{ ns}$$

### Equation 1-6

$$t_{\text{RDREGH(max)}} = t_{\text{ANV(min)}} - t_{\text{ORSKEW(max)}}$$
$$\begin{array}{ccc} 15 & - & 6.6 \\ \text{[FRC]} & & \text{[F32]} \end{array}$$

$$t_{\text{RDREGH(max)}} = 6.6 \text{ ns}$$

### Equation 1-2

$$t_{AA} \leq 2T - \text{MAX}(t_{AV} - t_{\text{RDREGH}}) - t_{S(\text{min})}$$
$$\begin{array}{cccc} 100 - (40 & - & 8.4) & - & 2.0 \\ \text{[FRC]} & \text{[FRC]} & \text{[F32]} & & \text{[F374]} \end{array}$$

$$t_{AA} \leq 66.4 \text{ ns}$$

### Equation 1-3

$$t_{ACS} \leq 2T - t_{\text{DECODE(max)}} - \text{MAX}(t_{AV} - t_{\text{RDREGH}}) - t_{S(\text{min})}$$
$$\begin{array}{cccc} 100 - 9.0 & - & (40 & - & 8.4) & - & 2.0 \\ \text{[FRC]} & \text{[F138]} & & \text{[FRC]} & \text{[F32]} & & \text{[F374]} \end{array}$$

$$t_{ACS} \leq 57.4 \text{ ns}$$

### Equation 1-4

$$t_{OH(\text{min})} + t_{\text{ANV(min)}} \geq t_{\text{RDREGH(max)}} + t_{H(\text{min})}$$
$$\begin{array}{cccc} 0 & + & 15 & \geq & 8.4 & + & 2.0 \\ \text{[SRAM]} & \text{[FRC]} & & \text{[F32]} & & & \text{[F374]} \end{array}$$
$$15 \text{ ns} \geq 10.4 \text{ ns}$$

### Equation 1-5

$$t_{HZ(\text{min})} + t_{\text{ANV(min)}} \geq t_{\text{RDREGH(max)}} + t_{H(\text{min})}$$
$$\begin{array}{cccc} 0 & + & 15 & \geq & 8.4 & + & 2.0 \\ \text{[SRAM]} & \text{[FRC]} & & \text{[F32]} & & & \text{[F374]} \end{array}$$
$$15 \text{ ns} \geq 10.4 \text{ ns}$$

## Write Equations:

### Equation 2-1

$$t_{WC} \leq 2T - t_{\text{ANVAV(max)}}$$
$$\begin{array}{cc} 100 - 12 & \\ \text{[FRC]} & \text{[FRC]} \end{array}$$

$$t_{WC} \leq 88.0 \text{ ns}$$

### Equation 2-2

$$t_{AW} \leq 2T - t_{\text{WHAV(max)}}$$
$$\begin{array}{cc} 100 - 25 & \\ \text{[FRC]} & \text{[FRC]} \end{array}$$

$$t_{AW} \leq 75.0 \text{ ns}$$

### Equation 2-3

$$t_{CW} \leq 2T - t_{\text{WHAV(max)}} - t_{\text{DECODE(max)}}$$
$$\begin{array}{ccc} 100 - 25 & - & 9.0 \\ \text{[FRC]} & \text{[FRC]} & \text{[F138]} \end{array}$$

$$t_{CW} \leq 66.0 \text{ ns}$$

### Equation 2-4

$$t_{WP} \leq 2T - t_{\text{PW(max)}}$$
$$\begin{array}{cc} 100 - 25 & \\ \text{[FRC]} & \text{[FRC]} \end{array}$$

$$t_{WP} \leq 75.0 \text{ ns}$$

### Equation 2-5

$$t_{DW} \leq 2T - t_{\text{CP(max)}} - t_{\text{WHWRCH(max)}}$$
$$\begin{array}{ccc} 100 - 12.5 & - & 18 \\ \text{[FRC]} & \text{[F374]} & \text{[FRC]} \end{array}$$

$$t_{DW} \leq 69.5 \text{ ns}$$

### Equation 2-8

$$t_{DLY(\text{min})} = t_{\text{WZ(max)}} - t_{\text{PZ(min)}} - t_{\text{OR(min)}}$$
$$\begin{array}{ccc} 20 & - & 2.0 & - & 3.0 \\ \text{[SRAM]} & \text{[F374]} & \text{[F32]} & & \end{array}$$

$$t_{DLY(\text{min})} = 15 \text{ ns (USE } 20 \text{ ns ' 10\%)}$$

### Equation 2-6

$$t_{\text{WOE(max)}} = t_{DLY(\text{max})} + t_{\text{OR(max)}}$$
$$\begin{array}{cc} 22 & + & 6.6 \\ \text{[DELAY]} & & \text{[F32]} \end{array}$$

$$t_{\text{WOE(max)}} = 28.6 \text{ ns}$$

### Equation 2-7

$$t_{DW} \leq 2T - t_{\text{PW(max)}} - t_{\text{PZ(max)}} - t_{\text{WOE(max)}}$$
$$\begin{array}{ccc} 100 - 25 & - & 12.5 & - & 28.6 \\ \text{[FRC]} & \text{[FRC]} & \text{[F374]} & \text{[delay]} & \end{array}$$

$$t_{DW} \leq 33.9 \text{ ns}$$

## RESULTS

### READ PARAMETERS:

Minimum  $t_{RC}$  = 82.0 ns  
 Minimum  $t_{AA}$  = 66.4 ns  
 Minimum  $t_{ACS}$  = 57.4 ns  
 Minimum  $t_{OH}$  = 0 ns (Assumed)  
 Minimum  $t_{HZ}$  = 0 ns (Assumed)

### WRITE PARAMETERS:

Minimum  $t_{WC}$  = 88.0 ns  
 Minimum  $t_{AW}$  = 75.0 ns  
 Minimum  $t_{CW}$  = 66.0 ns  
 Minimum  $t_{WP}$  = 75.0 ns  
 Minimum  $t_{DW}$  = 33.9 ns (Equation 2-7 used for  $t_{DW}(\min)$ )  
 Minimum  $t_{WR}$  = 0 ns (Because FRC's  $t_{WR} = 0$  ns)

### DELAY LINE:

20 ns Delay Line (\*10%)

Based on those results, the Hitachi HM6168H-45 was selected. This is a 4096 x 4-bit Static RAM with a 45-ns access time. Its specifications are:

### READ PARAMETERS:

Minimum  $t_{RC}$  = 45.0 ns  
 Minimum  $t_{AA}$  = 45.0 ns  
 Minimum  $t_{ACS}$  = 45.0 ns  
 Minimum  $t_{OH}$  = 5.0 ns  
 Minimum  $t_{HZ}$  = 0 ns

### WRITE PARAMETERS:

Minimum  $t_{WC}$  = 45.0 ns  
 Minimum  $t_{AW}$  = 40.0 ns  
 Minimum  $t_{CW}$  = 40.0 ns  
 Minimum  $t_{WP}$  = 35.0 ns  
 Minimum  $t_{DW}$  = 20.0 ns  
 Minimum  $t_{WR}$  = 0 ns

Sixteen 4K x 4-bit SRAMs are required to complete a 32K x 8-bit FIFO buffer. The complete design is shown in Figure 14. This illustrates the two OR-gates, the delay line, the decoder, the two registers, the Static RAM array and the 674219 FIFO RAM Controller in a 20-MHz design.

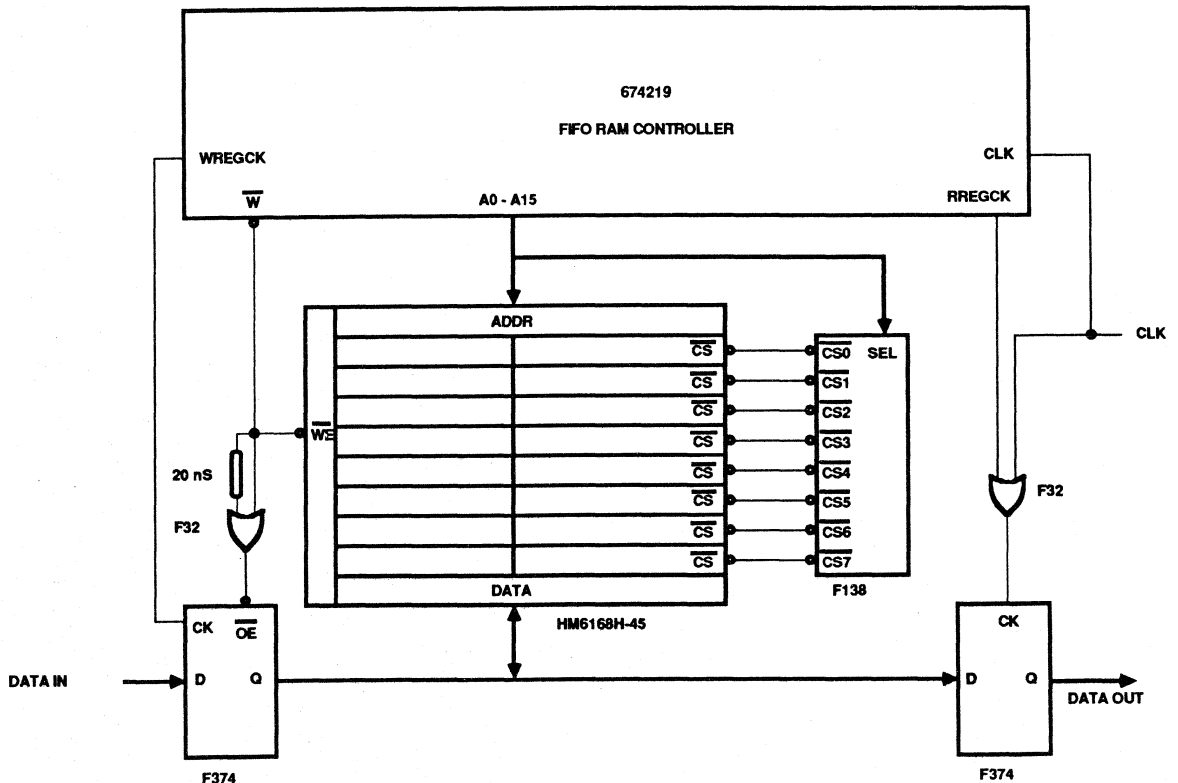


Figure 14. Worst Case Design for 20 MHz

## Absolute Maximum Ratings

Supply voltage $V_{CC}$	-0.5 V to 7.0 V
DC input voltage $V_I$	-0.5 V to 5.5 V
DC output voltage, $V_O$	-0.5 V to 5.5 V
Off-state output voltage	-0.5 V to 5.5 V
Storage temperature	-65° to +150°C

## Operating Conditions

SYMBOL	PARAMETER	FIG.	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	N/A	4.5	5	5.5	4.75	5	5.25	V
$T_A$	Operating free-air temperature	N/A	-55		125	0		75	°C
$t_{CLKWH}$	Clock width HIGH	9,10	45			31			ns
$t_{CLKWL}$	Clock width LOW	9,10	34			18			ns
$f_{CLK}$	Clock frequency	N/A			12.5			20	MHz
$t_{REQL}$	Request LOW time	7,9,10	12			12			ns
$t_{REQH}$	Request HIGH time	9,10	25			25			ns
$t_{MRL}$	Master Reset width LOW	7	60			50			ns
$t_{MRS}$	Master Reset HIGH to WREQ LOW	7	25			25			ns
$t_{PS}$	Priority to non-sampling clock setup time	5,6	30			25			ns
$t_{EWQ}$	WEN to WREQ setup time	7,9	0			0			ns
$t_{ERRQ}$	REN to RREQ setup time	10	0			0			ns
$t_{WEH}$	WREQ to WEN hold time	9	15			15			ns
$t_{REH}$	RREQ to REN hold time	10	15			15			ns
$t_{WRQC}$	WREQ LOW to sampling clock setup time	7,9	5*		30*	10*		25*	ns
$t_{RRQC}$	RREQ low to sampling clock setup time	10	5*		30*	10*		25*	ns

\* The request window must be observed to guarantee proper operation, between min and max values are not allowed.

## Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION	COMMERCIAL			UNIT	
			MIN	TYP	MAX		
$V_{IL}$	Low-Level input voltage				0.8	V	
$V_A$	High-level input voltage				2	V	
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$ $I_I = -18 \text{ mA}$			-1.5	V	
$I_{IL}^*$	Low-level input current	$V_{CC} = \text{MIN}$ $V_I = 0.45 \text{ V}$			-250	$\mu\text{A}$	
$I_{IH}^*$	High-level input current	$V_{CC} = \text{MIN}$ $V_I = 2.4 \text{ V}$			50	$\mu\text{A}$	
$I_I$	Maximum input current	$V_{CC} = \text{MIN}$ $V_I = 5.5 \text{ V}$			1	mA	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ $V_{CC} = \text{MIN}$ $V_{CC} = \text{MIN}$ $I_{OL} \text{ (Address)} = 16 \text{ mA}$ $I_{OL} \text{ (Control)} = 8 \text{ mA}$ $I_{OL} \text{ (Flag)} = 8 \text{ mA}$			0.5	V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ $V_{CC} = \text{MIN}$ $V_{CC} = \text{MIN}$ $I_{OH} \text{ (Address)} = -3 \text{ mA}$ $I_{OH} \text{ (Control)} = -3 \text{ mA}$ $I_{OH} \text{ (Flag)} = -3 \text{ mA}$			2.4	V	
$I_{OS}^{**}$	Output short-circuit current	$V_{CC} = \text{MAX}$ $V_{OH} = 0 \text{ V}$			-20	-90	mA
$I_{OZH}$ $I_{OZL}$	Off-state output currents	$V_{CC} = \text{MAX}$ $V_{CC} = \text{MAX}$ $V_O = 2.4 \text{ V}$ $V_O = 0.4 \text{ V}$			+40	-350†	$\mu\text{A}$
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$			350	mA	

\*Except TEST pin, which should always be grounded.

\*\*No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

† $I_{OZL}$  is Output leakage current plus  $I_{IL}$ .

2

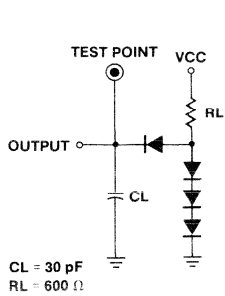
## Switching Characteristics

SYMBOL	PARAMETER	FIG.	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>MRWH</sub>	Master Reset LOW to WRDY HIGH	7			50		50	ns	
t <sub>MRRL</sub>	Master Reset LOW to RRDY LOW	7			50		50	ns	
t <sub>MREF</sub>	Master Reset LOW to EMPTY flag HIGH	7			50		50	ns	
t <sub>MRAL</sub>	Master Reset LOW to Almost HIGH	7			60		55	ns	
t <sub>MRWRC</sub>	Master Reset LOW to WREGCK HIGH	7			40		35	ns	
t <sub>MRRRC</sub>	Master Reset LOW to RREGCK HIGH	7			40		35	ns	
t <sub>MRWBH</sub>	Master Reset LOW to W HIGH	7			50		50	ns	
t <sub>AV</sub>	Clock to address valid	7,9,10,12,13			50		40	ns	
t <sub>ANV</sub>	Clock to address not valid	7,9,10,12,13	15			15		ns	
t <sub>ANVAV</sub>	Address not valid to address valid	7,9,10,12,13			20		12	ns	
t <sub>CWRL</sub>	Clock to WRDY LOW	7,9			35		35	ns	
t <sub>CWRH</sub>	Clock to WRDY HIGH	7,9			40		35	ns	
t <sub>CWRGL</sub>	Clock to WREGCK LOW	7,9			35		30	ns	
t <sub>CWRGH</sub>	Clock to WREGCK HIGH	7,9			35		30	ns	
t <sub>CWL</sub>	Clock to W LOW	7,9			50		45	ns	
t <sub>CWH</sub>	Clock to W HIGH	7,9			25		25	ns	
t <sub>AS</sub>	Address valid to W LOW	7,9	0		12	0	12	ns	
t <sub>WR</sub>	Address not valid to W HIGH	7,9			0		0	ns	
t <sub>WP</sub>	W pulse width LOW at f <sub>CLK(max)</sub>	9,13	100*			50**		ns	
t <sub>PW</sub>	W pulse width HIGH	4,13	12		30	12	25	ns	
t <sub>WHAV</sub>	W HIGH to address valid	4,9,13			35		25	ns	
t <sub>WHWRCH</sub>	W HIGH to WREGCK HIGH	4,13			25		18	ns	
t <sub>CRRL</sub>	Clock to RRDY LOW	10			35		30	ns	
t <sub>CRRH</sub>	Clock to RRDY HIGH	7,10			40		35	ns	
t <sub>CRRGL</sub>	Clock to RREGCK LOW	7,10			35		30	ns	
t <sub>CRRGH</sub>	Clock to RREGCK HIGH	7,10,12			35		30	ns	
t <sub>ARRH</sub>	Address valid to RREGCK HIGH at f <sub>CLK(max)</sub>	10	110*			60**		ns	
t <sub>ANRRH</sub>	Address not valid to RREGCK HIGH	10			10		8	ns	
t <sub>CE</sub>	Clock to EMPTY flag	7,9,10			40		35	ns	
t <sub>CF</sub>	Clock to FULL flag	9,10			40		35	ns	
t <sub>CHF</sub>	Clock to Half-Full flag	9,10			50		45	ns	
t <sub>CA</sub>	Clock to Almost flag	9,10			60		55	ns	
t <sub>LZ</sub>	Address bit LOW to Hi-Z	15			30		30	ns	
t <sub>HZ</sub>	Address bit HIGH to Hi-Z	15			30		30	ns	
t <sub>ZL</sub>	Address bit Hi-Z to LOW	15			30		30	ns	
t <sub>ZH</sub>	Address bit Hi-Z to HIGH	15			30		30	ns	

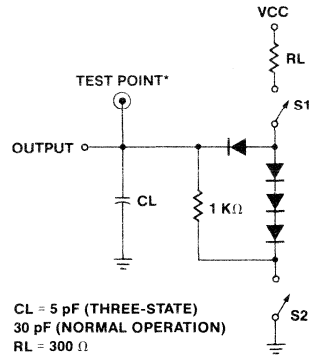
\* f<sub>CLK(max)</sub> = 12.5 MHz (Military).

\*\* f<sub>CLK(max)</sub> = 20 MHz (Commercial).

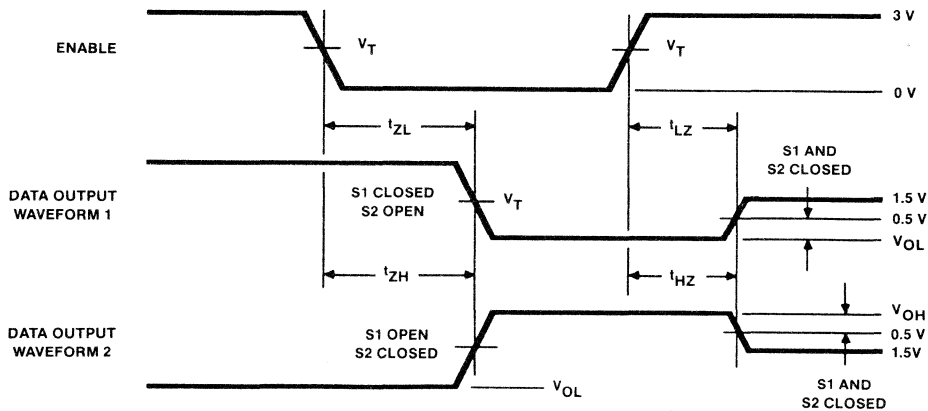
## Standard Test Load



**Load Circuit  
for Bi-State Outputs  
(Control and Flag Outputs)**



**Load Circuit  
for Three-State Outputs  
(Address Outputs)**



Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled.  
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled.

**Figure 15. Enable and Disable Timing**

Notes: A.  $C_L$  includes probe and jig capacitance.

B. All diodes are 1N916 or 1N306A.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz.  $Z_{Out} = 50 \Omega$  and  $t_R \leq 2.5$  ns  $t_F \leq 2.5$  ns.

F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

# Am4701-45

Bidirectional 512x8 FIFO Am4701 BIFIFO (Previously 67C4701)



## DISTINCTIVE CHARACTERISTICS

- 2-512x8 FIFO buffer, provides asynchronous bidirectional full duplex communication.
- Full and Empty Flags
- Programmable Almost-Full and Almost-Empty flags.
- Byte detect mode.
- No handshaking necessary.
- Built in parity checker/generator.
- Generates and detects framing bit.
- Programmable Interrupt request.
- Bypass mode—Changes the Am4701 to a transceiver.
- Two mailboxes.
- Bidirectional data bus.
- Low power consumption.

## GENERAL DESCRIPTION

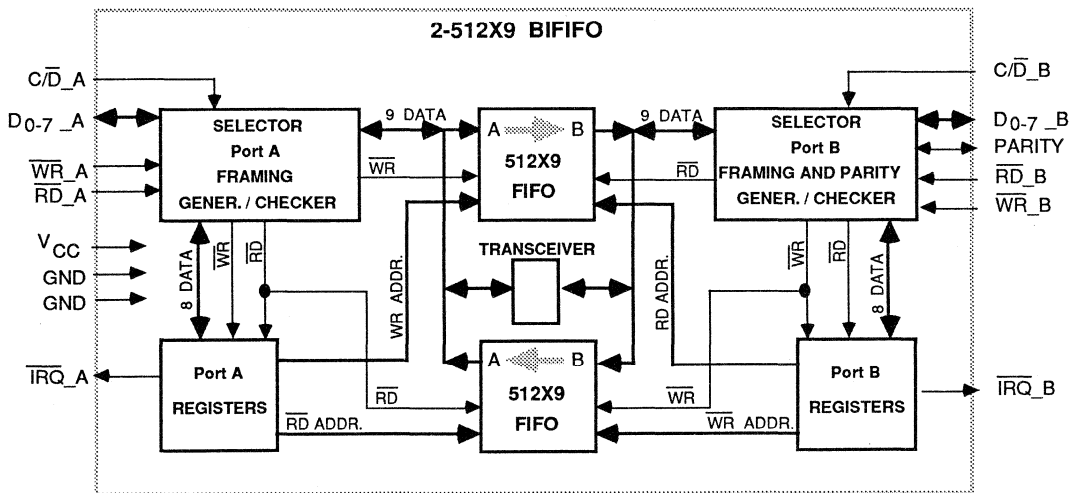
The Am4701 is a CMOS RAM-based, fully asynchronous, byte-wide bidirectional First In First Out (FIFO) device that is 512 words deep with 8-bit wide words in each direction. It contains two 512x9 dual-port memory arrays with the ninth bit in each array reserved for framing and parity functions.

The Am4701 can accept and output data asynchronously and simultaneously at data rates from 0 to 16.7 MHz. Interrupt driven status flags are provided to signify Full, Empty and user programmable Almost Full and Almost Empty conditions. Parity generation/check-

ing, programmable interrupt requests, byte-detection, framing and port-to-port communication through mail boxes are provided on chip. The Am4701 can also operate in Bypass Mode where it behaves like a transceiver.

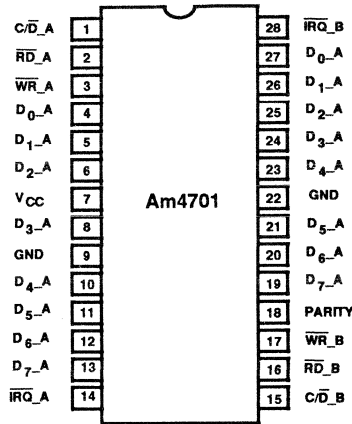
The Am4701 is ideally suited for bidirectional inter-processor communication and data-buffering between a CPU and a peripheral device. The ability to buffer large transfers of data and its rate adaption capabilities make the Am4701 useful in communication, image processing, DSP and printing systems.

## BLOCK DIAGRAM

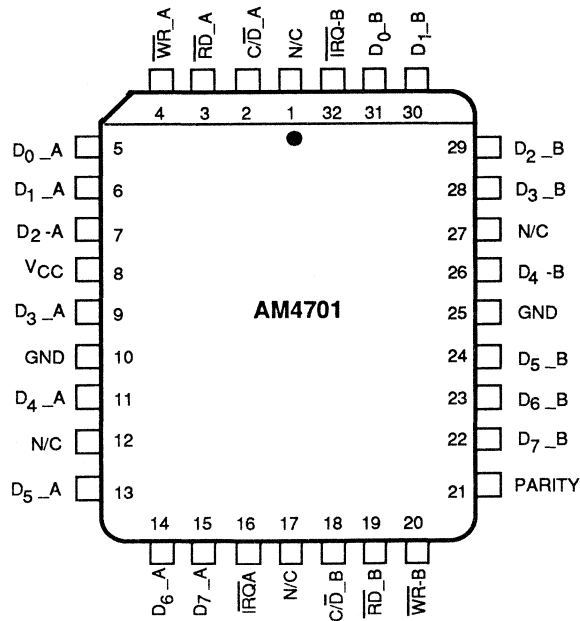


# CONNECTION DIAGRAM

## TOP VIEW DIP



## PLCC PRELIMINARY

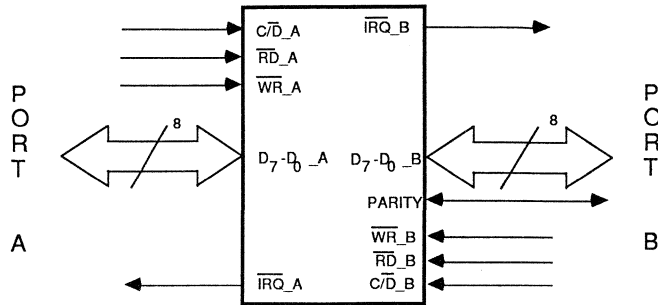


NOTE: Pin 1 is marked for orientation.

11120-010B

N/C: No Connection

## LOGIC SYMBOL



11120-009B

## DEFINITIONS

### PIN NAMES

PORT B	PORT A	NAMES
$\overline{RD}_B$	$\overline{RD}_A$	READ ENABLE
$\overline{WR}_B$	$\overline{WR}_A$	WRITE ENABLE
$C/\overline{D}_B$	$C/\overline{D}_A$	COMMAND / DATA SELECTION
$\overline{IRQ}_B$	$\overline{IRQ}_A$	INTERRUPT REQUEST OUTPUT
$D_{0-7}_B$	$D_{0-7}_A$	BIDIRECTIONAL DATA BUS
PARITY		PARITY / FRAMING BIT (PORT B ONLY)
	$V_{CC}$	SUPPLY VOLTAGE
	GND	GROUND ( 2 PINS )

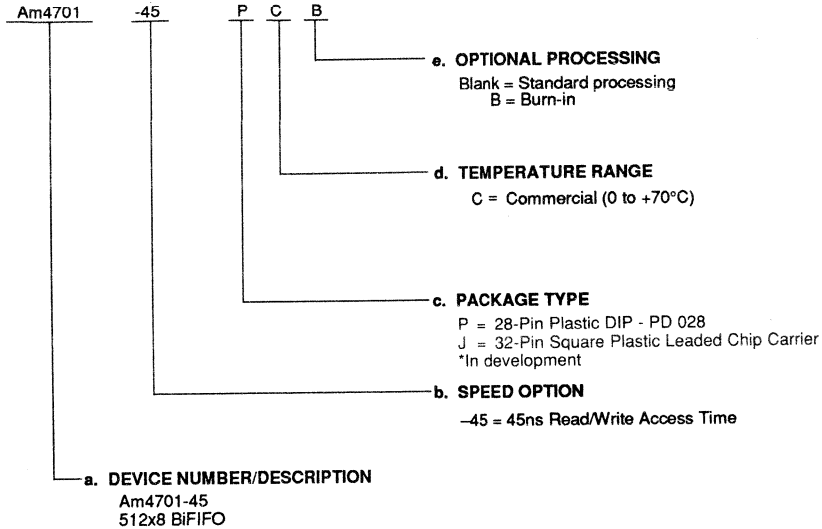


# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
Am4701-45	PC, JC (future)

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

---

## PIN DESCRIPTION

### $D_7$ - $D_0$ \_A, B

8-bit bidirectional data bus for port A, B.

### Parity

Bidirectional parity/framing bit for port B only.

### $\overline{RD}$ \_A,B

Read input for port A or B. The falling edge of Read initiates a read from the FIFO or the internal registers. Both ports can be read simultaneously by  $\overline{RD}_A$  and  $\overline{RD}_B$ .

### $\overline{WR}$ \_A,B

Write input to port A or B. The falling edge of Write initiates a write cycle. Both ports can write simultaneously by  $\overline{WR}_A$  and  $\overline{WR}_B$ .

### $C/\overline{D}$ \_A,B

Command / Data selection for port A or B.

$C/\overline{D}$  = High : Read or Write to the internal registers.

$C/\overline{D}$  = Low : Read or Write to the FIFO.

### $\overline{IRQ}$ \_A,B

Interrupt request output of port A, B. The  $\overline{IRQ}$  flag will be active low by any change of status in the appropriate port and is reset by reading the status register of the same port. Each port's  $\overline{IRQ}$  flag can be masked by its mask register.

---

## FUNCTIONAL DESCRIPTION

The Am4701 provides an asynchronous full duplex connection between two CPUs working in a Multi-processing mode, or between a CPU and a peripheral device.

Each port writes into a 512x8 FIFO and reads from the other FIFO. Each port has a set of internal register and a framing generator/checker. Port B has an additional parity generator/checker.

### I. Registers

Each port of Am4701 has a set of internal registers which control the operation of BiFIFO. Each port's registers can read and write asynchronously. Accessing these registers requires two cycles. In order to access these registers, the user has to write the address of the register during Cycle 1 in the pointer register. In Cycle 2 write/read operation of the addressed register is performed. The pointer register (write only register) and status register (read only register) are located at address 0. Accessing the pointer register or status register requires one cycle only. Accessing of other registers is explained below:

#### Writing Data to register

(i) Cycle 1-Writing Address: With  $C/\overline{D}$  at high,  $\overline{WR}$  is asserted low and the address of register appearing at data bus  $D_0$ - $D_2$  (see Fig. 12)  $t_{DW}$  prior to and  $t_{DH}$  after the rising edge of  $\overline{WR}$  will be written to the pointer register.

(ii) Cycle 2-Writing Data: With  $C/\overline{D}$  at high and  $\overline{WR}$  at low, the data set on the data bus (see Fig. 12)  $t_{DW}$  prior to and  $t_{DH}$  after the rising edge of  $\overline{WR}$  will be written into the addressed register.

#### Reading Data from register

(i) Cycle 1-Writing Address: With  $C/\overline{D}$  at high,  $\overline{WR}$  is asserted low and the address of register appearing at data bus  $D_0$ - $D_2$  (see Fig. 12)  $t_{DW}$  prior to and  $t_{DH}$  after the rising edge of  $\overline{WR}$  will be written to the pointer register.

(ii) Cycle 2-Reading Data: With  $C/\overline{D}$  at high, the falling edge of  $\overline{RD}$  initiates the read cycle. (see Fig. 11) Data appears on the data bus  $t_{RA}$  after the falling edge of  $\overline{RD}$ .

After Cycle 2 the pointer register is cleared automatically.

### II. FIFO

The part has two 512x9 FIFOs connected back to back. Each port can read and write asynchronously. The FIFO is based on a dual port RAM cell and can be read and written simultaneously. The read and write addresses to the FIFO are generated by the read and the write pointers of every port. Data is limited to 8 bits. The ninth bit in the FIFO is provided to support parity or framing functions.

#### Writing Data to the FIFO

With  $C/\overline{D}$  at low, the falling edge of write ( $\overline{WR}$ ) initiates a write cycle (see Fig. 12). Data appearing at inputs  $D_0$ - $D_8$ ,  $t_{DS}$  prior to and  $t_{DH}$  after the rising edge of  $\overline{WR}$  will be stored sequentially in the FIFO.

#### Reading Data from the FIFO

With  $C/\overline{D}$  at low, the falling edge of Read ( $\overline{RD}$ ) initiates a read cycle (see Fig. 11). Valid data appears on the data bus  $t_{RA}$  after the falling edge of  $\overline{RD}$  and remains valid for  $t_{OH}$  after the rising edge of  $\overline{RD}$ .

### III. Parity

The Am4701 has a parity generator/checker for port B only. Port B Command register enables the generator and chooses the odd or even parity mode. While reading from port B, the parity bit is generated and sent out by the parity pin output.

While writing to port B, the parity checker gets 9 bits of data and checks if the parity bit is valid. If the parity bit is wrong, port B will get an interrupt at the end of the write, Bit 9 of the written byte will be set to HIGH. When the byte reaches port A, the framing detector of port A will detect the byte and interrupt port A.

### IV. Framing

Both ports have a framing generator and checker. The framing bit points a byte in a block, and can be used to identify :

Beginning or end byte in a block.

Command byte between data bytes.

Wrong data byte between valid data bytes.

#### A. Framing from Port A to Port B

Port A writes bytes of data to port B with framing bit = "0". When port A wants to change the framing bit, it has to write a "1" to the framing bit in the pointer register. Writing to the FB bit in the pointer register will set the framing bit of the next data byte written to the FIFO.

The FB bit in the pointer register will be reset automatically after writing to the FIFO; every writing to the FB flag will frame one byte of data only.

The byte with the framing bit will be shifted to port B and set the FD (frame detect) flag in port B's status register. If the FD flag is not masked it will set the  $\overline{\text{IRQ}}_B$  output and interrupt port B's CPU.

If port B is working in the framing mode, the framing bit will be sent out through the parity pin together with the other 8 data bits while port B is reading.

If port B is working in the Parity mode, the framing bit will be changed at port B to a parity bit by the parity generator and will be sent to port B's CPU through the parity output pin. However, the frame detect flag will be set in port B's status register.

#### B. Framing from Port B to Port A

Port B can send framing bits to port A in 3 different modes:

- a. While working in the parity mode.
  - b. While working in the framing mode and using the parity pin.
  - c. While working in the framing mode and using framing bit in the pointer register.
- a. Port B's CPU writes to port B 8 data bits and a parity bit. The parity checker in port B checks the parity bit and sets the PE (parity error) flag if an error is detected. The PE flag will set the  $\overline{\text{IRQ}}$  of port B. The errored byte will automatically be signed by a framing bit, which will be detected by the frame checker in port A. When the erroneous byte reaches port A, the framing bit will set  $\overline{\text{IRQ}}_A$ .
  - b. Port B's CPU writes to port B 8 data bits and a framing bit through the parity input pin. The bit will be detected by the frame checker in port A and will set  $\overline{\text{IRQ}}_A$ .
  - c. Port B's CPU writes to port B 8 data bits and the framing bit is written through the pointer register (like in port A). The bit will be detected by the frame checker in port A and will set  $\overline{\text{IRQ}}_A$ .

### V. Bypass Mode

The bypass mode changes the Am4701 to a transceiver between the A and B buses. The bypass mode is controlled by the "BP" bit in port A command register. Changing to this mode will not change the data in the FIFO and the address of the FIFO pointers. Table 1 gives the logic state of control pins for transceiver action and for accessing internal registers in Bypass Mode.

#### A. Writing/Reading Between Port A and Port B.

While BP bit in port A command register is HIGH and C/D of port A and port B are LOW, port A can read and write to port B data bus. Port B's read and write commands will be ignored, the only master on port A and port B is port A's CPU.

Function	$\overline{\text{RD}}_A$	$\overline{\text{WR}}_A$	$\text{C}/\overline{\text{D}}_A$	$\overline{\text{RD}}_B$	$\overline{\text{WR}}_B$	$\text{C}/\overline{\text{D}}_B$
Writing data from A to B Bus.	H	L	L	X	X	L
Reading data from B to A Bus.	L	H	L	X	X	L
Writing data to A registers.	H	L	H	X	X	X
Reading data from A registers.	L	H	H	X	X	X
Writing data to B registers.	H	L	L	H	L	H
Reading data from B registers.	L	H	L	L	H	H

Table 1. Bypass Mode Truth Table

## B. Writing/Reading Port A's Registers.

While BP bit in port A command register is HIGH and C/D of port A is HIGH, port A can access its internal registers as in the FIFO mode. Port B's read and write commands will be ignored and the only master on the Am4701 is port A.

databus  $D_0-D_7_A$ . With  $C/\overline{D}_A$  at LOW,  $C/\overline{D}_B$  at HIGH, and  $\overline{WR}_A$  at LOW,  $\overline{WR}_B$  is pulsed LOW. Data appearing on  $D_0-D_7_A$  (see Fig. 20)  $t_{DW}$  prior to and  $t_{DH}$  after the rising edge of  $\overline{WR}_B$  will be written to the register.

## C. Writing/Reading Port B's Registers.

While BP bit in port A command register is HIGH, port A can access port B's internal registers.

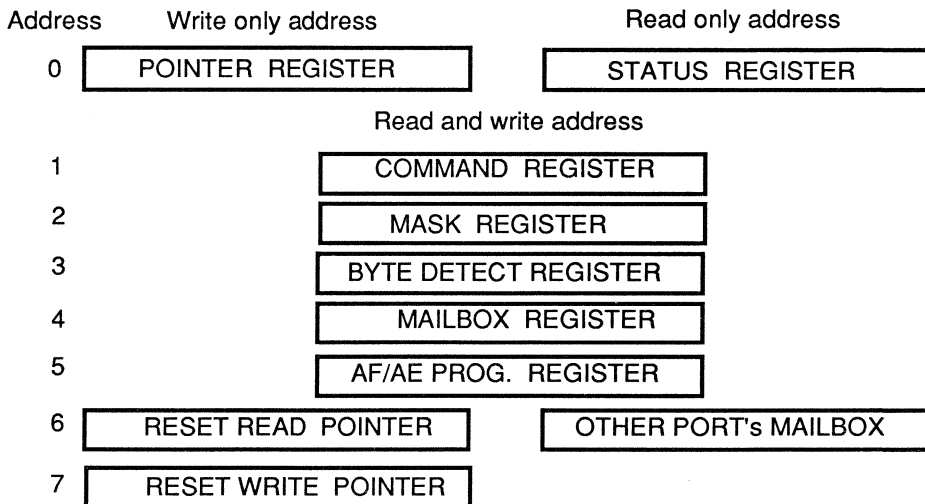
### (i) Writing to port B Registers

- a. Cycle 1-Writing Address: With  $C/\overline{D}_A$  at LOW,  $C/\overline{D}_B$  at HIGH and  $\overline{WR}_A$  at LOW,  $\overline{WR}_B$  is pulsed LOW. Data appearing on  $D_0-D_2_A$  (see Fig. 20)  $t_{DW}$  prior to and  $t_{DH}$  after the rising edge of  $\overline{WR}_B$  will be written to the pointer register of B.
- b. Cycle 2-Writing Data: Port A sets the data to be written to port B's register at the

### (ii) Reading from port B Registers

- a. Cycle 1-Writing Address: With  $C/\overline{D}_A$  at LOW,  $C/\overline{D}_B$  at HIGH and  $\overline{WR}_A$  at LOW,  $\overline{WR}_B$  is pulsed LOW. Data appearing on  $D_0-D_2_A$  (see Fig. 20)  $t_{DW}$  prior to and  $t_{DH}$  after the rising edge of  $\overline{WR}_B$  will be written to the pointer register of B.
- b. Cycle 2-Reading Data: With  $C/\overline{D}_A$  at LOW,  $C/\overline{D}_B$  at HIGH and  $\overline{RD}_A$  at LOW,  $\overline{RD}_B$  is pulsed LOW. The falling edge of  $\overline{RD}_B$  initiates the read cycle (see Fig. 19). Data appears in  $D_0-D_7_A$   $t_{RA}$  after to falling edge of  $\overline{RD}_B$ .

## INTERNAL REGISTER



1029 04

Figure 1. One Port's Register Set

Every port of the Am4701 has 7 internal registers addressed by the Pointer register.

The internal registers are:

- Pointer register (write only register).
- Status register (read only register).
- Command, Mask, Byte-detect, Mailbox, Almost-Full Almost-empty registers.

The Pointer and Status registers are both addressed at address 0. The other read/write registers are addressed at address 1 to 5. Addresses 6 and 7 have no registers, they are used to reset the read and write pointers and to read the other port's mailbox.

There is a difference in the accessing forms between the two registers in address 0 and all the other registers.

The two registers in address 0 are accessed directly when the C/D input is high, and WR or RD is LOW:

C/D=H, WR=L will write to the Pointer register.  
 C/D=H, RD=L will read from the status register.

Accessing the other registers has two stages:

1. Writing an address to the Pointer register which will point to the desired register.
2. Writing or reading data to / from the register addressed by the pointer.

After the second stage has been finished, the pointer is automatically cleared to 0 and ready for a new writing or reading. Two successive reads from the status register will assure that the pointer is cleared.

## Pointer Register (Fig. 2)

### A2-A0

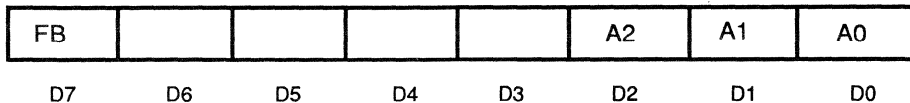
The Pointer register contains 3 address bits A2-A0. These bits select which of the registers will be read or written during the next command access. After master reset the contents of the pointer is zero and the first access to the registers will always be to the pointer (by write) or to the status register (by read).

The next read or write accesses a register addressed by the pointer A2 - A0 bits. The pointer address bits are reset after the read or write to the addressed register is completed.

### FB

Framing bit ; This bit is used to write a framing bit to the FIFO. The bit is set by writing twice to the pointer while D7=1.

The next write to the FIFO will write the data byte together with a framing bit. The FB bit will reset automatically after the data byte is written to the FIFO.



1029 05

Figure 2. Pointer Register

## Status Register (Fig. 3)

Each port has a status register, it is read by the port to determine the meaning of any interrupt. Reading the status register will clear the  $\overline{IRQ}$  flag, except of an interrupt caused by the mailbox. A mailbox interrupt will be cleared by reading the mailbox.

While "shift" bit in the command register is "1", the status register will display the other port's FULL, EMPTY, AF and AE flags.

The status register has the following flags:

### MR

Master reset; the flag is set when one of the ports has reset the part by writing a master reset command to its command register. The part can be reset by either of the two ports. Only reading the status register of the port which sets the MR will terminate the master reset command. However, the other port has to read its status register to reset the MR bit.

### FULL

The FIFO is full, every write command will be ignored. The interrupt flag is maskable but the status bit will reflect the true state.

### EMPTY

The FIFO is empty, every read command will be ignored. The interrupt flag is maskable but the status bit will reflect the true state.

### AF

Almost Full; The flag is set when the write pointer reaches the limit which was programmed in the Almost Full / Almost Empty register.

### AE

Almost Empty; The flag is set when the read pointer reaches the limit which was programmed in the Almost Full / Almost Empty register.

### MB

Mailbox interrupt request from one port to the other—requests to read new data in the mailbox. The flag is set by writing to the mailbox (by the other port), the flag is cleared by reading the other port's mailbox.

### BDT

Byte detect; the flag is set when the port is reading from the FIFO a preprogrammed byte in the BDT register. The flag is cleared by reading the Status register.

### PE/FD

Parity error or frame detect;

In port A it is always frame detect.

In port B it will be a Parity Error bit when the parity checker is enabled, or a Frame Detect bit when the parity checker is disabled.



1029 06

Figure 3. Status Register

### Command Register (Fig. 4)

The Command register of port A is different from port B because the parity generator is in port B only.

#### MR

Software Master Reset — Either port can reset the FIFO by writing a “1” to the MR bit in its Command register. To prevent erroneous resets, the port must write the MR=1 twice, and only then it will be recognized as a master reset. The MR command will be terminated by reading the status register by the port which originated the MR.

#### SHIFT

The shift bit is used to display the other port’s FULL, EMPTY, AF and AE flags. After a master reset the shift bit is reset and the status register will show the own port’s flags. When a CPU on one port sets this bit, the status register will show the other port’s FULL, EMPTY, AF and AE flags.

#### PEN

Parity enable in port B only. The port sets this bit to enable the parity checker/generator, when this bit is reset, the parity generator/checker is generating and checking the framing bit.

#### PO/PE

Parity odd or even selection.

PO/PE = H - odd parity.

PO/PE = L - even parity.

#### BP

Bypass mode selection in port A Command register only. Selects the functioning of Am4701 as a FIFO or as a transparent buffer.

BP = “1” - Bypass mode

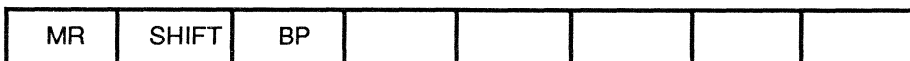
BP = “0” - FIFO mode.

### BDT Register

The byte detect register contains a programmable byte that the port wants to detect while reading the FIFO. When the byte is detected and the mask is enabled, the BDT flag and the  $\overline{IRQ}$  output will be set. The flag is cleared by reading the status register.

### Mailbox

Every port has a 8 bit mailbox to write messages to the other port. By writing new data to port A(B)’s mailbox, port B(A)’s MB bit in its status register and  $\overline{IRQ\_B(A)}$  flag will be set. The flags will be cleared by port B(A)’s reading its mailbox. Every port is allowed to read either mailbox, but can write to its own mailbox only.



Port A Command Register



Port B Command Register

1029 07

Figure 4. Command Registers

### Mask Register (Fig. 5)

The mask register masks the flags which will generate the interrupt request  $\overline{IRQ}$ . A zero in the register masks the interrupt for this flag. After master reset the mask bits are set for FULL and EMPTY and reset for all the other flags. The MR is the only unmaskable flag and will always cause an interrupt.

#### FULL/EMPTY

The FULL and EMPTY flags are nonmasked after a master reset, the flags will be masked after writing a zero to the appropriate bits.

#### AF, AE

Almost full, almost empty flags.

#### MB

Mailbox interrupt request from other port.

**BDT**

Byte detected, the byte read from the FIFO is equal to the byte preprogrammed in the BDT register

**PE/FD**

Parity error or frame detected.

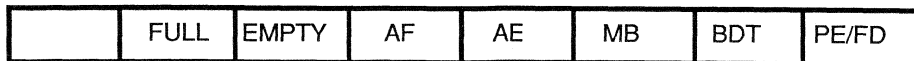


Figure 5. Mask Registers

1029 08

**AF/AE Programmable Register (Fig. 6)**

Every port can program the limit of its AF and AE flags. The programming is done in increments of 16. After the master reset the register is automatically set to 00H which will set the AF and AE flags at 16 writes before FULL and 16 reads before EMPTY.

The AF flag is programmable in increments of 16, from 16 to 256 writes before FULL by the four AF3–AF0 bits.

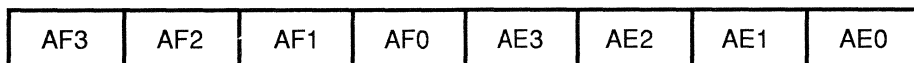
The AE flag is programmable in increments of 16, from 16 to 256 reads before EMPTY by the four AE3–AE0 bits.

**Reset Read / Write Pointers**

The read and write pointers of either ports can be reset by writing to register 6 or 7 of that port respectively with any data. The reset of the pointers is used to overwrite or read again an errored block.

Resetting the Read/Write pointers will cause erroneous AF, AE flags. Only a master reset or a reset of all the four pointers (in port A and B) will cause correct AF, AE flags.

It is recommended to mask the AF and AE flags in the mask register when using this mode.



1029 09

Figure 6. AF/AE Programming Registers

2

**APPLICATIONS**

The Am4701 provides an asynchronous 2-512x8 bit FIFO buffer between two CPUs or between a CPU and a peripheral device. The Am4701 is located on a board together with one CPU which is connected to the Am4701 by 8 data bits.

The other CPU may be on the same or on another board and can be connected in one of the following modes:

1. 8-bit data only.
2. 8-bit data and a parity bit.

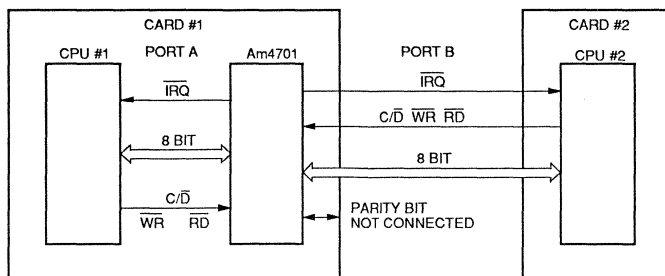
**I. 8-Bit Connection (Fig. 7)**

The 8-bit connection is allowed for communication between two CPUs. In this mode the parity pin at port B is not connected and the Am4701 transfers 8 bits of data only.

**II. 8-Bit Data with Parity (Fig. 8)**

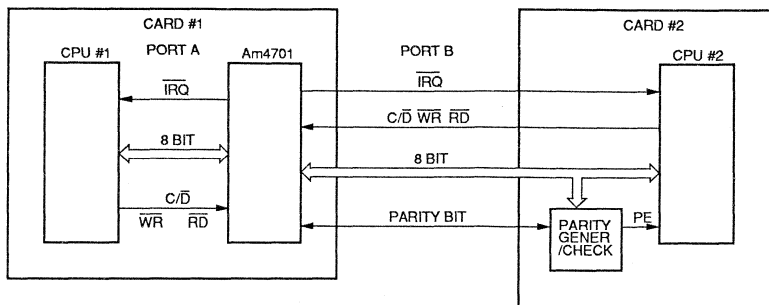
This mode is used to connect two CPUs on two separate cards. Am4701 and CPU #1 are on the same card. The CPU #2 on card #2 must have a parity Generator/Checker.

The built in Parity Generator/Checker of Am4701 will be used by CPU #1. With Am4701 in parity mode, the data



1029 10

Figure 7. 8-Bit Connection



1029 11

Figure 8. 8-Bit with Parity

written by CPU #1 will be available at port B with parity bit (parity generated by Am4701).

While transferring data from CPU #2 to CPU #1, the built in parity checker in Am4701 will check the parity coming from card #2. CPU #2 will get an interrupt (IRQ\_B) if it has written data with parity error. CPU #1 will also get an interrupt (IRQ\_A) while reading the data with parity error.

### III. Bypass Mode — CPU Connected to a Peripheral (Fig 9)

This mode is used to transfer data or commands between a CPU and a programmable peripheral through the Am4701. In this mode the Am4701 behaves like a transparent buffer.

For example a USART, we can send the commands and read the status of the USART in the bypass mode, the data will be sent through the FIFO in both direction.

The  $\overline{RD}$ ,  $\overline{WR}$ ,  $C/\overline{D}$  to the peripheral and the Am4701 will be generated by a PAL or any other discrete logic. The PAL gets address lines from the CPU, decodes them and generates  $\overline{RD}$ ,  $\overline{WR}$ ,  $C/\overline{D}$  signals depending on the address.

#### A. FIFO Mode

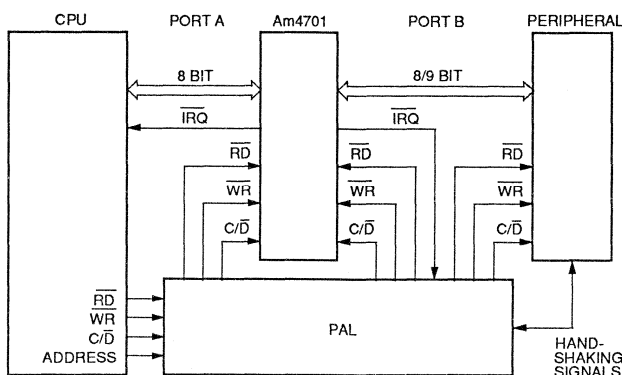
The FIFO mode is selected by resetting the BP bit in port A command register. In this mode the data written/read by the CPU will be transferred through the FIFO.

The control signals to port A, B of the Am4701 and to the peripheral will be generated by the PAL according to the handshaking signals between the peripheral and the PAL.

#### B. Bypass Mode

The Am4701 gets into the bypass mode by setting the BP bit in port A command register. From this point the Am4701 behaves like a bidirectional buffer, data passes directly from port A to port B.

The BYPASS mode can be used for writing commands to port B internal registers by the CPU in port A. The CPU transfers the data from port A to port B in the bypass mode and the  $\overline{RD}$  or  $\overline{WR}$  signals are generated by the PAL. The PAL generates the signals according to the address inputs from the CPU.



1029 12

Figure 9. Bypass Mode



## ABSOLUTE MAXIMUM RATINGS\*

Supply Voltage, $V_{CC}$ .....	-0.5 V to 7.0 V
DC Input Voltage, $V_I$ .....	-0.5 V to $V_{CC} + 0.5$ V
Storage Temperature, $T_S$ .....	-65 to +150°C
Power Dissipation .....	1 W
DC Output Current .....	50 mA

\* Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## OPERATING RANGES

Commercial (C) Devices	
Temperature ( $T_A$ ) .....	0 to +70°C
Supply Voltage ( $V_{CC}$ ) .....	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Commercial			Unit
				Min.	Typ.	Max.	
$V_{IL}$	Low-level input voltage	Note 1				0.8	V
$V_{IH}$	High-level input voltage	Note 1		2			V
$I_{IN}$	Input current	$V_{CC} = \text{MAX}$	$V_I = \text{GND}$ OR $V_{CC}$			10	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 6 \text{ mA}$			0.4	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = 2 \text{ mA}$	2.4			V
$I_{OZ}$	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = \text{GND}$ OR $V_{CC}$			10	$\mu\text{A}$
$I_{CC}$	Quiescent supply current	$V_{CC} = \text{MAX}$	$V_I = \text{GND}$ OR $V_{CC}$			15	mA
$I_{CC}$	Max. Freq. supply current	$V_{CC} = \text{MAX}$	$V_I = \text{GND}$ OR $V_{CC}$			100	mA

2

## Capacitance ( $0^\circ\text{C} < T_A < +70^\circ\text{C}$ )( $V_{CC} = 5.0 \text{ Volts} \pm 10\%$ )

Symbol	Parameter	Conditions	Typ.	Units	Notes
$C_1$	Capacitance on Input Pins	$V_{IN} = 0 \text{ V}$	5	pF	2
$C_0$	Capacitance on Output pins	$V_{OUT} = 0 \text{ V}$	7	pF	2

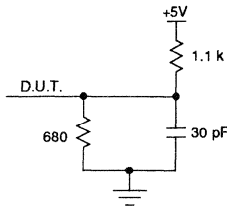


Figure 10.

### Notes:

- These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- For reference only.

1029 13

**Switching Characteristics** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ )

No.	Symbol	Parameter	Commercial		Unit	Notes
			Min.	Max.		

**Read Cycle** (Fig. 11)

1	$t_{RC}$	Read Cycle time	60		ns	
2	$t_{RA}$	Read Access time		45	ns	
3	$t_{RAP}$	Read Access time with Parity		55	ns	
4	$t_{RPW}$	Read Pulse width	45		ns	
5	$t_{RR}$	Read recovery time	15		ns	
6	$t_{OH}$	Output Hold after RD	5		ns	
7	$t_{LZ}$	$\overline{RD}$ Low to Output Active	5		ns	
8	$t_{HZ}$	$\overline{RD}$ High to Output Disable		30	ns	
9	$t_{AH}$	$C/\overline{D}$ Hold time after $\overline{RD}$ or $\overline{WR}$	5		ns	
10	$t_{AS}$	$C/\overline{D}$ Set Up time to $\overline{RD}$ or $\overline{WR}$	5		ns	
11	$t_{RCS}$	Write end to begin Read	30		ns	1
	$t_F$	Input Rise and Fall times		5	ns	

**Write Cycle** (Fig. 12, 21, 22)

12	$t_{RCH}$	Read end to begin Write	30		ns	1
13	$t_{WC}$	Write Cycle time	60		ns	
14	$t_{WP}$	Write Pulse Width	45		ns	
15	$t_{DW}$	Data Set Up to $\overline{WR}$	30		ns	
16	$t_{DH}$	Data Hold time after $\overline{WR}$	5		ns	
17	$t_{WR}$	Write recovery time	15		ns	
18	$t_{FL}$	Fall through time	60		ns	2

**Notes:**

1. This parameter refers to read/write on the same port.
2. See Fig. 21 and 22.

## Switching Characteristics

No.	Symbol	Parameter	Commercial		Unit	Notes
			Min.	Max.		

### IRQ and Flag Timing (Fig. 13, 14, 15, 16)

21	$t_{WLIL}$	Write LOW to $\overline{IRQ}$ LOW				
	$t_{WLIL}$	Write LOW to FULL flag Set		55	ns	
	$t_{WLIL}$	Write LOW to AF flag Set		75	ns	
22	$t_{WHIL}$	Write High to $\overline{IRQ}$ LOW				
	$t_{WHIL}$	Write HIGH to PE flag Set		45	ns	
	$t_{WHIL}$	Write HIGH to MB flag Set		45	ns	
23	$t_{RHH}$	Read status HIGH to /IRQ HIGH		45	ns	
24	$t_{RLIL}$	Read LOW to $\overline{IRQ}$ LOW				
	$t_{RLIL}$	Read to EMPTY flag Set		55	ns	
	$t_{RLIL}$	Read to AE flag Set		75	ns	
25	$t_{RHIL}$	Read High to $\overline{IRQ}$ LOW				
	$t_{RHIL}$	Read to FD flag Set		45	ns	
	$t_{RHIL}$	Read to BDT flag Set		45	ns	
26	$t_{RLIH}$	Read to MB flag reset		45	ns	

### Bypass Timing (Fig. 17, 18)

27	$t_p$	Propagation delay	60		ns	
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2

## SWITCHING WAVEFORMS

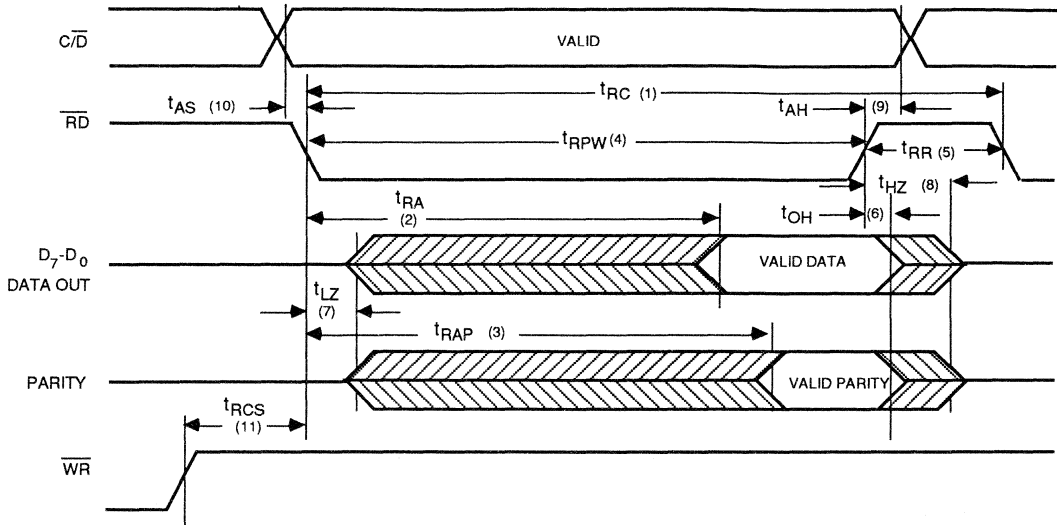


Figure 11. Read Cycle (Either Port)

11120-001B

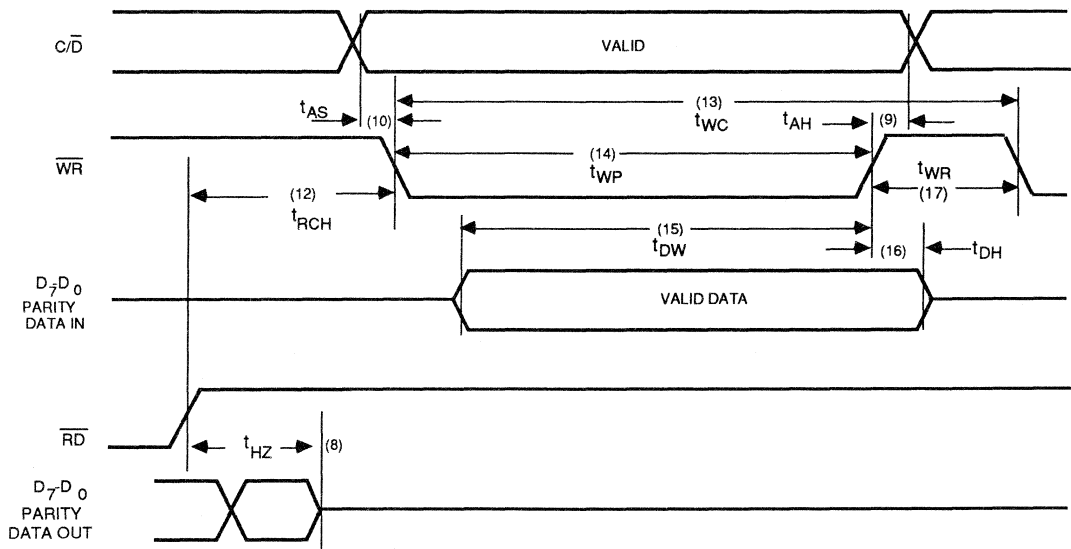


Figure 12. Write Cycle (Either Port)

11120-002B

## SWITCHING WAVEFORM

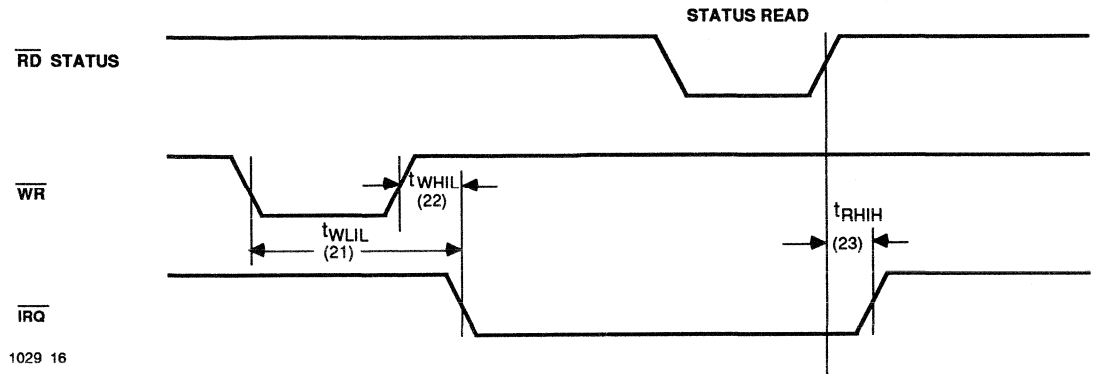


Figure 13. Setting IRQ by FULL, AF, MB, PE flags from FIFO (note 1).

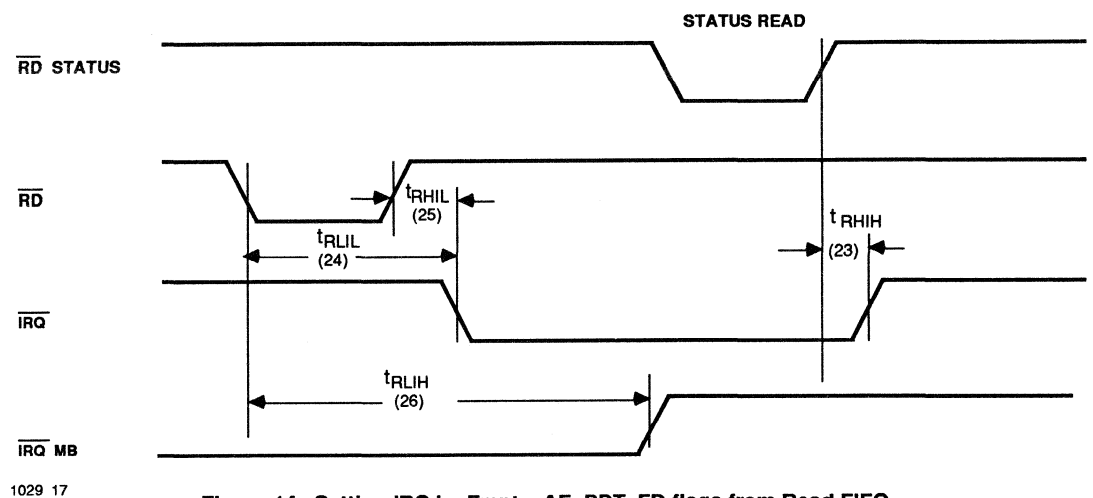


Figure 14. Setting IRQ by Empty, AE, BDT, FD flags from Read FIFO.

Note 1: The MB flag is set by writing to the mailbox and reset by reading mailbox

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## SWITCHING WAVEFORM

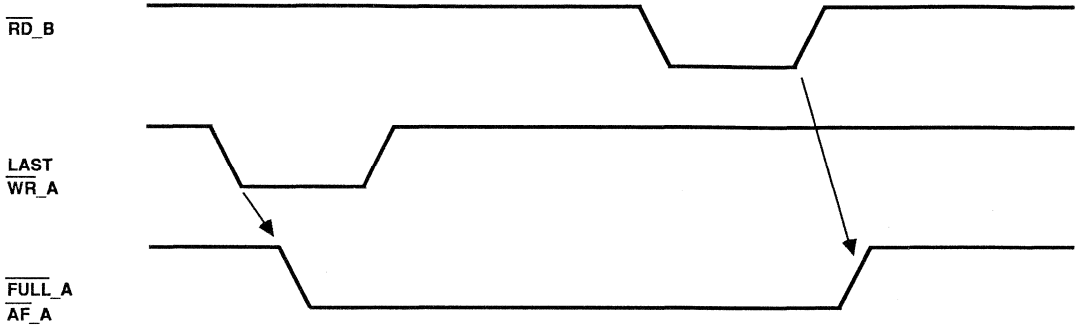


Figure 15. FULL, AF, flags from Read/Write FIFO (note 1).

1029 18

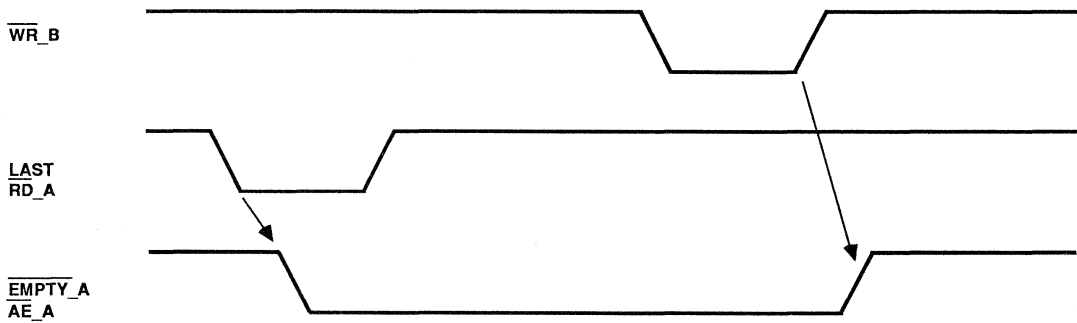
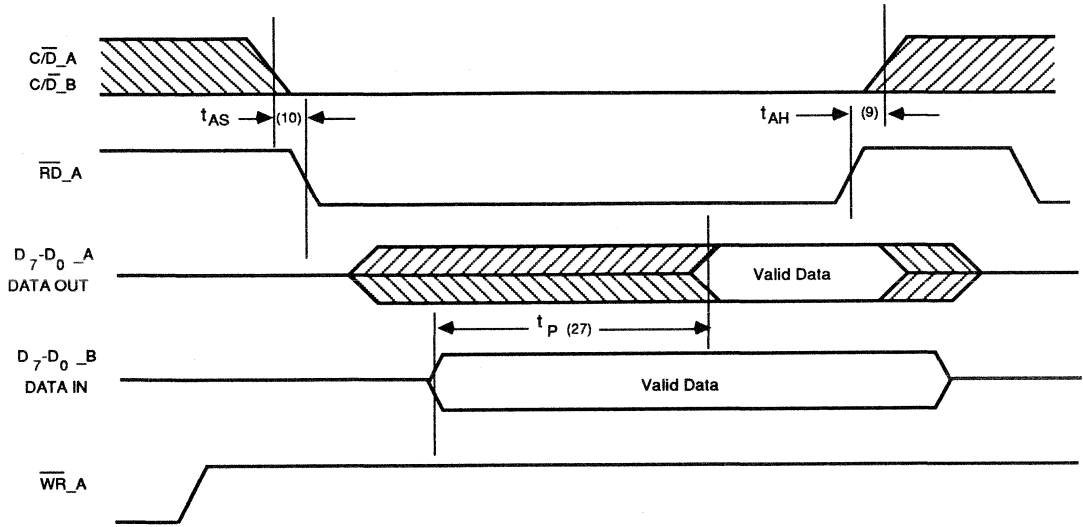


Figure 16. Setting EMPTY, AE, flags from Read/Write FIFO (note 1).

1029 19

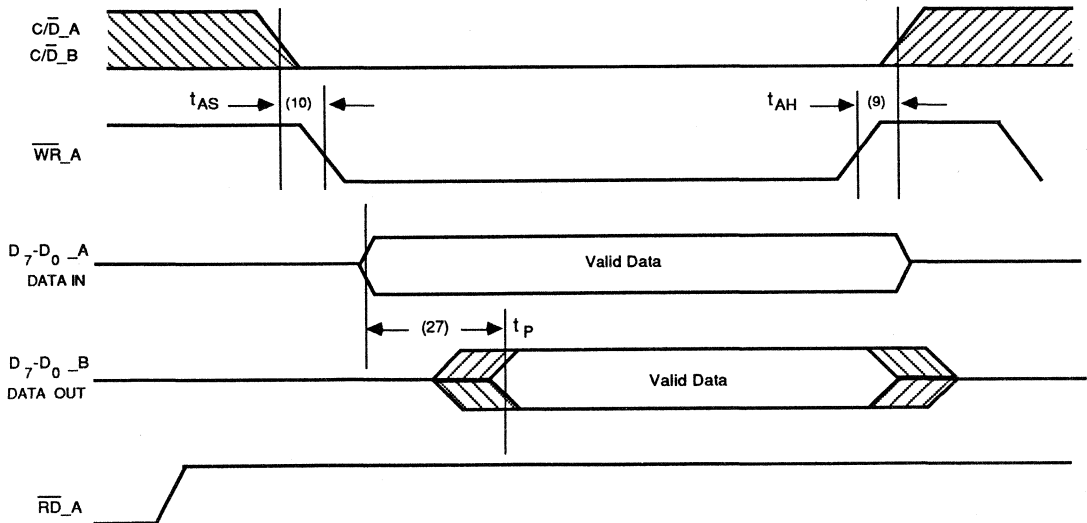
Note 1: The flags setting time can not be measured directly because the flags do not have output pins.

## SWITCHING WAVEFORM



11120-003B

**Figure 17. Bypass Mode-Read Data from B to A Bus**  
( $\bar{RD}_B=X, \bar{WR}_B=X$ )\*



11120-004B

**Figure 18. Bypass Mode-Writing Data from A to B Bus**  
( $\bar{RD}_B=X, \bar{WR}_B=X$ )\*

\*Refer to Table 1: Bypass Mode Truth Table. X = Don't care.

## SWITCHING WAVEFORM

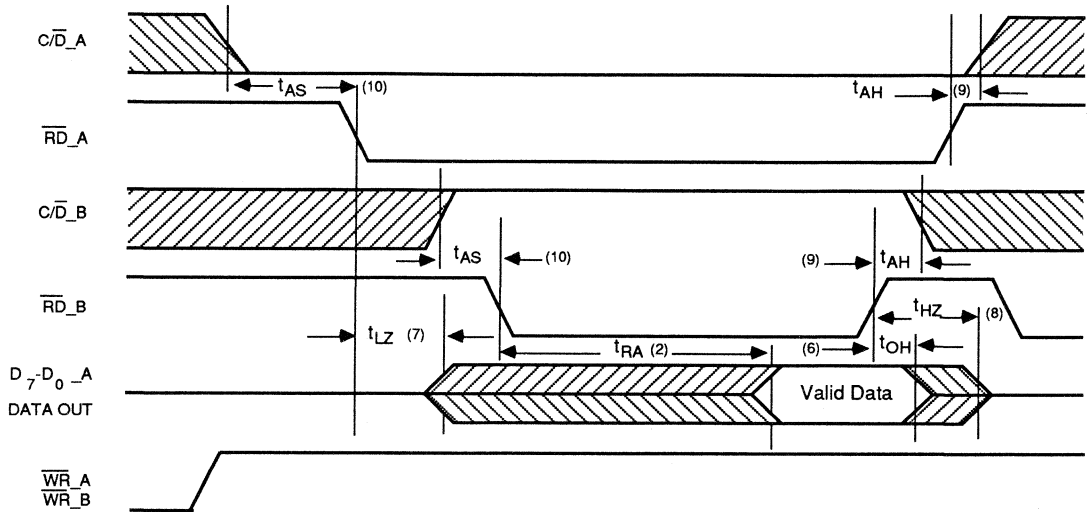


Figure 19. Bypass Mode-Reading Data From B Registers\*

11120-005B

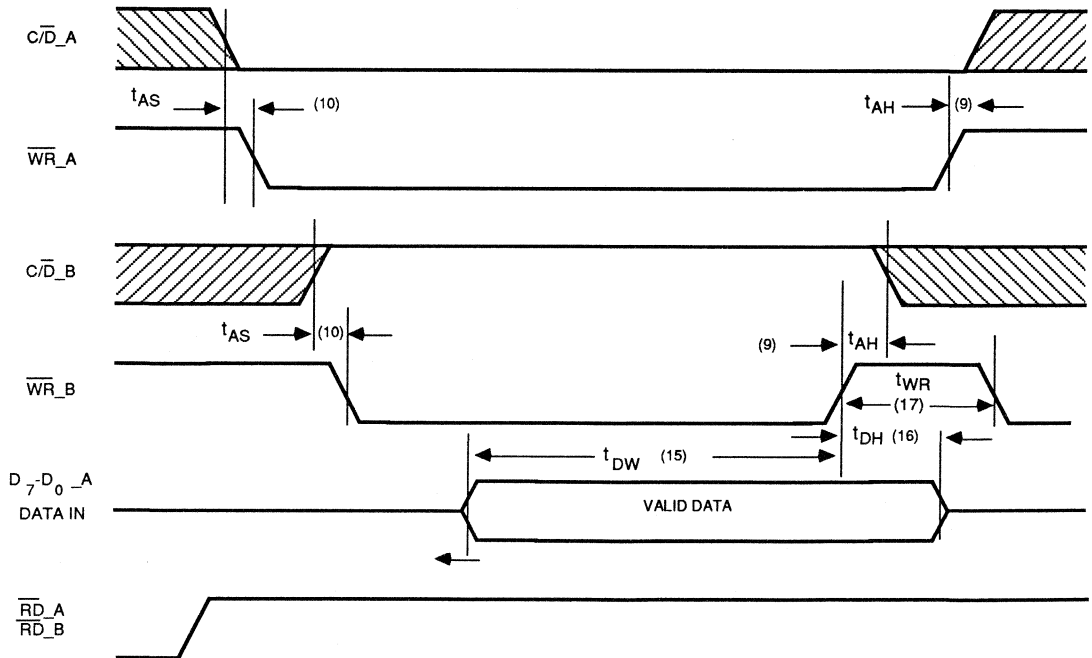


Figure 20. Bypass Mode-Writing Data To B Registers\*

11120-006B

\*Refer to Table 1: Bypass Mode Truth Table.



# SWITCHING WAVEFORM

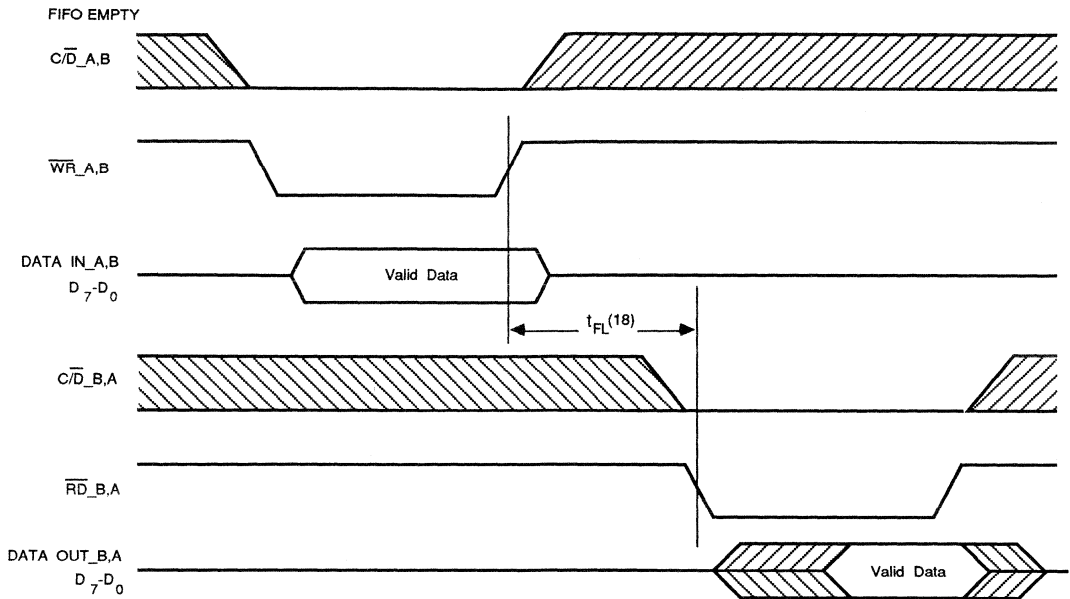


Figure 21. Read Data Flow Through

11120-007B

2

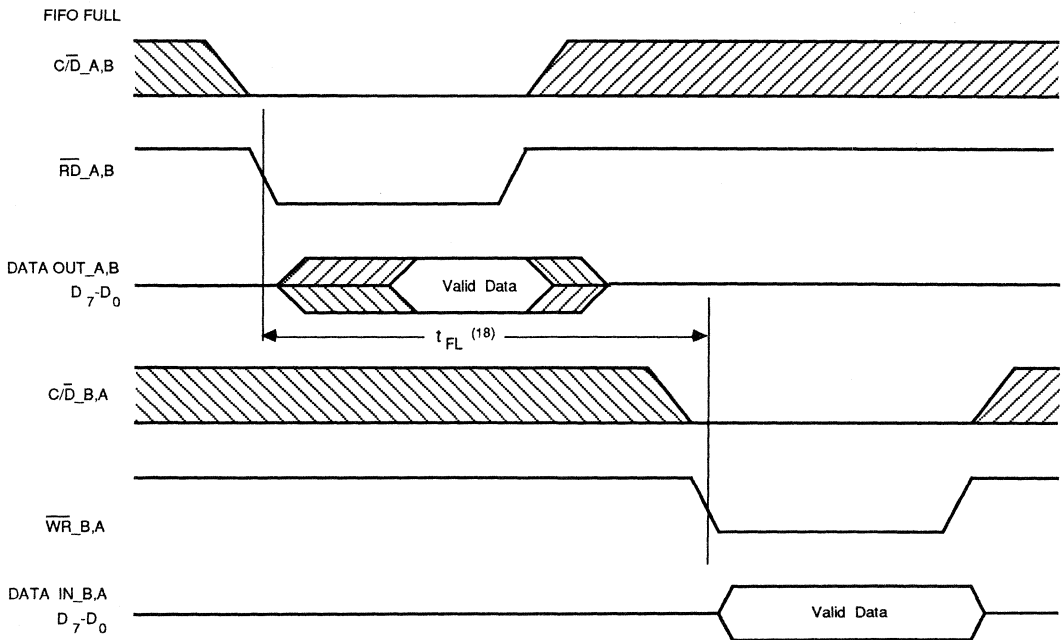


Figure 22. Write Data Flow Through

11120-008B

# Military Specialty Memory

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Whatever your military data buffering needs, Advanced Micro Devices has the right specialty memory device to fit your application. All of our military bipolar and CMOS First-in First-out (FIFO) memories are fully screened to MIL-STD-883.

## Bipolar Military FIFOs

The 57401 and 57402 standard bipolar FIFOs feature 64 words by 4-bit and 64 words by 5-bit architectures. Words can be asynchronously loaded and unloaded from these FIFOs at 7 MHz. Standard FIFOs are offered in enhanced 10 MHz versions, the 57401A and 57402A. Both standard and enhanced FIFOs are available as standalone and cascadable devices. Cascadable FIFOs are expandable in word width and depth. AMD's bipolar process has been proven to be radiation-tolerant at neutron fluences up to  $1 \times 10^{13}$  neutrons/cm<sup>2</sup>. The process has also shown typical recovery times of 50 to 70  $\mu$ s from a 1  $\mu$ s pulse at a dose rate of  $2 \times 10^{10}$  RADs (Si)/s.

## High Performance FIFO

The 57413A is AMD's fastest military FIFO. It offers a full 25 MHz shift-in/shift-out rate, for performance-critical applications. Other features include three-state outputs and status flags. Two flags, Half-Empty and Almost Empty/Full alert the system when the FIFO is half full (32 words or more), almost empty (8 words or less), or almost full (56 or more words).

## CMOS FIFO Family

AMD's family of zero-power CMOS FIFOs will offer the ultimate in speed and low power. All five new devices are fully cascadable for easy expansion in word width and depth. They feature asynchronous shift-in/shift-out rates of 12 MHz with extremely low power consumption. When in standby (quiescent) mode, these devices consume only 550  $\mu$ watts of power. The active power dissipation is equally impressive. At maximum frequency (12MHz) military CMOS FIFOs require only 40 mA.

The CMOS FIFOs employ a static RAM-based memory array which allows them to operate with an extremely short fall-through time. Designers with high speed requirements will not have to

wait for the ripple-through delay associated with register-based FIFOs. In addition, AMD's CMOS FIFOs offer fully-TTL compatible inputs and outputs.

The 57C401 and 57C402 are organized like the standard 64x4 and 64x5 FIFOs, but add enhanced speed and reduced power. These parts are designed for applications in systems where higher speed and zero power is a requirement.

The 57C4013 and 57C4023 resemble the 'C401 and 'C402 but also offer three-state outputs. The ability to turn off the FIFO outputs is useful in testing and in on-board bus applications.

The 57C4033 is a unique 64x5 device which offers status flags in addition to three-state outputs. The two flags, Half-Empty and Almost Empty/Full operate in the same manner as on the 57413A.

AMD will soon offer a line of high density CMOS FIFOs: the Am7200 (256x9), Am7201 (512x9), Am7202 (1Kx9), and Am7203 (2Kx9) buffer memories. These devices feature static-RAM-based architectures specially tailored for applications requiring increased depth. They feature a 40-ns access time and 25-mA standby power. Our high density FIFOs are fabricated on AMD's proprietary poly-load CMOS process.

## Uses of FIFOs

AMD's military FIFOs are a simple, economical way of matching the instantaneous data rates of two digital systems. Examples are dual microprocessor systems where the FIFO keeps transmitting microprocessor "free" by storing the data for the second processor in advance. The first processor is able to load the data as a block and continue with other tasks, and the second can receive the data from the FIFO as it is required. A similar situation might occur in a display system where a general-purpose microprocessor sends data to a specialized graphics processor.

In many aircraft, a central computer supervises several distributed microprocessors which, in turn, control subsystems such as weapons, targeting, radar, and displays. The use of FIFOs as serial data buffers to these subsystem microprocessors allows the central processor to prepare and send data quickly, freeing it to move on to the next task.

# First-In First-Out Devices Selector Guide (MIL)



## Low Density FIFOs

Technology	Part Number	Organization	Type	Max Data Rate, MHz	Max I <sub>CC</sub> , mA	Package Type	Pin Count	Features
B	C57401	64x4	C	7	160	J, L	16, 20 (LCC)	TPO
B	57401	64x4	S	7	160	J, L	16, 20 (LCC)	TPO
B	C57401A	64x4	C	10	180	J, L	16, 20 (LCC)	TPO
B	57401A	64x4	S	10	180	J, L	16, 20 (LCC)	TPO
B	C57402	64x5	C	7	180	J, L	18, 20 (LCC)	TPO
B	57402	64x5	S	7	180	J, L	18, 20 (LCC)	TPO
B	C57402A	64x5	C	10	200	J	18, 20 (LCC)	TPO
B	57402A	64x5	S	10	200	J	18, 20 (LCC)	TPO
C	57C401-12	64x4	C	12	40	J	16	TPO Low Power, RAM Based
C	57C4013-12	64x4	C	12	40	J	16	TPO Low Power, RAM Based
C	57C402-12	64x5	C	12	40	J	18	TPO Low Power, RAM Based
C	57C4023-12	64x5	C	12	40	J	18	TPO Low Power, RAM Based
C	57C4033-12	64x5	C	12	40	J	20	TPO Low Power, RAM Based, Status Flags
B	57413A	64x5	S	25	240	J	20	TPO, Status Flags

2

## High Density FIFOs †

Technology	Part Number	Organization	Type	Max Data Rate, MHz	Max I <sub>CC</sub> , mA	Package Type	Pin Count	Features
C	Am7200-80	256x9	C	10	90	X	28	TPO Access Time = 80 ns, Status Flags
C	Am7200-65	265x9	C	12	90	X	28	TPO Access Time = 65 ns, Status Flags
C	Am7200-50	265x9	C	15	90	X	28	TPO Access Time = 50 ns, Status Flags
C	Am7200-40	265x9	C	20	100	X	28	TPO Access Time = 40 ns, Status Flags
C	Am7201-80	512x9	C	10	90	X	28	TPO Access Time = 80 ns, Status Flags
C	Am7201-65	512x9	C	12	90	X	28	TPO Access Time = 65 ns, Status Flags
C	Am7201-50	512x9	C	15	90	X	28	TPO Access Time = 50 ns, Status Flags
C	Am7201-40	512x9	C	20	100	X	28	TPO Access Time = 40 ns, Status Flags
C	Am7202-80	1Kx9	C	10	90	X	28	TPO Access Time = 80 ns, Status Flags
C	Am7202-65	1Kx9	C	12	90	X	28	TPO Access Time = 65 ns, Status Flags
C	Am7202-50	1Kx9	C	15	90	X	28	TPO Access Time = 50 ns, Status Flags
C	Am7202-40	1Kx9	C	20	100	X	28	TPO Access Time = 40 ns, Status Flags
C	Am7203-80	2Kx9	C	10	90	X	28	TPO Access Time = 80 ns, Status Flags
C	Am7203-65	2Kx9	C	12	90	X	28	TPO Access Time = 65 ns, Status Flags
C	Am7203-50	2Kx9	C	15	90	X	28	TPO Access Time = 50 ns, Status Flags
C	Am7203-40	2Kx9	C	20	100	X	28	TPO Access Time = 40 ns, Status Flags

Notes:

Technology:

B – Bipolar  
C – CMOS

C – Cascadable  
S – Standalone

PackageType:

X, J - Ceramic DIP  
L - Ceramic Leadless Chip Carrier  
W - Ceramic Flat Pack

Features:

TPO – Three State Output  
TPO – Totem Pole Output

† In development.

## Military Specialty Memory

### JAN 38510 and Standard Military Drawing Program

AMD is an active participant in the JAN 38510 and Standard Military Drawing (SMD) Program. The idea behind the SMD Program is to standardize MIL-STD-883, Class B microcircuits where fully qualified JAN product is not available. The advantage to the user is that SMDs are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.

Standard Military Drawings should always be considered to improve availability over source control drawings. It is standard practice at AMD to convert our 883, Class B processing to SMDs

for all products which we are approved to supply. AMD then dual marks these devices with both the SMD number and the Generic Part Number. DESC approved products can then be procured to either part number as standard product through both OEM and Distributor channels.

The following cross reference will allow you to determine the appropriate SMD and JAN Drawing for each FIFO device. AMD will continue to work closely with the DESC, generating new drawings, which will provide a steady flow of advanced technology products to standardized specifications.

### MIL-M-38510 Slash Sheet Cross Reference for AMD Generic Part Number

M38510	01	02	03	04	05	06	07	08	09	10
503	10H8	12H6	14H4			10L8	12L6	14L4		
504	16L8A	16R8A	16R6A	16R4A			16L8A-2	16R8A-2	16R8A-2	16R4A-2
505	20L8A	20R8A	20R6A	20R4A						

### Standard Military Drawing Generic Part Type Cross Reference

STANDARD MILITARY PART NUMBER	GENERIC PART NUMBER	JAN REPLACEMENT NUMBER
5962-8779101EX	57401J/883B	—
5962-87791012X	57401L/883B	—
5962-8779102VX	57402J/883B	—
5962-87791022X	57402L/883B	—
5962-8779103EX	57401AJ/883B	—
5962-87791032X	57401AL/883B	—
5962-8779104VX	57402AJ/883B	—
5962-87791042X	57402AL/883B	—
5962-8779105EX	C57401J/883B	—
5962-87791052X	C57401L/883B	—
5962-8779106VX	C57402J/883B	—
5962-87791062X	C57402L/883B	—
5962-8779107EX	C57401AJ/883B	—
5962-87791072X	C57401AL/883B	—
5962-8779108VX	C57402AJ/883B	—
5962-87791082X	C57402AL/883B	—

MMI PACKAGE DESIGNATOR	PACKAGE TYPE	STANDARD LEAD FINISH	MIL-SPEC LEAD FINISH DESIGNATOR
J/JS	CERAMIC DIP	SOLDER DIP	A
W	CERAMIC FLATPACK	SOLDER DIP	A
L	CERAMIC LEADLESS CHIP CARRIER	SOLDER DIP	A

### Product Introduction Procedures

All new products released by the Military Products Division must successfully pass Mil-Std-883 Class B processing prior to new product announcement. This practice allows us to do checkout of bonding diagrams, electrical test tapes and burn circuits in a manufacturing environment. Programmability is checked when applicable. Our Military Engineering Department reviews electrical data to insure performance and yields to military data sheet limits are acceptable, prior to new product release. This procedure allows MPD to keep manufacturing start-up problems to a minimum on new product orders.

### Standard Processing Flows

MPD Processing and Screening flows are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows.

Standard processing flows for the Military Products Division include:

- MPD Modified Level S
- JAN 38510 Class B
- Military Drawing Program
- Mil-Std-883 Class B

In addition, these flows are expanded to provide for factory programming on PAL circuits, when required by our customers.

Major benefits can be realized by ordering product to standard flows whenever possible:

- Minimize need for source control drawings.
- Cost savings on unit cost—no price adders for custom processing.
- Improved lead time—no spec review or negotiation time, plus the ability to pull product from various work-in-process stages or purchase product from finished goods inventory.

For your reference, we have included our Modified Levels flow, our Mil-Std-883 Class B flow and our Mil-Temp Product flow.

It is the policy of AMD, to always operate to the most current revision of Mil-M-38510 and Mil-Std-883.

### Manufacturing and Screening Locations

JAN Products, MPD Modified Level "S", and customer orders which call for U.S.A. assembly, are manufactured in our DESC certified line in Sunnyvale, California.

MIL-STD-883 Class B products, and orders to source control drawings, where stateside build is not required, are assembled at our Penang, Malaysia facility. This facility is qualified by AMD Quality Department, as well as by many of our customers, to manufacture MIL-STD-883 Class B product. Conformance to MIL-STD-883 requirements is routinely monitored through audits at the Penang facility as well as incoming inspections in Sunnyvale. Manufacturing capabilities for each AMD facility are highlighted on the chart below.

To identify the assembly location of each military device, the Country of origin is marked on all products prior to shipment. Products assembled in our stateside facility in Sunnyvale, California, will have "USA" marked on the topside of the device. The exception to this is JAN 38510 product, which is marked to the MIL-M-38510 requirements only.

Offshore built product, which is manufactured in Penang, Malaysia, will have "Malaysia" or "Malay" marked on the bottom side of the device.

### Manufacturing Capabilities

	SUNNYVALE	PENANG
Assembly	X	X
Precap Inspection	X	X
Environmental Testing	X	X
Electrical Pre-Test	X	X
Burn-In	X	X
Post Burn-In Electricals	X	X
Group A Testing	X	X
Mark	X	X
Factory Programming	X	
Qualification and Quality Conformance Testing	X	



## Military Specialty Memory

### STANDARD MILITARY FLOW CHART

Screening	Modified Level S	Requirement	Class B	Requirement
	<b>MIL-STD-883 Method 5004</b>		<b>MIL-STD-883 Method 5004</b>	
S.E.M.	2018	Sample		
Assembly	USA assembly		Typically offshore assembly	
Non-destruct bond pull	2023	100%		
Die shear/ Destruct bond pull	2019 (sample)	SS = 2 REJ = 0		
Internal visual	2010 cond. A (modified)	100%	2010 cond. B	100%
Stabilization bake	1008	100%	1008	100%
Temperature cycling	1010	100%	1010	100%
Constant acceleration	2001 test cond. D or E Y1 orientation only	100%	2001 test cond. D or E Y1 orientation only	100%
Seal A) Fine B) Gross			1014 cond. A or B cond. C	100%
Particle impact noise detection (PIND)	2020 cond. A only	100%		
Interim electrical parameters	Per application device specification $T_A = 25^\circ\text{C}$ only	100%		
Serialization		100%		
X-Ray	2010 two views X and Y axis only	100%		
Interim electrical (1) parameter	Per applicable device specification $T_A = 25^\circ\text{C}$ only	100%	Per applicable device (1) specification $T_A = 25^\circ\text{C}$ only	100%
Burn In	1015 Cond. D $T_A = +125^\circ\text{C}$ (min) Time = 240 hrs	100%	1015 Cond. C or D	100%
Freeze Out	Option			
Post electrical parameters	Per applicable device specification $T_A = 25^\circ\text{C}$ only (delta's when required)	100%	Per applicable device specification $T_A = 25^\circ\text{C}$ only	100%
Delta calculations (when applicable)	Per applicable device specification			
Percent defect allowable	DC Parameters PDA = 5% or 1 device whichever is greater Functional Parameters PDA = 3% or 1 device whichever is greater		DC Parameters PDA = 5% or 1 device whichever is greater	

(1) Programming and verification are performed at  $25^\circ\text{C}$  only.

(2) Unprogrammable PAL Devices – AC parameters are tested on programmed sample.

**Standard Military Flow Chart** (Cont'd.)

SCREENING	MODIFIED LEVEL S	REQUIREMENT	CLASS B	REQUIREMENT
	<b>MIL-STD-883 METHOD 5004</b>		<b>MIL-STD-883 METHOD 5004</b>	
Final electrical parameters (hot and cold extremes)	Per applicable device specification	100%	Per applicable device specification	100%
Sal A) Fine B) Gross	1014 cond, A or B cond C	100%		
Group A lot	5005 Level S. (2)	Per applicable device specification	5005 Class B (2)	Sample every lot
Group B inspection lot Group C Group D External visual	5005 level S not applicable 5005 level S 2009	As required  As required 100%	5005 Class B 5005 Class B 5005 Class B 2009 Generic data available in lieu of lot quality conformance inspection	Every 6 weeks Every 13 weeks Every 26 weeks 100%

(1) Programming and verification are performed at 25°C only.

(2) Unprogrammable PAL Devices—AC parameters are tested on programmable sample.

# Military Specialty Memory

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## Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

- Mil-M-38510, Appendix A, "Product Assurance Program"
- Mil-Q-9858, "Quality Program Requirements"
- Mil-I-45208, "Inspection System Requirements"

AMD facilities in Sunnyvale are certified by the Defense Electronics Supply Center (DESC), to manufacture and qualify Bipolar PROMs and PAL circuits in accordance with Mil-M-38510 Class B. This certification was a result of a successful audit of our production and quality systems to the stringent requirements of MIL-M-38510.

## Quality Assurance

Following 100% screening, the Military Products Division samples all products processed in conformance to Mil-Std-883 Class B, to the following LTPD levels:

Test	LTPD
DC 25°C	2
DC+125°C	3
DC-55°	5
Functional at 25°C	2
Functional at Temperature Extremes	5
AC 25°C	2
AC +125°C	3
AC -55°	5

The Military Products Division ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of MIL-STD-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

For products requiring programming prior to AC tests, testing is performed utilizing MIL-M-38510 slash sheet sample plans.

## Product Qualification/Quality Conformance Inspection (QCI)

The Military Products Division has a quality conformance testing program in accordance with MIL-STD-883, Method 5005. Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that AMD, as a minimum, conduct qualification testing per Company Policy specification on Product Reliability Qualification (00-019). Once qualified, each package type (from each assembly line) and device (by technology group as delineated in MIL-M-38510) are incorporated into AMD Quality Conformance Inspection program which utilizes the requirements of MIL-M-38510.

When military programs do not require that QCI data be run on the specific lot shipped, AMD Quality Conformance program allows customers to obtain generic data on all product families manufactured by the Military Products Division. Generic Qualification Data enables customers to eliminate costly qualification and destruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following product data is available:

### Group B - Package Related Tests

- QCI is performed every 6 weeks of manufacture on each package type.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor assembly and device package integrity.

### Group C - Product/Process Related Tests

- QCI is performed every 13 weeks of manufacture, on representative devices from the same microcircuit group.
- Life test data may be used to qualify similar technologies.
- Purpose: To monitor the reliability of the process and the parametric performance for each product technology.

### Group D - In-Depth Package Related Tests

- QCI is conducted every 26 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.

### Generic Data

AMD's Generic Data Program is based on MIL-M-38510, which allows for shipments based on 26 weeks of coverage for Group C Testing and 36 weeks of coverage for Group D Testing.

Should circumstances arise where generic coverage to MIL-M-38510 is not possible, AMD reserves the right to ship product based on 52 weeks of generic Group C and/or D coverage per MIL-Std-883.

### Process Audits

Process Audits are performed in accordance with Mil-M-38510, Appendix A, (self audits) by the Quality Assurance Department.



### Customer Material Returns

In order to better service our military customers who must return product to the factory, the Military Products Division has established its own customer material returns department. Our goal and policies are outlined below so you may know what to expect when returning product to MPD.

#### Goals

10 day turn-around to respond to a return.

- Notification to the customer of any discrepancy relating to the return.
- For returns which cannot be validated, a written notice of M.P.D.'s intent to return product will be sent to our customer.
- Product returned to our customer will be accompanied by an explanation and/or parametric test data and serialized devices.

#### Standard Policies

- Product which is returned specifically as electrical failures and is not accompanied by test data, will be tested at all three temperatures (-55°C, 25°C, and +125°C)
- If no are failures found, the product will be returned to the customer.
- A device count is done upon arrival of a return at AMD. Credit will be given only for the number of devices received by the factory.
- Product returned by the Franchised Distributor for rescreen or stock rotation will be accepted only if proper traceability paperwork accompanies each lot of product.
- All returns must be sent to 3625 Peterson Way, Santa Clara, CA 95051. Attn: "MPD CMR DEPARTMENT".

#### Information Checklist

The following accompanying a material return will assist us in responding to your return in the shortest possible time.

1. Double check accuracy of device counts.
2. Identify rejects from good devices, when returned together.
3. Supply as much detail as you can about the description of the electrical failure mode (i.e.: AC Fail, DC Fail, FCT Fail, or description of any test numbers used).
4. Whenever possible, identify dissimilar failures or keep separate devices which fail different parameters by serializing failures.
5. Enclose a copy of any data which you may have taken on the failed devices (i.e.: Forcing conditions, temperature tested, parameter and value, an address that failed). List what was expected vs. what was received.
6. For programmability failures, please send programming masters or a truth table. Also please indicate whether single or multiple pulse programming was used and the equipment device was programmed on.
7. What environmental testing was performed.
8. Failure rates.

Although our intent is that our customers will never have to use these guidelines, if a problem should arise, the Military Products Division will strive to disposition and respond to your material return as thoroughly and promptly as possible.

### Electrostatic Discharge Control Procedures

The Military Products Division of AMD fully employs static control procedures throughout its facilities in Penang, Malaysia and Sunnyvale, California.

All manufacturing areas where product is processed or handled, including our Reliability Labs, Engineering Labs, etc., have full static control such as wrist straps, antistatic smocks, grounded stainless steel tables, conductive mats and ion generators whenever necessary.

All product is moved throughout our facilities and shipped to customers in static shielded containers.

In addition, MPD distributors must demonstrate that they meet the same stringent standards regarding ESD handling and control procedures as the factory. Individual distributor locations are audited and approved annually by MPD's Quality Assurance Department.

An ESD identifier is marked on all products in front of the date code, and all shipping containers are labeled with an ESD Caution Message. ESD procedures are continually reviewed, to ensure that our customers receive only the highest quality product from the Military Products Division.

### Radiation Hardness Program

#### 1. Radiation Effects

It has been stated that some level of radiation tolerance will be required in up to 50% of all military applications by 1990. Due to this increased concern over radiation effects on integrated circuits, the Military Products Division has embarked on a program to determine what radiation dose rates our circuits will withstand.

#### 2. Neutron Irradiation

We have successfully completed neutron radiation testing on our Bipolar processes in accordance with Mil-Std-883, Method 1017.2. Eleven different device types, which currently represent all our Bipolar processes, were parametrically and functionally tested at 25°C before and after exposure to fluence levels of  $2 \times 10^{12}$  N/cm<sup>2</sup>,  $1 \times 10^{13}$  N/cm<sup>2</sup>,  $4 \times 10^{13}$  N/cm<sup>2</sup> and  $1 \times 10^{14}$  N/cm<sup>2</sup>. Input low current ( $I_{IL}$ ) is the primary measurement of permanent circuit degradation. The parametric failures ( $I_{LC} > 250 \mu A$ ) seen occurred at relatively high fluence levels. Also, no major changes in  $I_{CC}$  were noted for any circuit.

## Military Specialty Memory

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The following is a list of the device types tested:

53S1681	(2048x8 PROM)
53RA1681A	(2048x8 Registered PROM)
53S3281	(4096x8 PROM)
57401A	(64x4 FIFO)
PAL16R4A	(High Speed Programmable Array Logic)
PAL16R4B	(Very High Speed Programmable Array Logic)
PAL16R4D	(Oxide Isolated Ultra High Speed Programmable Array Logic)
PAL20R4A	(High Speed Programmable Array Logic)
PAL20RA10	(Asynchronous Programmable Array Logic)

All devices passed test limits at  $1 \times 10^{13}$  N/cm<sup>2</sup> level, with the 53RA1681A, 53S3281, and 57401A also passing the  $4 \times 10^{13}$  N/cm<sup>2</sup> fluence level. In addition, the 57401A passed test limits at  $1 \times 10^{14}$  N/cm<sup>2</sup> level.

### 3. Dose Rate Effects

Dose rate data has been obtained on our junction isolated Bipolar processes. All recovered in 50 to 70 microseconds from a 1 microsecond pulse of  $2 \times 10^{10}$  rads (Si) per second.

The products tested were:

PAL14L8	PAL10L8
PAL16L6	PAL12L6
PAL20L10	PAL16L8
PAL20X10	PAL16R8
PAL20X8	PAL16R6
PAL12H6	PAL16R4
PAL14H4	

### 4. Future Radiation Testing

Our future test plans include:

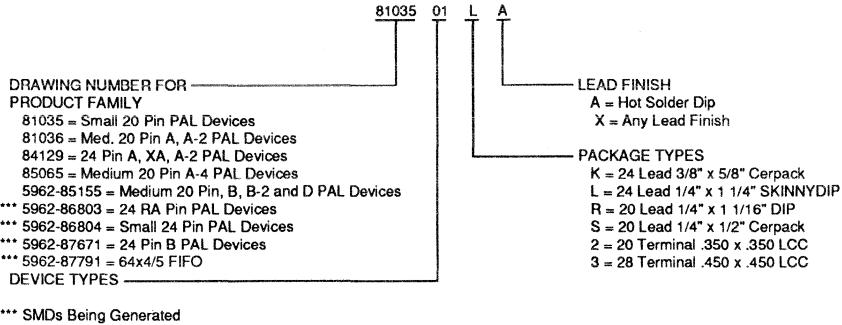
- Total Dose
- Single Event Upset
- Latch-up and Burn-out

AMD's new Bipolar and CMOS processes may be radiation tested after production release.

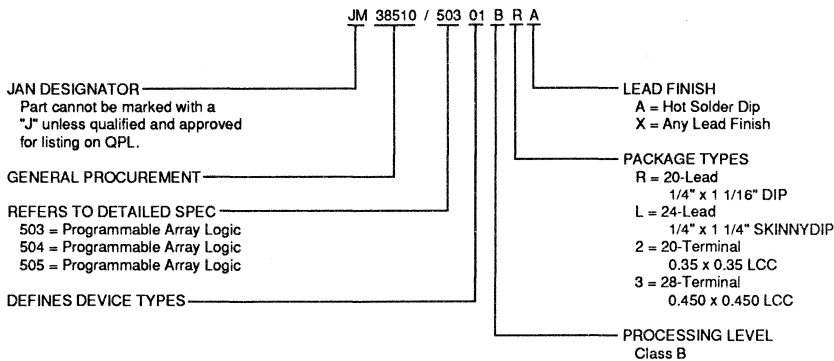
Detailed neutron and dose rate radiation data is available from the Military Products Division.

**JAN 38510 and STANDARD MILITARY DRAWING PROGRAM**

**STANDARD MILITARY DRAWING NUMBERING SYSTEM**



**JAN PART NUMBERING SYSTEM**



**PART NUMBER INTERPRETATION:**

When ordering to JAN 38510 and Military Drawing numbers, the lead finish designator (last letter in part number) is commonly called out as "X". This is a way of stating that the customer will accept the standard manufacturer's lead finish for the package orders. "X" is not a lead finish designator in itself, therefore, when product is shipped, the actual lead finish designator will be marked on the devices.

# C57401 C57401A C57402 C57402A 57401 57401A 57402 57402A

Military Standard FIFOs 64x4 64x5  
Cascadable & Standalone Memory



Advanced  
Micro  
Devices

## DISTINCTIVE CHARACTERISTICS

- Choice of 7 or 10 MHz shift-out/shift-in rates
- Choice of standalone or cascadable devices
- Choice of 4-bit or 5-bit data width
- TTL Inputs and outputs
- Cascadable devices readily expandable in the word and bit dimension
- Standalone devices expandable in the word dimension only
- Structured pinouts. Output pins directly opposite corresponding inputs pins
- Asynchronous operation
- Dose rate (transient upset) junction-isolated bipolar process  $2 \times 10^{10}$  RADs (Si)/s recovery time of 50 to 70  $\mu$ s from a 1  $\mu$ s pulse
- Neutron fluence (permanent damage):  $1 \times 10^{13}$  N/cm<sup>2</sup>

## GENERAL DESCRIPTION

The C/57401/1A and C57402/2A are "fall through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits respectively.

FIFO word width and depth are expandable on cascadable devices. Standalone devices are expandable in word width only.

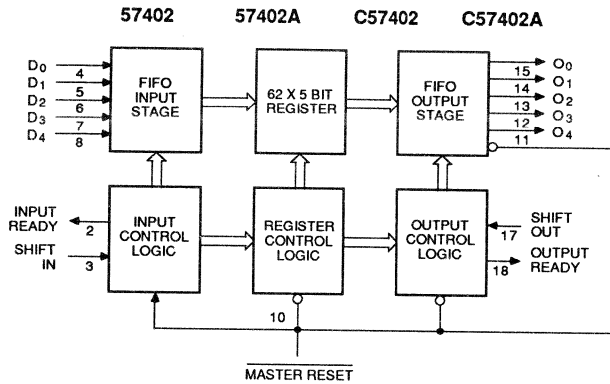
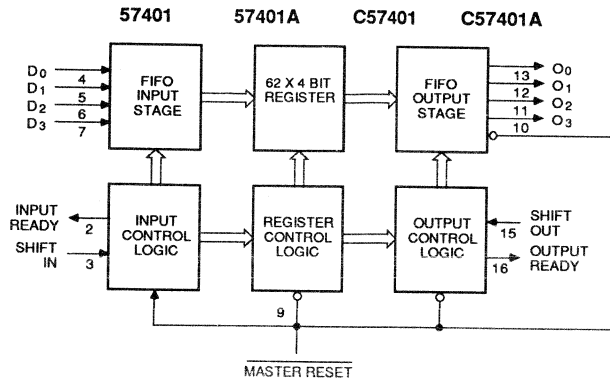
## Ordering Information

PART NUMBER	PINS	PACKAGE	PACKAGE TYPE	MIL-M-38510 CASE OUTLINE	CASCADABLE/STANDALONE	DESCRIPTION
57401*	16	CD 016	Ceramic Dip	D-2	Standalone	7 MHz 64X4 FIFO
		CL 020	Leadless Chip Carrier	C-2	Standalone	
57401A*	16	CD 016	Ceramic Dip	D-2	Standalone	10 MHz 64X4 FIFO
		CL 020	Leadless Chip Carrier	C-2	Standalone	
57402	18	CD 018	Ceramic Dip	D-6	Standalone	7 MHz 64X5 FIFO
		CL 020	Leadless Chip Carrier	C-2	Standalone	
57402A	18	CD 018	Ceramic Dip	D-6	Standalone	10 MHz 64X5 FIFO
		CL 020	Leadless Chip Carrier	C-2	Standalone	
C57401*	16	CD 016	Ceramic Dip	D-2	Cascadable	7 MHz 64X4 FIFO
		CL 020	Leadless Chip Carrier	C-2	Cascadable	
C57401A*	16	CD 016	Ceramic Dip	D-6	Cascadable	10 MHz 64X4 FIFO
		CL 020	Leadless Chip Carrier	C-2	Cascadable	
C57402	18	CD 018	Ceramic Dip	D-6	Cascadable	7 MHz 64X5 FIFO
		CL 020	Leadless Chip Carrier	C-2	Cascadable	
C57402A	18	CD 018	Ceramic Dip	D-6	Cascadable	10 MHz 64X5 FIFO
		CL 020	Leadless Chip Carrier	C-2	Cascadable	

\* Also available in Ceramic Flatpackage. Contact factory for detail.

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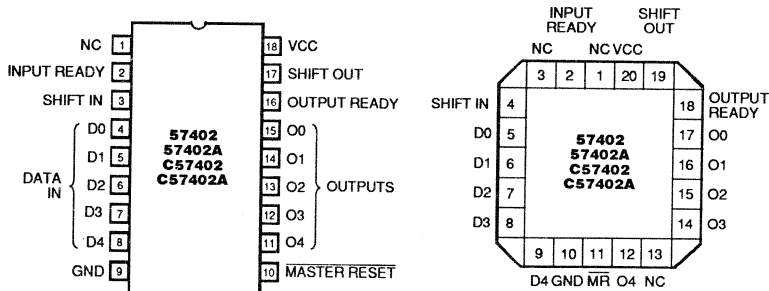
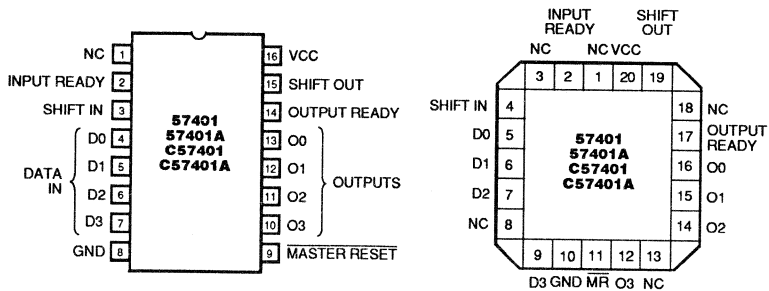
# BLOCK DIAGRAMS DIP Pinout



505 127

**2**

# CONNECTION DIAGRAMS



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## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage .....	-1.5 V to 7 V
Off-state output voltage .....	-0.5 V to 5.5 V
Storage Temperature .....	-65°C to +150°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and a functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## OPERATING CONDITIONS 57401/2

Symbol	Parameter	Figure	Military			Unit
			Min	Typ	Max	
$V_{CC}$	Supply voltage		4.5	5	5.5	V
$T_A^*$	Operating temperature		-55		125	°C
$t_{SIH}^\dagger$	Shift in HIGH time	1	45			ns
$t_{SIL}$	Shift in LOW time	1	45			ns
$t_{IDS}$	Input data setup	1	10			ns
$t_{IDH}$	Input data hold time	1	55			ns
$f_{IN}$	Shift in rate	1	7			MHz
$f_{OUT}$	Shift Out rate	4	7			MHz
$t_{SOH}^\dagger$	Shift Out HIGH time	4	45			ns
$t_{SOL}$	Shift Out LOW time	4	45			ns
$t_{MRW}$	Master Reset pulse <sup>†</sup>	8	30			ns
$t_{MRS}^{**}$	Master Reset to SI	8	45			ns

\* Instant-On Case Temperature

\*\*  $t_{MRS}$  is measured on initial characterization lots only and is not directly tested in production.

## SWITCHING CHARACTERISTICS 57401/2 Over Operating Conditions

Symbol	Parameter	Figure	Military		Unit
			Min	Max	
$t_{IRL}^\dagger$	Shift In to Input Ready LOW	1		60	ns
$t_{IRH}^\dagger$	Shift In to Input Ready HIGH	1		60	ns
$t_{ORL}^\dagger$	Shift Out to Output Ready LOW	4		65	ns
$t_{ORH}^\dagger$	Shift Out to Output Ready HIGH	4		70	ns
$t_{ODH}$	Output Data Hold (previous word)	4	10		ns
$t_{ODS}$	Output Data Shift (next word)	4		65	ns
$t_{PT}$	Data throughput or "fall through"	3, 6		4	μs
$t_{MRORL}$	Master Reset to OR LOW	8		65	ns
$t_{MRIRH}$	Master Reset to IR HIGH	8		65	ns
$t_{IPH}^*$	Input Ready pulse HIGH	3	20		ns
$t_{OPH}^*$	Output Ready pulse HIGH	6	20		ns

† See AC test and high speed application note.

\*  $t_{IPH}$  and  $t_{OPH}$  are measured on initial characterization lots only and are not directly tested in production.

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage .....	-1.5 V to 7 V
Off state output voltage .....	-0.5 V to 5.5 V
Storage temperature .....	-65°C to +150°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and a functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## OPERATING CONDITIONS 57401A/2A

Symbol	Parameter	Figure	Military			Unit
			Min	Typ	Max	
$V_{CC}$	Supply voltage		4.5	5	5.5	V
$T_A^*$	Operating temperature		-55		125	°C
$t_{SIH}^\dagger$	Shift in HIGH time	1	35			ns
$t_{SIL}$	Shift in LOW time	1	35			ns
$t_{DS}$	Input data setup	1	5			ns
$t_{IDH}$	Input data hold time	1	45			ns
$f_{IN}$	Shift in rate	1	10			MHz
$f_{OUT}$	Shift Out rate	4	10			MHz
$t_{SOH}^\dagger$	Shift Out HIGH time	4	35			ns
$t_{SOL}$	Shift Out LOW time	4	35			ns
$t_{MRW}$	Master Reset pulse	8	40			ns
$t_{MRS}^{**}$	Master Reset to SI	8	45			ns

\* Instant-On Case Temperature

\*\*  $t_{MRS}$  is measured on initial characterization lots only and is not directly tested in production.

## SWITCHING CHARACTERISTICS 57401A/2A Over Operating Conditions

Symbol	Parameter	Figure	Military		Unit
			Min	Max	
$t_{IRL}^\dagger$	Shift In to Input Ready LOW	1		50	ns
$t_{IRH}^\dagger$	Shift In to Input Ready HIGH	1		50	ns
$t_{ORL}^\dagger$	Shift Out to Output Ready LOW	4		65	ns
$t_{ORH}^\dagger$	Shift Out to Output Ready HIGH	4		65	ns
$t_{ODH}$	Output Data Hold (previous word)	4	10		ns
$t_{ODS}$	Output Data Shift (next word)	4		60	ns
$t_{PT}$	Data throughput or "fall through"	3, 6		2.2	μs
$t_{MRORL}$	Master Reset to OR LOW	8		65	ns
$t_{MRIRH}$	Master Reset to IR HIGH	8		65	ns
$t_{IPH}^*$	Input Ready pulse HIGH	3	20		ns
$t_{OPH}^*$	Output Ready pulse HIGH	6	20		ns

† See AC test and high speed application note.

\*  $t_{IPH}$  and  $t_{OPH}$  are measured on initial characterization lots only and are not directly tested in production.

2

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage .....	-1.5 V to 7 V
Off state output voltage .....	-0.5 V to 5.5 V
Storage temperature .....	-65°C to +150°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and a functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## OPERATING CONDITIONS C57401/2

Symbol	Parameter	Figure	Military			Unit
			Min	Typ	Max	
$V_{CC}$	Supply voltage		4.5	5	5.5	V
$T_A^*$	Operating temperature		-55		125	°C
$t_{SIH}^\dagger$	Shift in HIGH time	1	45			ns
$t_{SIL}$	Shift in LOW time	1	45			ns
$t_{DS}$	Input data setup	1	0			ns
$t_{IDH}$	Input data hold time	1	55			ns
$f_{IN}$	Shift in rate	1	7			MHz
$f_{OUT}$	Shift Out rate	4	7			MHz
$t_{SOH}^\dagger$	Shift Out HIGH time	4	45			ns
$t_{SOL}$	Shift Out LOW time	4	45			ns
$t_{MRW}$	Master Reset pulse <sup>†</sup>	8	30			ns
$t_{MRS}^{**}$	Master Reset to SI	8	45			ns

\* Instant-On Case Temperature

\*\*  $t_{MRS}$  is measured on initial characterization lots only and is not directly tested in production.

## SWITCHING CHARACTERISTICS C57401/2 Over Operating Conditions

Symbol	Parameter	Figure	Military			Unit
			Min		Max	
$t_{IRL}^\dagger$	Shift In to Input Ready LOW	1			60	ns
$t_{IRH}^\dagger$	Shift In to Input Ready HIGH	1			60	ns
$t_{ORL}^\dagger$	Shift Out to Output Ready LOW	4			65	ns
$t_{ORH}^\dagger$	Shift Out to Output Ready HIGH	4			70	ns
$t_{ODH}$	Output Data Hold (previous word)	4	10			ns
$t_{ODS}$	Output Data Shift (next word)	4			65	ns
$t_{PT}$	Data throughput or "fall through"	3, 6			4	µs
$t_{MRORL}$	Master Reset to OR LOW	8			65	ns
$t_{MRIRH}$	Master Reset to IR HIGH	8			65	ns
$t_{IPH}^*$	Input Ready pulse HIGH	3	30			ns
$t_{OPH}^*$	Output Ready pulse HIGH	6	30			ns

† See AC test and high speed application note.

\* This parameter applies to FIFOs communicating with each other in a cascaded mode.  $t_{IPH}$  and  $t_{OPH}$  are measured on initial characterization lots only and are not directly tested in production.



## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage .....	-1.5 V to 7 V
Off-state output voltage .....	-0.5 V to 5.5 V
Storage temperature .....	-65°C to +150°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and a functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## OPERATING CONDITIONS C57401A/2A

Symbol	Parameter	Figure	Military			Unit
			Min	Typ	Max	
$V_{CC}$	Supply voltage		4.5	5	5.5	V
$T_A^*$	Operating temperature		-55		125	°C
$t_{SIH}^\dagger$	Shift in HIGH time	1	35			ns
$t_{SIL}$	Shift in LOW time	1	35			ns
$t_{IDS}$	Input data setup	1	0			ns
$t_{IDH}$	Input data hold time	1	45			ns
$f_{IN}$	Shift in rate	1	10			MHz
$f_{OUT}$	Shift Out rate	4	10			MHz
$t_{SOH}^\dagger$	Shift Out HIGH time	4	35			ns
$t_{SOL}$	Shift Out LOW time	4	35			ns
$t_{MRW}$	Master Reset pulse	8	40			ns
$t_{MRS}^{**}$	Master Reset to SI	8	45			ns

\* Instant-On Case Temperature

\*\*  $t_{MRS}$  is measured on initial characterization lots only and is not directly tested in production.

## SWITCHING CHARACTERISTICS C57401A/2A Over Operating Conditions

Symbol	Parameter	Figure	Military			Unit
			Min	Max	Unit	
$t_{IRL}^\dagger$	Shift In to Input Ready LOW	1		50		ns
$t_{IRH}^\dagger$	Shift In to Input Ready HIGH	1		50		ns
$t_{ORL}^\dagger$	Shift Out to Output Ready LOW	4		65		ns
$t_{ORH}^\dagger$	Shift Out to Output Ready HIGH	4		65		ns
$t_{ODH}$	Output Data Hold (previous word)	4	10			ns
$t_{ODS}$	Output Data Shift (next word)	4		60		ns
$t_{PT}$	Data throughput or "fall through"	3, 6		2.2		μs
$t_{MRORL}$	Master Reset to OR LOW	8		65		ns
$t_{MRIRH}$	Master Reset to IR HIGH	8		65		ns
$t_{IPH}^*$	Input Ready pulse HIGH	3	30			ns
$t_{OPH}^*$	Output Ready pulse HIGH	6	30			ns

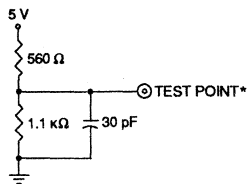
† See AC test and high speed application note.

\* This parameter applies to FIFOs communicating with each other in a cascaded mode.  $t_{IPH}$  and  $t_{OPH}$  are measured on initial characterization lots only and are not directly tested in production.

2

## TEST LOAD FOR ALL DEVICES

Input pulse 0 to 3 V.  
 Input Rise and Fall Time (10%–90%).  
 5 ns minimum.  
 Measurements made at 1.5 V.



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\* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

## DC CHARACTERISTICS Over Operating Conditions For all Devices

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IL}$	Low-level input voltage				0.8 <sup>†</sup>	V
$V_{IH}$	High-level input voltage		2 <sup>†</sup>			V
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$ $I_I = -18 \text{ mA}$			-1.5	V
$I_{IL1}$	Low-level input current	$V_{CC} = \text{MAX}$ $V_I = 0.45 \text{ V}$			-0.8	mA
$I_{IL2}$					-1.6	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$ $V_I = 2.4 \text{ V}$			50	$\mu\text{A}$
$I_I$	Maximum input current	$V_{CC} = \text{MAX}$ $V_I = 5.5 \text{ V}$			1	mA
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ $I_{OL} = 8 \text{ mA}$			0.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ $I_{OH} = -0.9 \text{ mA}$	2.4			V
$I_{OS}$	Output short-circuit current*	$V_{CC} = \text{MAX}$ $V_O = 0 \text{ V}$	-20		-90	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$  Inputs low, outputs open.	57401		160	mA
			57401A		180	
			57402		180	
			57402A		200	
			C57401		160	
			C57401A		180	
			C57402		180	
			C57402A		200	

\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

<sup>†</sup>  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## FUNCTIONAL DESCRIPTION

### Data Input

After power up the Master Reset is pulsed low (Fig 8) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the  $D_x$  inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought low. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a Shift-Out is applied. If the memory is full, IR will remain LOW.

### Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front.  $t_{PT}$  defines the time required for the first data to travel from input to the output of a previously empty device.

### Data Output

Data is read from the  $O_x$  outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage.

When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and  $O_x$  remains as before (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least  $t_{PT}$ ) or completely empty (Output Ready stays LOW for at least  $t_{PT}$ ).

### AC Test and High Speed App. Notes

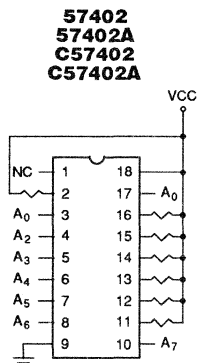
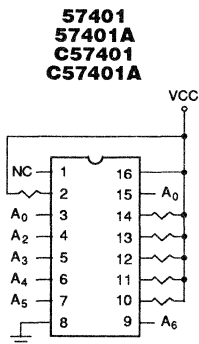
Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1  $\mu$ F directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time ( $t_{DH}$ ) and the next activity of the Input Ready ( $t_{RL}$ ) to be extended relative to Shift In going High. This same type of problem is also related to  $t_{IRH}$ ,  $t_{ORL}$  and  $t_{ORH}$  as related to Shift-Out.

## LIFE TEST/ BURN-IN CIRCUITS

### Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883. Test method 1015, conditions A through E. Test conditions are selected at AMD's option.

### Dynamic Burn-In Circuitry



$T_{ambient} = 125^{\circ}C$

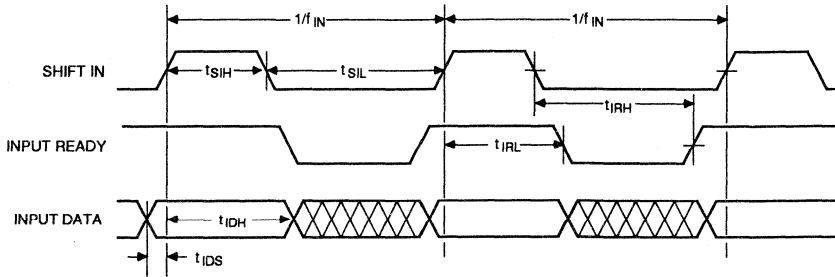
$V_{CC} = 5.25 \pm 0.25 V$

Square wave pulses on  $A_0$  to  $A_8$  are:

1. 50%  $\pm$  15% duty cycle
2. Logic "0" = -1 V to 0.7 V
3. Logic "1" = 2.4 V to  $V_{CC}$
4. Frequency of each address is to be one-half of each preceding input, with  $A_0$  beginning at 100 kHz.

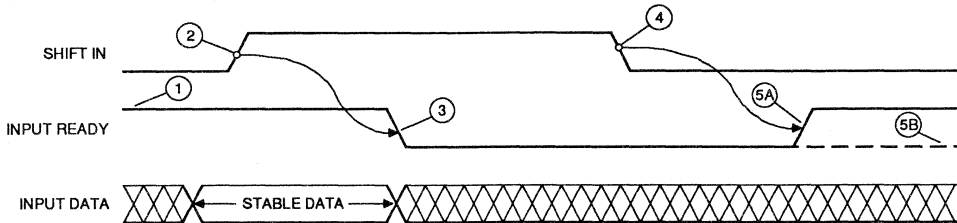
e.g.,  $A_0 = 100 \text{ kHz}$   
 $A_1 = 50 \text{ kHz} \pm 10\%$   
 $A_2 = 25 \text{ kHz} \pm 10\%$   
 $A_n = 1/2 A_{n-1} \pm 10\%$ , etc.

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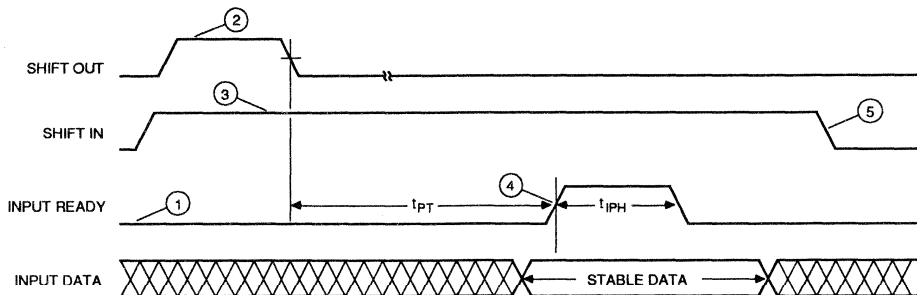
505 136

Figure 1. Input Timing



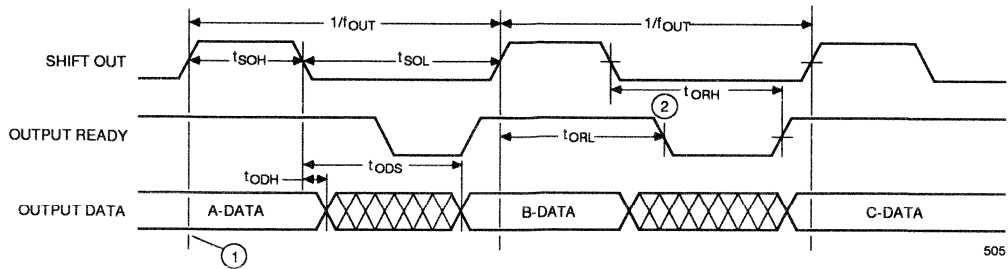
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Figure 2. The Mechanism of Shifting Data into the FIFO



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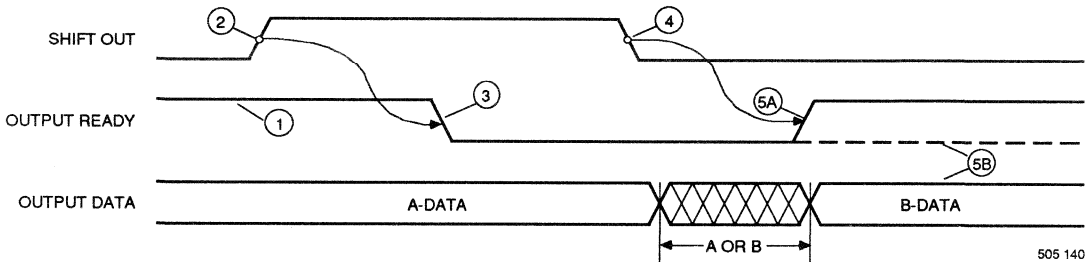
Figure 3. Data Is Shifted in Whenever Shift In and Input Ready Are Both HIGH



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1. The diagram assumes that at this time words 63, 62, 61 are loaded with A, B, C Data, respectively.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

**Figure 4. Output Timing**



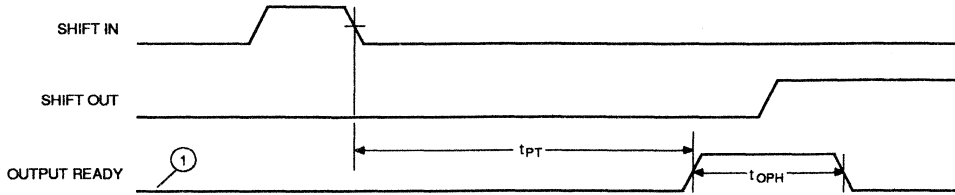
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1. Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
2. Shift-Out goes HIGH causing the next step.
3. Output ready goes LOW.
4. Contents of word 62 (B-DATA) is released for "fall-through" to word 63.
- 5A. Output ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
- 5B. If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

Note: Shift Out pulses applied when Output Ready is LOW will be ignored (Figure 7).

**Figure 5. The Mechanism of Shifting Data Out of the FIFO**

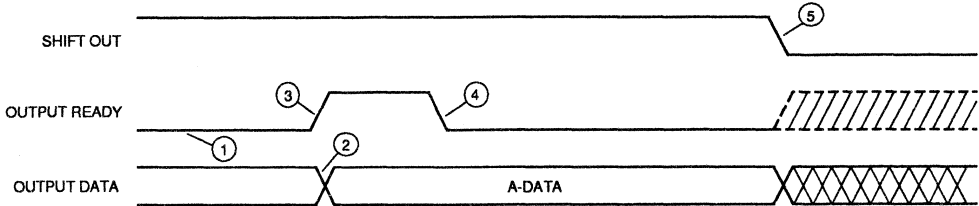
**2**



1. FIFO initially empty.

505 141

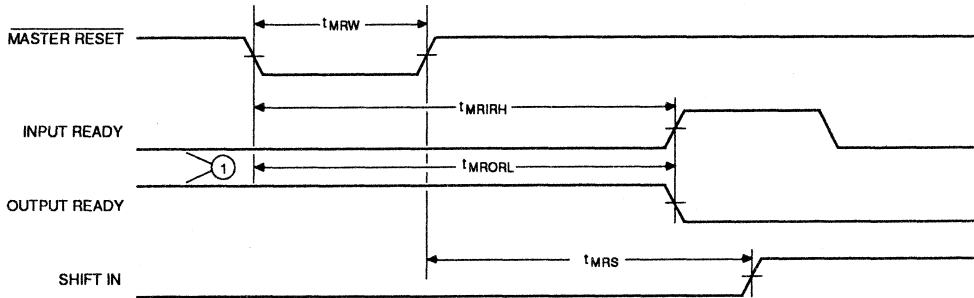
**Figure 6.  $t_{PT}$  and  $t_{OPH}$  Specification**



1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating arrival of new data.
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

505 142

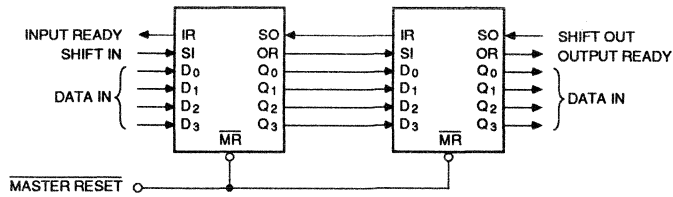
**Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH**



1. FIFO initially full.

505 143

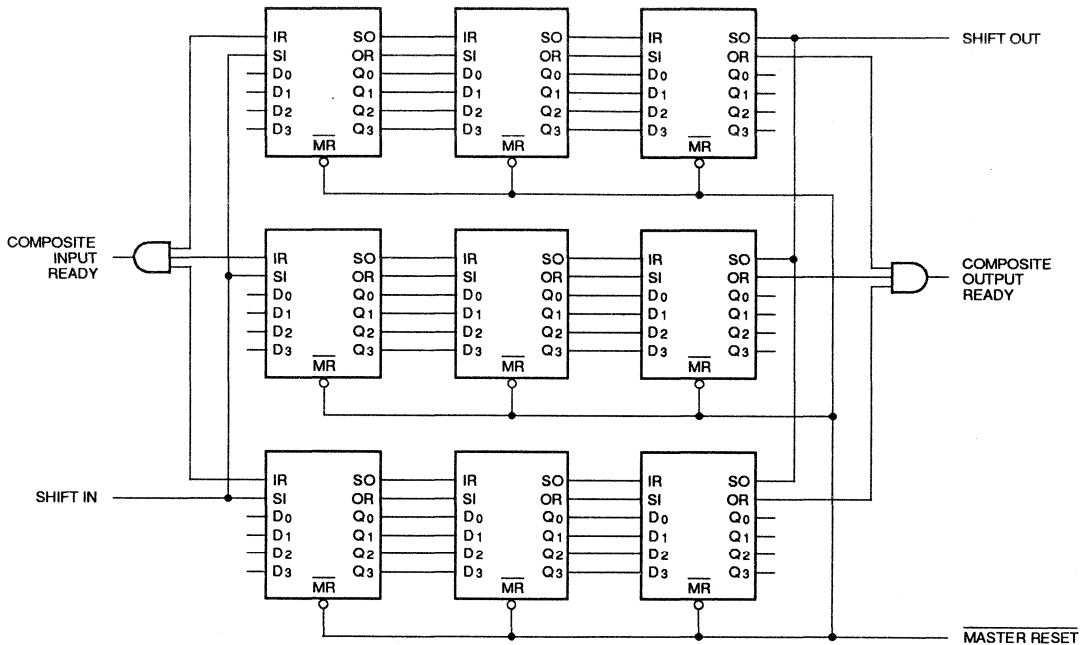
**Figure 8. Master Reset Timing**



505 144

**Figure 9. Cascading FIFOs to Form 128X4 FIFO with C57401/A**

Cascadable FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.



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**Figure 10. 192X12 FIFO with C57401/A**

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Cascadable FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.



# 57413A

## Military First-In First-Out (FIFO) 64x5 Memory 25MHz (Standalone)

Conforms to Mil-Std-883, Class B\*

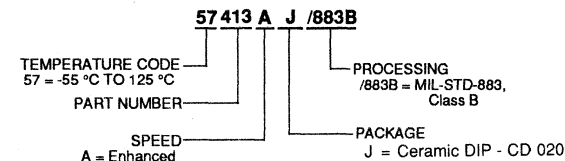
### DISTINCTIVE CHARACTERISTICS

- High-speed 25 MHz shift-in/shift-out rates
- High-drive capability
- Three-state outputs
- Half-Full and Almost-Full/Empty status flags
- Structured pinouts, Output pins directly opposite corresponding Input pins
- Asynchronous operation
- TTL-compatible Inputs and Outputs
- Dose rate (transient upset) junction-isolated bipolar process  $2 \times 10^{10}$  RADs (Si)/s recovery time of 50 to 70  $\mu$ s from 1  $\mu$ s pulse
- Neutron fluence (permanent damage):  $1 \times 10^{13}$  N/cm<sup>2</sup>

### GENERAL DESCRIPTION

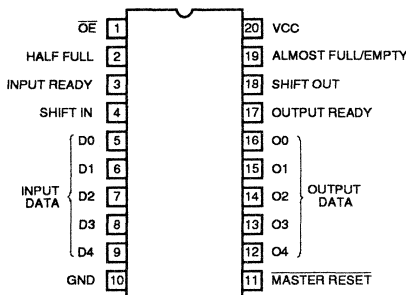
The 57413A is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at a 25 MHz input/output rate. The data is loaded and emptied on first-in/first-out basis. It is a three-state device with high-drive ( $I_{OL} = 12$  mA) data outputs. This device can be connected in parallel to give FIFOs of any word length. It has a Half-Full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of the 57413A are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

### ORDERING INFORMATION



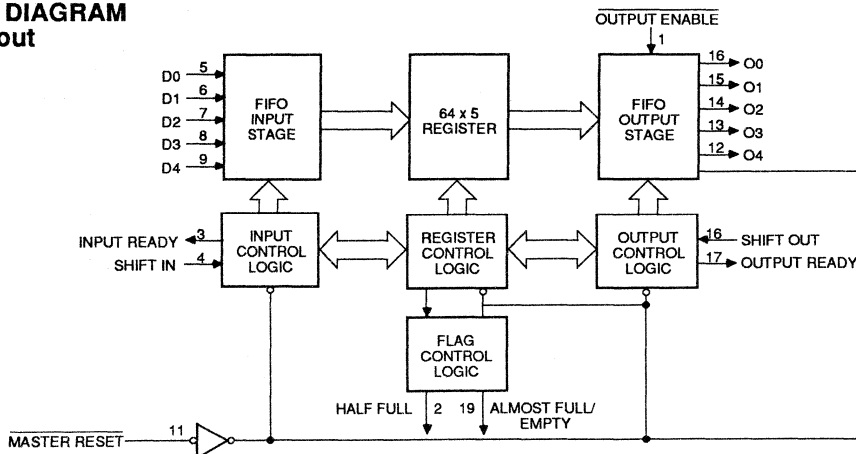
505 146

### PIN CONFIGURATION



505 147

### BLOCK DIAGRAM DIP Pinout



505 148



## Absolute Maximum Ratings\*

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input Voltage range .....	-1.5 V to 7 V
Off-state output voltage .....	-0.5 V to 5.5 V
Storage temperature .....	-65°C to +150°C

\*Note:

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## Operating Conditions

Symbol	Parameter	Figure	Min	Max	Unit
$V_{CC}$	Supply voltage		4.5	5.5	V
$t_{SIH}^{\dagger}$	Shift in HIGH time	1	16		ns
$t_{SIL}^{\dagger}$	Shift in LOW time	1	20		ns
$t_{IDS}$	Input data setup time	1	2		ns
$t_{IDH}$	Input data hold time	1	25		ns
$f_{IN}$	Shift in rate	1	DC	25	MHz
$f_{OUT}$	Shift Out rate	4	DC	25	MHz
$t_{SOH}^{\dagger}$	Shift out HIGH time	4	10		ns
$t_{SOL}$	Shift out LOW time	4	27		ns
$t_{MRW}$	Master Reset pulse	8	35		ns
$t_{MRS}^{**}$	Master Reset to SI	8	35		ns
$V_{IL}^*$	Low level input voltage			0.8	V
$V_{IH}^*$	High level input voltage		2.0		V
$T_A^{***}$	Operating temperature		-55	125	°C

\*  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

\*\*  $t_{MRS}$  is measured on initial characterization lots only and is not directly tested in production.

† See AC test and high speed application note.

\*\*\* Instant-On Case temperature.

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**DC Characteristics** Over Operating Conditions Conforms to MIL-STD-883; Group A, Subgroups 1, 2, & 3.

Symbol	Parameter	Test Conditions		Min	Max	Unit
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$		-1.5	V
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.45 \text{ V}$		-250	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4 \text{ V}$		50	$\mu\text{A}$
$I_I$	Maximum input current	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$		1	mA
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL}$ (Data outputs)	12 mA	0.5	V
			$I_{OL}$ (IR, OR)	8 mA†		
			$I_{OL}$ (Flag outputs)	8 mA		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH}$ (Data outputs)	-3.0 mA	2.4	V
			$I_{OH}$ (IR, OR)	-0.9 mA		
			$I_{OH}$ (Flag outputs)	-0.9 mA		
$I_{OS}^*$	Output short-circuit current	$V_{CC} = \text{MAX}$	$V_O = 0 \text{ V}$	-20	-90	mA
$I_{HZ}$	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 2.4 \text{ V}$		20	$\mu\text{A}$
$I_{LZ}$		$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$		-20	$\mu\text{A}$
$I_{CC}^{**}$	Supply current	$V_{CC} = \text{MAX}$ , inputs low, outputs open			240	mA

\* Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

\*\* See curve for  $I_{CC}$  vs. temp.

† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

**Switching Characteristics** Over Operating Conditions Conforms to MIL-STD-883; Group A, Subgroups 9, 10, 11.

Symbol	Parameter	Figure	Min	Max	Unit
$t_{IRL}^\dagger$	Shift In $\uparrow$ to Input Ready LOW	1		28	ns
$t_{IRH}^\dagger$	Shift In $\downarrow$ to Input Ready HIGH	1		25	ns
$t_{ORL}^\dagger$	Shift Out $\uparrow$ to Output Ready LOW	4		28	ns
$t_{ORH}^\dagger$	Shift Out $\downarrow$ to Output Ready HIGH	4		25	ns
$t_{ODH}^\dagger$	Output Data Hold (previous word)	4	10		ns
$t_{ODS}$	Output Data Shift (next word)	4		40	ns
$t_{PT}$	Data throughput or "fall through"	3, 6		750	ns
$t_{MRORL}$	Master Reset $\downarrow$ to Output Ready LOW	8		30	ns
$t_{MRIRH}$	Master Reset $\uparrow$ to Input Ready HIGH	8		30	ns
$t_{MRIRL}^*$	Master Reset $\downarrow$ Input Ready LOW	8		30	ns
$t_{MRO}$	Master Reset $\downarrow$ to Outputs LOW	8		55	ns

\* If the FIFO is not full (IR High),  $\overline{MR}$  low forces IR low, followed by IR returning high when  $\overline{MR}$  goes high.

† See AC test and high-speed application note.

## Switching Characteristics Over Operating Conditions (Cont.)

Symbol	Parameter	Figure	Min	Max	Unit
$t_{IPH}$	Input ready pulse HIGH	3	5		ns
$t_{OPH}$	Output ready pulse HIGH	6	5		ns
$t_{ORD}$	Output ready $\uparrow$ HIGH to Data Valid	4		20	ns
$t_{AEH}^*$	Shift Out $\uparrow$ AF/E HIGH	9		145	ns
$t_{AEL}^*$	Shift In $\uparrow$ to AF/E LOW	9		650	ns
$t_{AFL}^*$	Shift Out $\uparrow$ to AF/E LOW	10		650	ns
$t_{AFH}^*$	Shift In $\uparrow$ to AF/E HIGH	10		145	ns
$t_{HFH}^*$	Shift In $\uparrow$ to HF HIGH	11		380	ns
$t_{HFL}^*$	Shift Out $\uparrow$ to HF LOW	11		380	ns
$t_{PHZ}^{**}$	Output Disable Delay	A		30	ns
$t_{PLZ}^{**}$		A		30	ns
$t_{PZL}$	Output Enable Delay	A		30	ns
$t_{PZH}$		A		50	ns

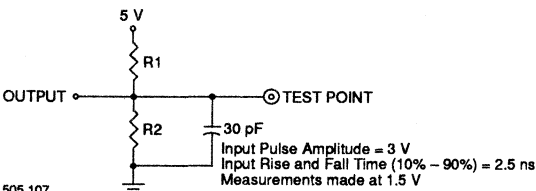
Note: Input rise and fall time (10%–90%) = 2.5 ns.

\* See timing diagram for explanation of parameters.

\*\* Actual test limits may be different to compensate for ATE.

Conforms to MIL-STD-883; Group A, Subgroups 9, 10, & 11.

### Standard Test Load

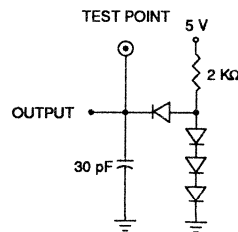


505 107

$I_{OL}$	R1	R2
12 mA	390 $\Omega$	760 $\Omega$
8 mA	600 $\Omega$	1200 $\Omega$

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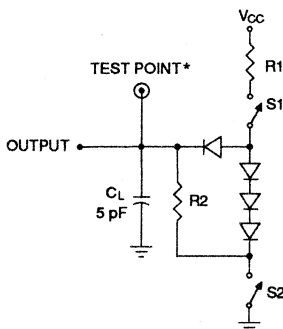
### Design Test Load



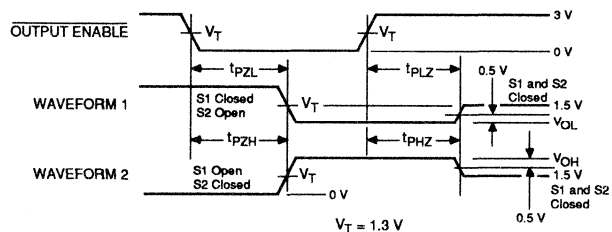
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### Three State Test Load\*



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Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

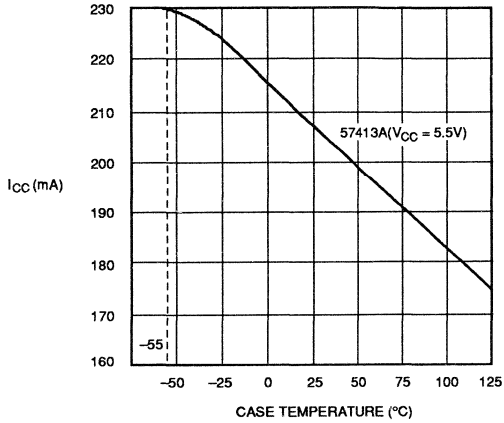
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

505 150

\* Equivalent test loads may be used for automatic testing

Figure A. Enable and Disable

## Typical $I_{CC}$ vs Temperature ( $V_{CC} = \text{MAX}$ )



505 151

## Military Case Outlines

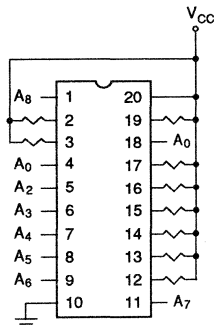
PACKAGE OUTLINE LETTER	CONFORMS TO MIL-M-38510F APPENDIX C CASE
J	D-8

505025B

## Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

### Dynamic Burn-In Circuitry



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$T_{\text{ambient}} = 125^{\circ}\text{C}$

$V_{CC} = 5.25 \pm 0.25 \text{ V}$

Square wave pulses on  $A_0$  to  $A_8$  are:

1.  $50\% \pm 15\%$  duty cycle
2. Logic "0" =  $-1 \text{ V to } 0.7 \text{ V}$
3. Logic "1" =  $2.4 \text{ V to } V_{CC}$
4. Frequency of each address is to be one-half of each preceding input, with  $A_0$  beginning at 100 kHz.

e.g.,  $A_0 = 100 \text{ kHz}$

$A_1 = 50 \text{ kHz} \pm 10\%$

$A_2 = 25 \text{ kHz} \pm 10\%$

$A_n = 1/2 A_{n-1} \pm 10\%$

## FUNCTIONAL DESCRIPTION

### Data Input

After power up the Master Reset is pulsed low (Figure 8) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from  $D_x$  inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will “bubble” to the front when data is shifted out),  $t_{pT}$  defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

### Data Output

Data is read from the  $O_x$  outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least  $t_{pT}$ ) or completely empty (Output Ready stays LOW for at least  $t_{pT}$ ).

## AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1  $\mu$ F directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not high due to (a) too high a frequency, or (b) FIFO being full or effected by the Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the “effective” timing of Input Data Hold time ( $T_{IDH}$ ) and the next activity of Input Ready ( $T_{IRL}$ ) to be extended relative to Shift-In going HIGH. This same type of problem is also related to  $T_{IRH}$ ,  $T_{DRL}$ , and  $T_{ORH}$  as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

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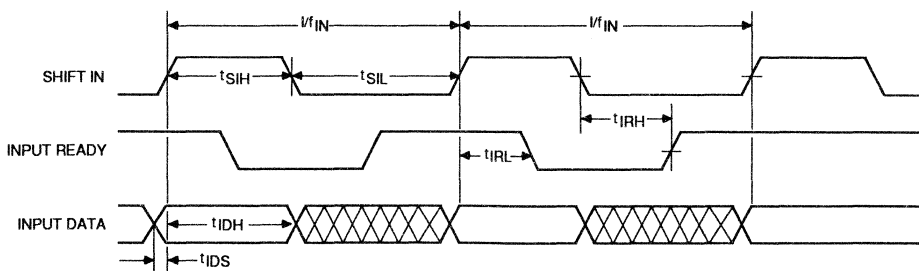
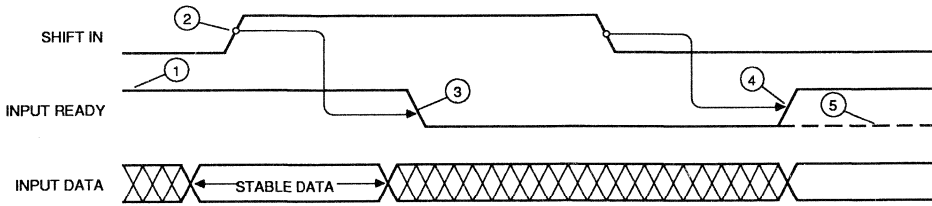


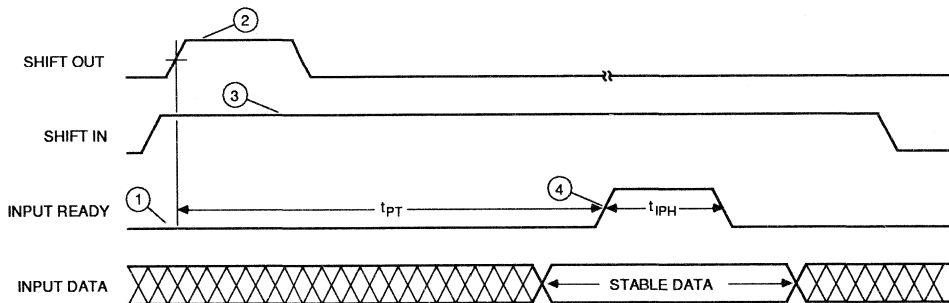
Figure 1. Input Timing



- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
  - ② Input Data is loaded into the first word. The Data from the first word is released for "fall through" to second word.
  - ③ Input Ready goes LOW indicating the first word is full.
  - ④ Shift-In going LOW allows input Ready to sense the status of the first word. The first word is now empty as indicated by input Ready HIGH.
  - ⑤ If the second word is already full then the data remains at the first word. Since the FIFO is now full input Ready remains low.
- Note: Shift-In pulses applied while input Ready is LOW will be ignored (See Figure 4).

**Figure 2. The Mechanism of Shifting Data Into the FIFO**

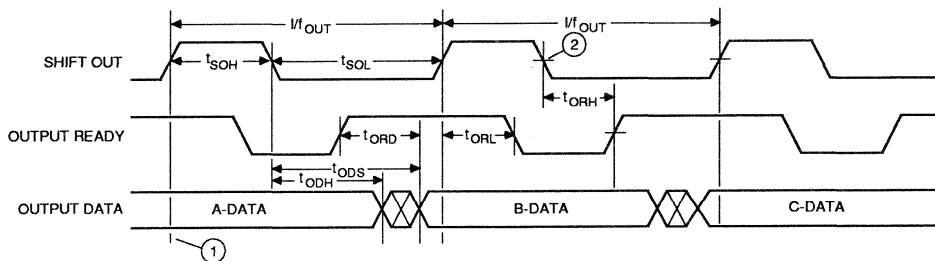
505 173



- ① FIFO is initially full.
- ② Shift-Out pulse is applied. An empty location starts "bubbling" to the front.
- ③ Shift-In is held HIGH.
- ④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

**Figure 3. Data Is Shifted in Whenever Shift In and Input Ready Are Both HIGH**

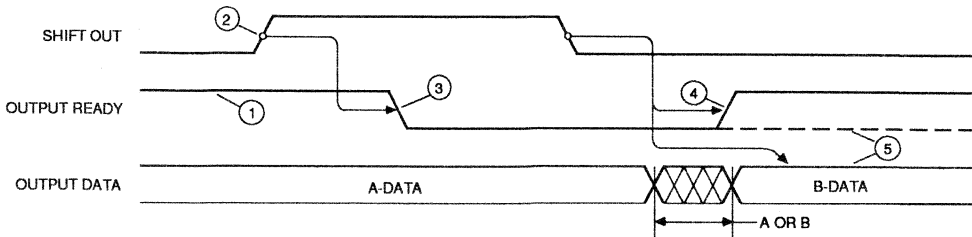
505 155



- ① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- ② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO or both high together.

**Figure 4. Output Timing**

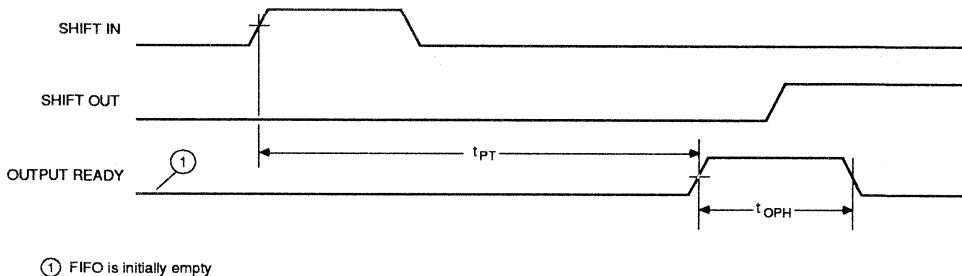
505 156



- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ② Shift-Out goes HIGH causing the contents of word 62 (B-DATA) to be released for fall through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
- ③ Output Ready goes LOW.
- ④ Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- ⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data become invalid.  
Note: Shift-Out pulses applied when Output Ready is LOW will be ignored (See Figure 7).

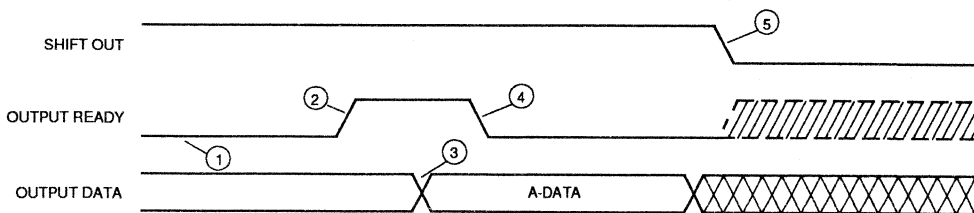
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**Figure 5. The Mechanism of Shifting Data Into the FIFO**



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**Figure 6.  $t_{PT}$  and  $t_{OPH}$  Specification**



- ① Word 63 is empty.
- ② Output Ready goes HIGH indicating arrival of the new data.
- ③ New data (A) arrives at the outputs (word 63).
- ④ Since Shift-Out is held HIGH, Output Data is subject to change. Output Ready will go HIGH or LOW.
- ⑤ As soon as Shift-Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or Low depending on whether there are any additional upstream words in the FIFO.

505 159

**Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH**

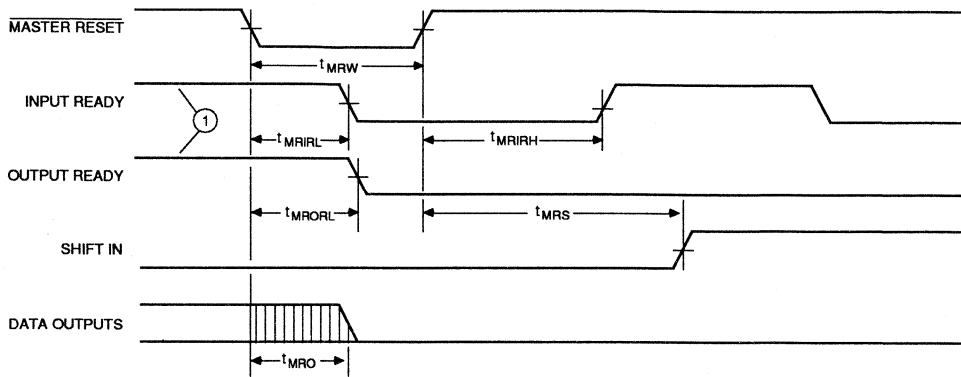
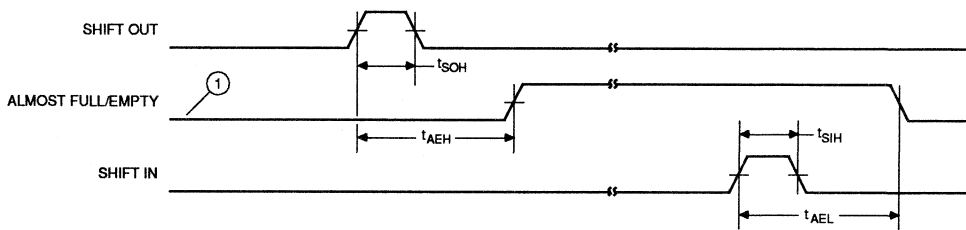


Figure 8. Master Reset Timing

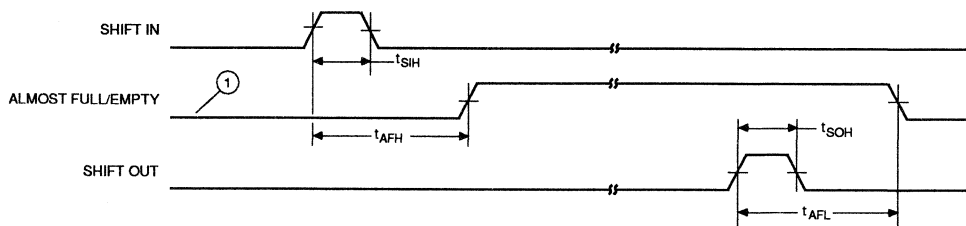
505 160



① FIFO contains 9 words (one more than almost empty).

Figure 9.  $t_{AEH}$ ,  $t_{AEL}$  Specifications

505 161

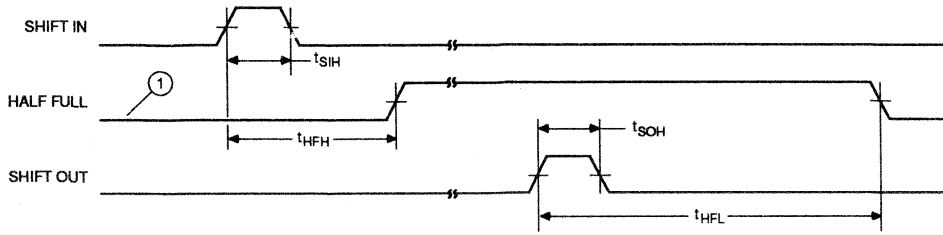


① FIFO contains 55 words (one short of almost full).

Figure 10.  $t_{AFH}$ ,  $t_{AFL}$  Specifications

505 162

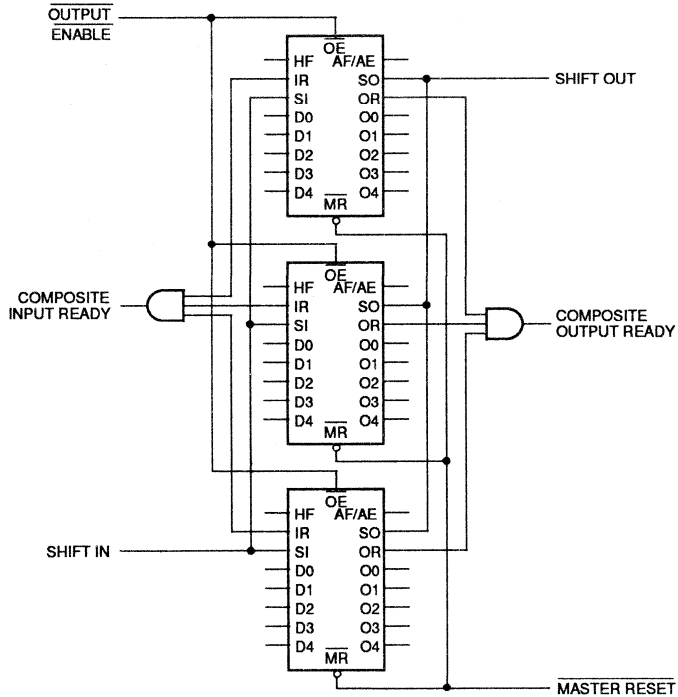




① FIFO contains 31 words (one short of half full).

505 163

Figure 11.  $t_{HFL}$ ,  $t_{HFH}$  Specifications



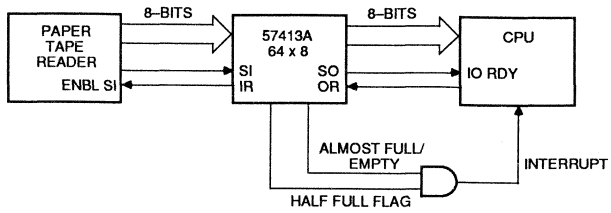
505 164

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite input and Output and Output Ready Flags. This requirement is due to the different fall through times of the FIFOs.

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Figure 12. 64 x 15 FIFO with 57413A

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Note: Expanding the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 12.

**Figure 13. Application for the 57413A "Slow and Steady Rate to Flat 'Blocked Rate'"**

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# 57C401/13 57C402/23 57C4033

Military CMOS Zero Power FIFOs  
 64x4 64x5 Memory 12 MHz (Cascadable)  
 Conforms to MIL-STD-883, Class B (Latest Revision)



Advanced  
 Micro  
 Devices

## DISTINCTIVE CHARACTERISTICS

- Zero standby power
- High-speed 12 MHz shift-in/shift-out data rates
- Very low active power consumption
- Choice of 4-bit or 5-bit data width
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- RAM-based architecture for short fall-through delay
- Full CMOS 8-transistor cell for maximum noise immunity
- Asynchronous operation
- Output Enable feature (57C4013/23/33)

## GENERAL DESCRIPTION

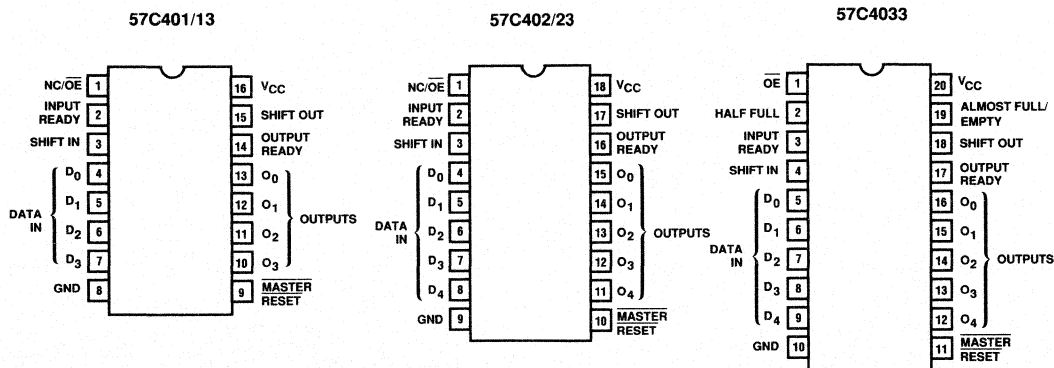
The 57C40X/XX series devices are high-performance CMOS RAM-based First-In First-Out buffer memory products organized as 64 words by 4 or 5 bits wide. These devices use Advanced Micro Devices' CMOS process technology and meet the demands for high-reliability, high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, improving overall system performance. Separate on-chip

Read and Write pointers address each memory location, allowing the data to propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well in high-speed disk controllers, graphics, and communication systems. The 550  $\mu$ watt standby power of these devices makes them ideal for ultra-low-powered and battery-powered systems.

2

## CONNECTION DIAGRAMS

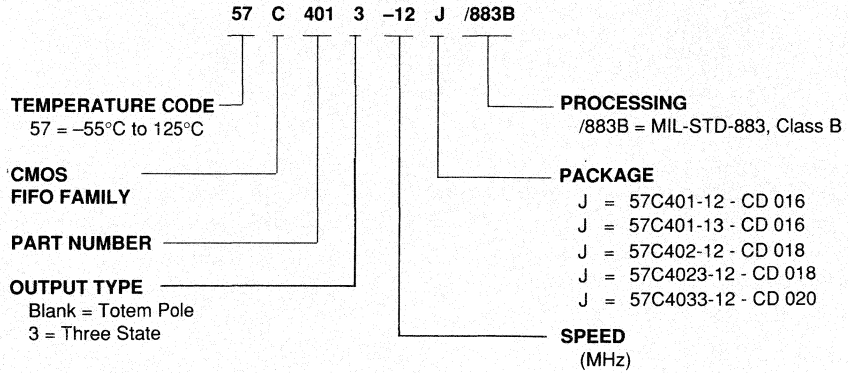
### For Ceramic DIP Packages



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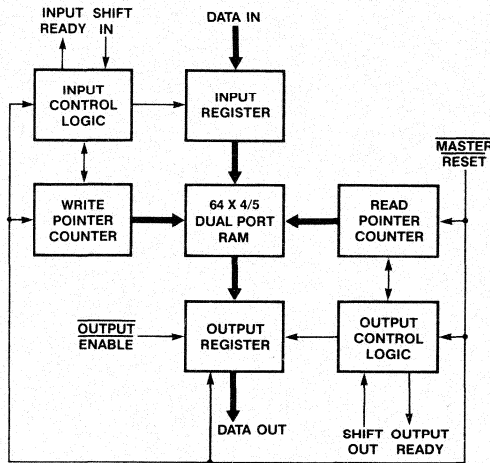
Figure 1.

# ORDERING INFORMATION

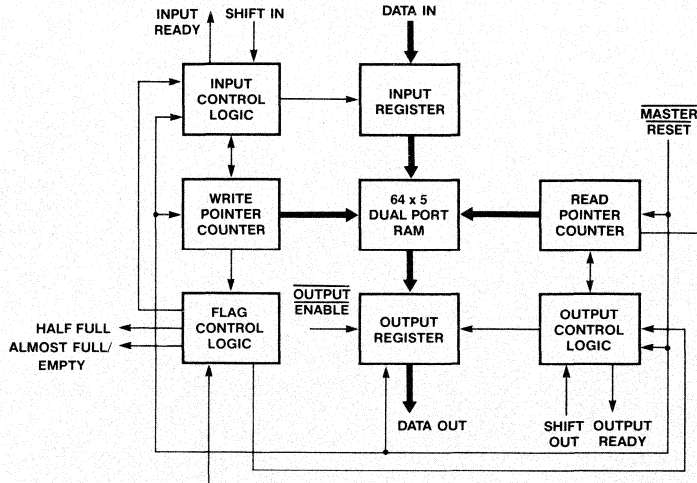


# BLOCK DIAGRAMS

57C401/13 57C402/23



57C4033



## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to +7.0 V
Input voltage range .....	-1.5 V to +7.0 V
Off-state output voltage .....	-0.5 V to +6.0 V
Storage temperature .....	-65°C to +150°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## OPERATING CONDITIONS

Symbol	Parameter	Figure	Min	Max	Unit
$V_{CC}$	Supply Voltage		4.5	5.5	V
$t_{SIH}$	Shift-In HIGH Time	1	16		ns
$t_{SIL}$	Shift-In LOW Time	1	25		ns
$t_{IDS}$	Input Data Setup to SI (Shift In)	1	0		ns
$t_{IDH}$	Input Data Hold Time to SI (Shift In)	1	40		ns
$t_{RIDS}$	Input Data Setup to IR (Input Ready)	3	0		ns
$t_{RIDH}$	Input Data Hold Time to IR (Input Ready)	3	30		ns
$f_{IN}$	Shift-In Rate	1	12		MHz
$f_{OUT}$	Shift-Out Rate	4	12		MHz
$t_{SOH}$	Shift-Out HIGH Time	4	27		ns
$t_{SOL}$	Shift-Out LOW Time	4	25		ns
$t_{MRW}^{**}$	Master Reset Pulse	8	45		ns
$t_{MRS}^{***}$	Master Reset to SI	8	75		ns
$V_{IL}^*$	Low Level Input Voltage			0.8	V
$V_{IH}^*$	High Level Input Voltage		2.0		V
$T_A^\dagger$	Operating Temperature		-55	125	°C

\*  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

\*\* If the FIFO is not full (IR HIGH)  $\overline{MR}$  LOW forces IR LOW, followed by IR returning high when  $\overline{MR}$  goes high.

\*\*\*  $t_{MRS}$  is measured on initial characterization lots only and is not directly tested in production.

† Instant-On Case Temperature.

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Conforms to MIL-STD-883; Group A, Subgroups 1, 2, and 3.

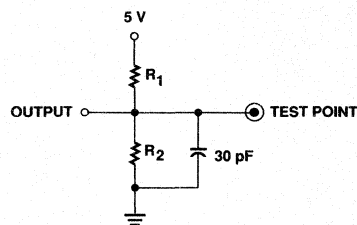
## DC CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Test Conditions		Min	Max	Unit
$I_{IN}$	Input Current	$V_{CC} = \text{MAX}$	$0 V < V_{IN} < 5.5 V$	-1	1	$\mu\text{A}$
$V_{OL}$	Low-Level Output Voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 20 \mu\text{A}$		0.1	V
			$I_{OL} = 8 \text{ mA}$		0.4	
$V_{OH}$	High-Level Output Voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -20 \mu\text{A}$	$V_{CC} - 0.1$		V
			$I_{OH} = -4 \text{ mA}$	2.4		
$I_{OZ}$	Off-State Output Current ('4013, '4023, '4033 devices)	$V_{CC} = \text{MAX}$	$0 V \leq V_{OUT} \leq 5.5 V$	-5	5	$\mu\text{A}$
$I_{OS}^*$	Output Short-Circuit Current	$V_{CC} = \text{MAX}$	$V_O = 0 V$	-20	-90	mA
$I_{CCop}^{**}$	Maximum Operating Current	$V_{CC} = \text{MAX}$ , All outputs open, $f = 12 \text{ MHz}$			40	mA
$I_{CCstby}$	Maximum Standby Current ('CZ' devices only)	$V_{CC} = \text{MAX}$ , All outputs open.			100	$\mu\text{A}$

\* No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

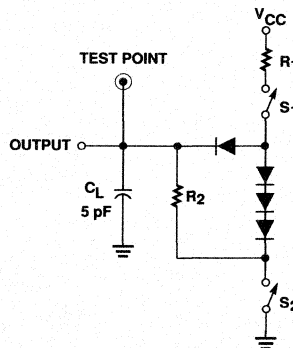
\*\* Tested on initial qualification lot only .

### STANDARD TEST LOAD\*



Input Pulse Amplitude = 3 V  
 Input Rise and Fall Time (10% – 90%) = 2.5 ns  
 Measurement made at 1.5 V

### THREE STATE TEST LOAD\*



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\*Equivalent test load may be used for automatic testing.

### RESISTOR VALUES

$I_{OL}$	$R_1$	$R_2$
8 mA	600 $\Omega$	1200 $\Omega$

Conforms to MIL-STD-883; Group A, Subgroups 9, 10, and 11.

## SWITCHING CHARACTERISTICS

Symbol	Parameter	Figure	Min	Max	Unit
$t_{IRL} \dagger$	Shift In $\uparrow$ to Input Ready LOW	1		70	ns
$t_{IRH} \dagger$	Shift In $\downarrow$ to Input Ready HIGH	1		65	ns
$t_{ORL} \dagger$	Shift Out $\uparrow$ to Output Ready LOW	4		65	ns
$t_{ORH} \dagger$	Shift Out $\downarrow$ to Output Ready HIGH	4		60	ns
$t_{ODH} \dagger$	Output Data Hold (previous word)	4	5		ns
$t_{ODS}$	Output Data Shift (next word)	4		40	ns
$t_{PT}$	Data Throughput	3,6		110	ns
$t_{MRORL}$	Master Reset $\downarrow$ to Output Ready LOW	8		120	ns
$t_{MRIRH}^*$	Master Reset $\uparrow$ to Input Ready HIGH	8		120	ns
$t_{MRO}$	Master Reset $\downarrow$ to Outputs LOW	8		45	ns
$t_{MRHFL}$	Master Reset $\downarrow$ to Half-Full Flag LOW ('4033 only)	9		120	ns
$t_{MRAEH}$	Master Reset $\downarrow$ to Almost Empty Flag HIGH ('4033 only)	9		120	ns
$t_{IPH}$	Input Ready Pulse HIGH	3	12		ns
$t_{OPH}$	Output Ready Pulse HIGH	6	10		ns
$t_{ORD}$	Output Ready $\uparrow$ to Data Valid	4		0	ns
$t_{AEH}$	Shift Out $\uparrow$ to AF/E High ('4033 only)	10		125	ns
$t_{AEL}$	Shift In $\uparrow$ to AF/E LOW ('4033 only)	10		125	ns
$t_{AFL}$	Shift Out $\uparrow$ to AF/E LOW ('4033 only)	11		125	ns
$t_{AFH}$	Shift In $\uparrow$ to AF/E HIGH ('4033 only)	11		125	ns
$t_{HFH}$	Shift In $\uparrow$ to HF HIGH ('4033 only)	12		125	ns
$t_{HFL}$	Shift Out $\uparrow$ to HF LOW ('4033 only)	12		125	ns
$t_{PHZ}^{**}$	Output Disable Delay ('4013, '4023, '4033 devices only)	A		30	ns
$t_{PLZ}^{**}$				30	
$t_{PZL}$	Output Enable Delay ('4013, '4023, '4033 devices only)	A		35	ns
$t_{PZH}$				35	

\* If the FIFO is not full (IR HIGH), MR LOW forces IR LOW, followed by IR returning high when MR goes high.

\*\* Actual test limits may be different to compensate for ATE.

† See timing diagram for explanation of parameters

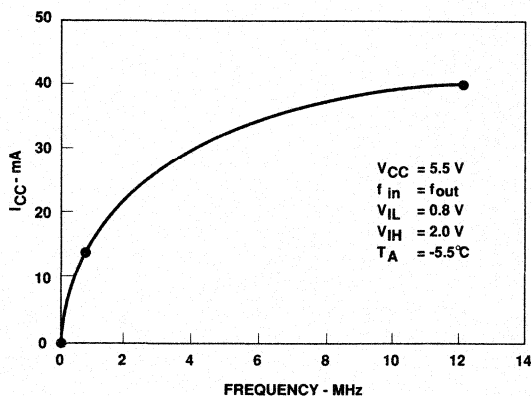
## CAPACITANCES\*

Symbol	Parameter	Test Condition	Min	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ $V_{CC} = 4.5\text{ V}$		10	pF
$C_{OUT}$	Output Capacitance			7	pF

\* These parameters are not tested in production but are evaluated at initial characterization and anytime the design is modified where capacitance may be affected.

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## I<sub>CC</sub> vs. FREQUENCY



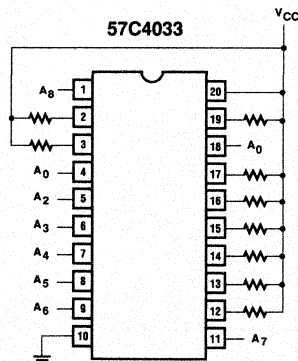
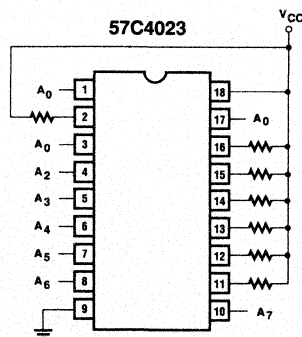
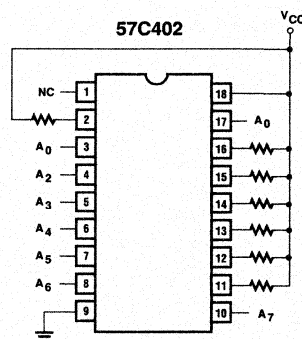
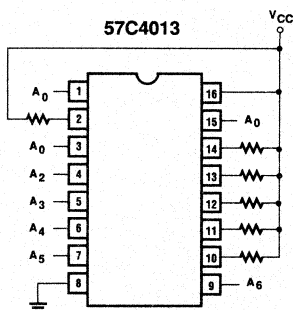
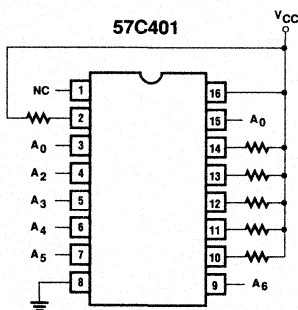
## MILITARY CASE OUTLINES

Device	Package	
	J (Cerdip)	
	Package Outline	Conforms to MIL-M-38510 Appendix C Case
57C401	16J	D-2
57C4013	16J	D-2
57C402	18J	D-6
57C4023	18J	D-6
57C4033	20J	D-8

## MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## DYNAMIC BURN-IN CIRCUITRY



$T_{\text{ambient}} = 125^\circ\text{C}$

$V_{CC} = 5.25 \pm 0.25 \text{ V}$

Square wave pulses on  $A_0$  to  $A_8$  are:

1.  $50\% \pm 15\%$  duty cycle
2. Logic "0" =  $-1 \text{ V}$  to  $0.7 \text{ V}$
3. Logic "1" =  $2.4 \text{ V}$  to  $V_{CC}$
4. Frequency of each address is to be one-half of each preceding input, with  $A_0$  beginning at 100 kHz.

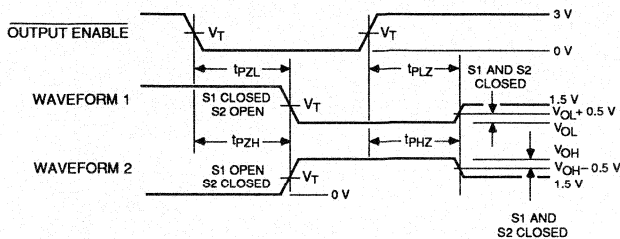
e.g.,  $A_0 = 100 \text{ kHz}$

$A_1 = 50 \text{ kHz} \pm 10\%$

$A_2 = 25 \text{ kHz} \pm 10\%$

$A_n = 1/2 A_{n-1} \pm 10\%$ , etc.





Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure A. Enable and Disable (57C4013/23/33 Only)

## FUNCTIONAL DESCRIPTION

### Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the  $D_x$  inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then IR will remain LOW.

### Data Output

Data is read from the  $O_x$  outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW and  $O_x$  remains as before, (i.e., data does not change if the FIFO is empty). A dual port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-outs).

### AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1  $\mu$ F directly between  $V_{CC}$  and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time ( $t_{IDH}$ ) and the next activity of Input Ready ( $t_{IRL}$ ) to be extended relative to Shift-In going HIGH. This same type of situation occurs with  $t_{IRH}$ ,  $t_{ORL}$ ,  $t_{ORH}$ , and the Status Flag timing as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.

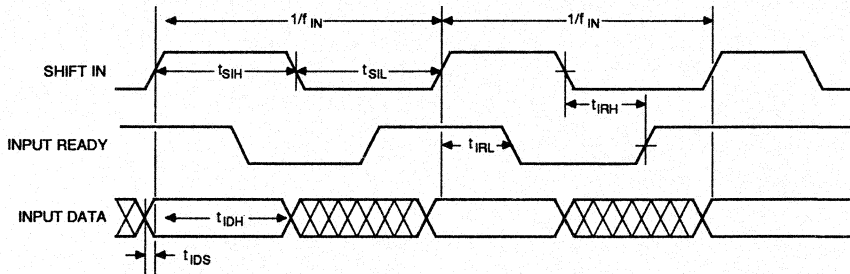
## HF AND AF/AE STATUS FLAGS (57C4033 Only)

The Half-Full (HF) will be high only when the net balance of words shifted into the FIFO exceeds the number of words shifted out by thirty-two or more (i.e., when the FIFO contains thirty-two or more words). The Almost-Full/Empty (AF/AE) flag will be HIGH when the FIFO contains fifty-six or more words or when the FIFO contains eight or fewer words (see Figures 10, 11 and 12).

Care should be exercised in using the status flags because they are capable of producing arbitrarily short pulses. For example, if

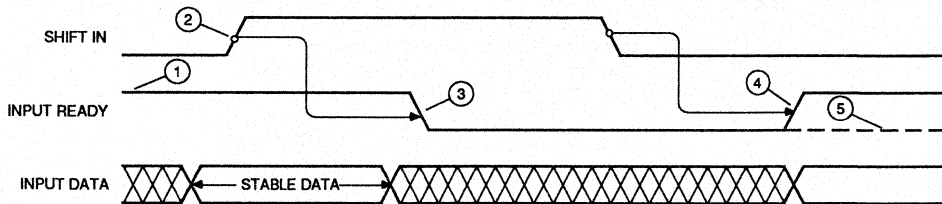
the FIFO contains thirty-one words, and SI and SO pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of SI and SO.

The flags will always settle to the correct state after the appropriate delay (e.g.,  $t_{HFL}$ ,  $t_{HFH}$  in this example). This property of the status flags will clearly be a function of dynamic relation between SI and SO. Generally, the use of level-sensitive, rather than edge-sensitive status detection circuits will alleviate this hazard.



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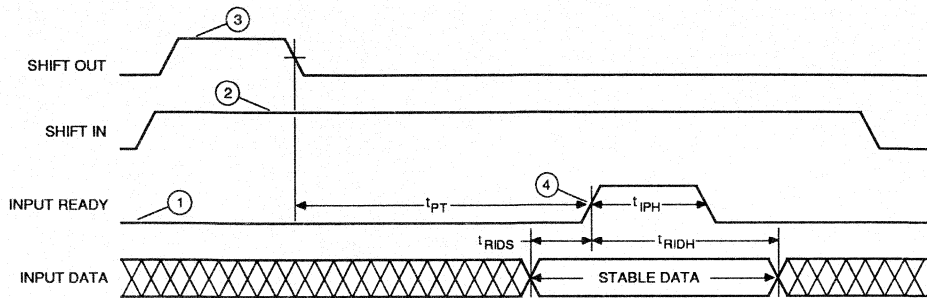
Figure 1. Input Timing



- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- ② Input Data is loaded into the first available memory location.
- ③ Input Ready goes LOW indicating this memory location is full.
- ④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
- ⑤ If the FIFO is already full, then the Input Ready remains low.

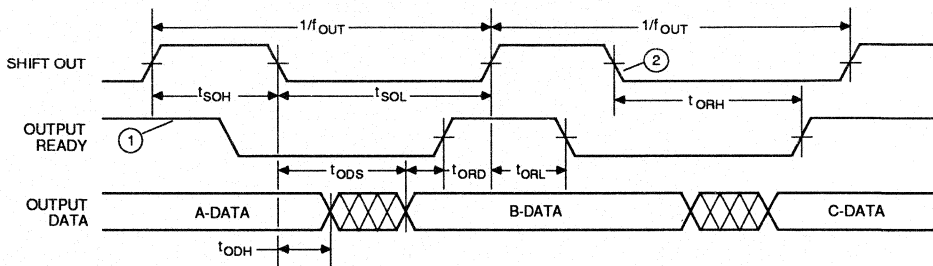
Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

Figure 2. The Mechanism of Shifting Data Into the FIFO



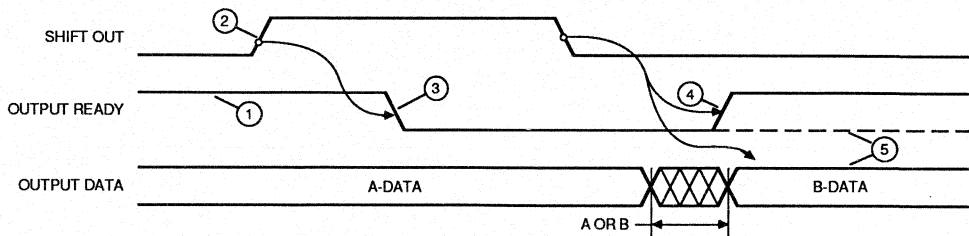
- ① FIFO is initially full.
- ② Shift In is held HIGH.
- ③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
- ④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

**Figure 3. Data Is Shifted In Whenever Shift In and Input Ready Are Both HIGH**



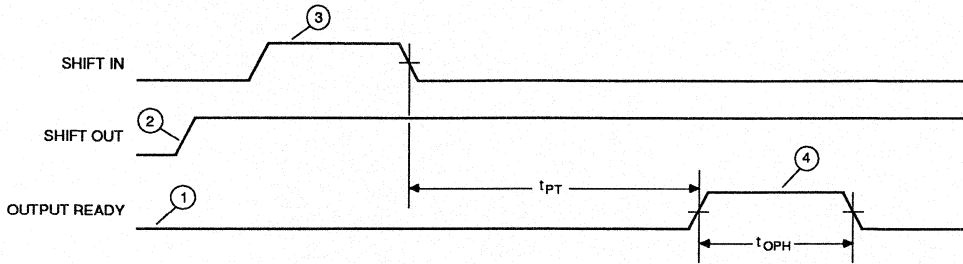
- ① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
- ② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

**Figure 4. Output Timing**



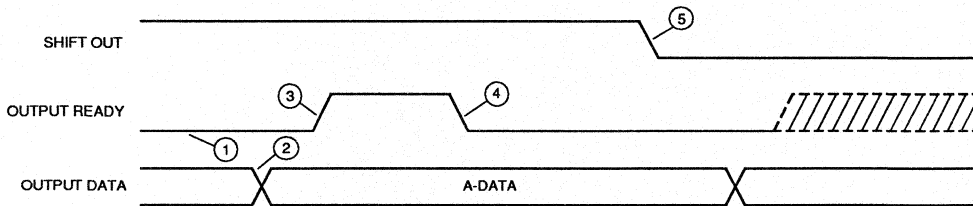
- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ② Shift-Out goes HIGH causing (B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
- ③ Output Ready goes LOW.
- ④ Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- ⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

**Figure 5. The Mechanism of Shifting Data Out of the FIFO**



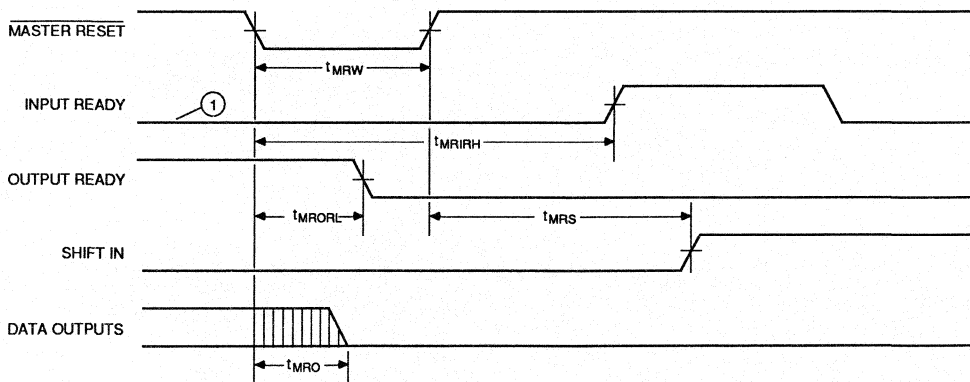
- ① FIFO is initially empty.
- ② Shift Out is held HIGH.
- ③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
- ④ As soon as Output Ready becomes HIGH, the word is shifted out.

**Figure 6.  $t_{PT}$  and  $t_{OPH}$  Specification**

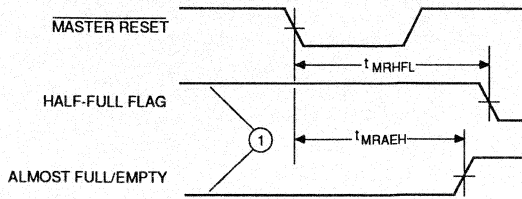


- ① The internal logic does not detect the presence of any data in the FIFO.
- ② New data (A) arrives at the outputs.
- ③ Output Ready goes HIGH indicating arrival of the new data.
- ④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- ⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

**Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH**

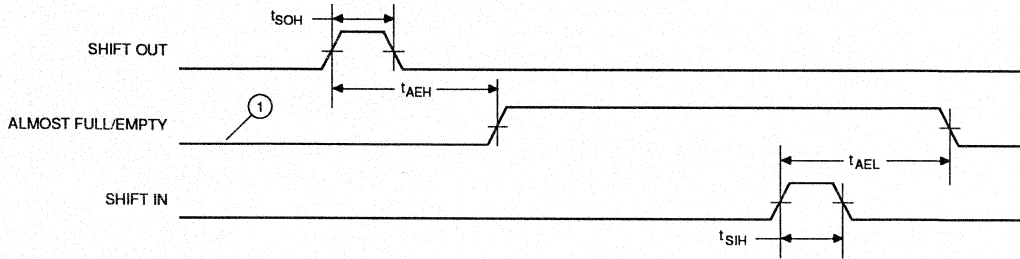


**Figure 8. Master Reset Timing**



① FIFO initially has between 32 and 56 words.

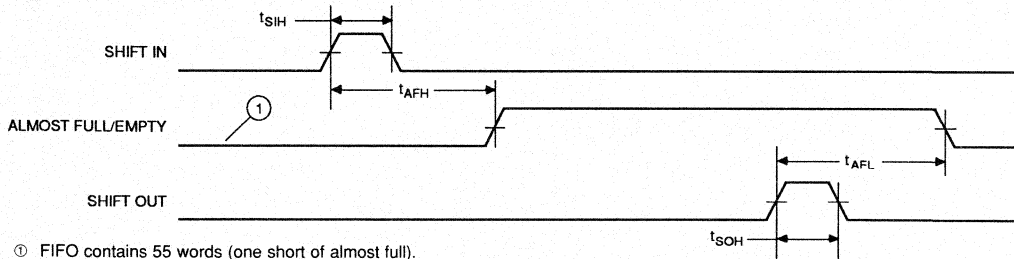
**Figure 9.  $t_{MRHFH}$  and  $t_{MRAEH}$  Specifications**



① FIFO contains 9 words (one more than almost empty).

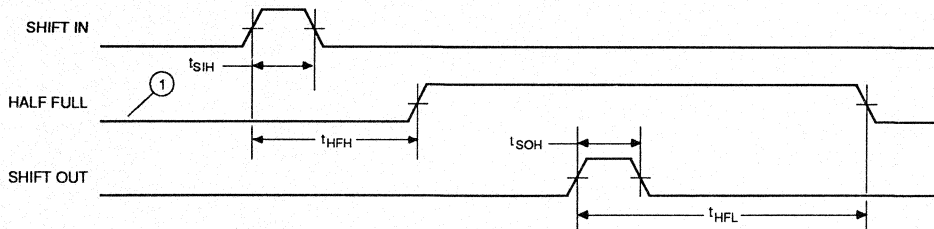
**Figure 10.  $t_{AEH}$  and  $t_{AEL}$  Specifications**

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① FIFO contains 55 words (one short of almost full).

**Figure 11.  $t_{AFH}$  and  $t_{AFL}$  Specifications**

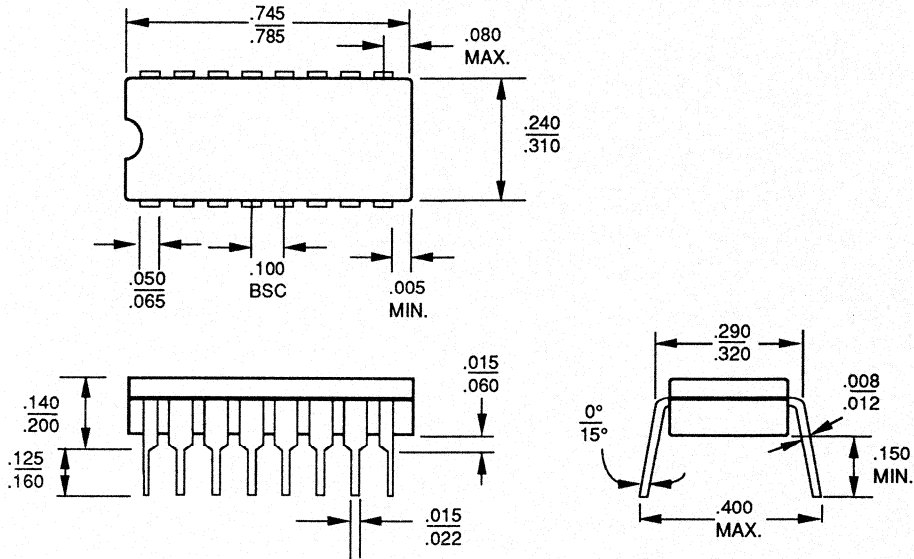


① FIFO contains 31 words (one short of almost full).

**Figure 12.  $t_{HFL}$  and  $t_{HFH}$  Specifications**

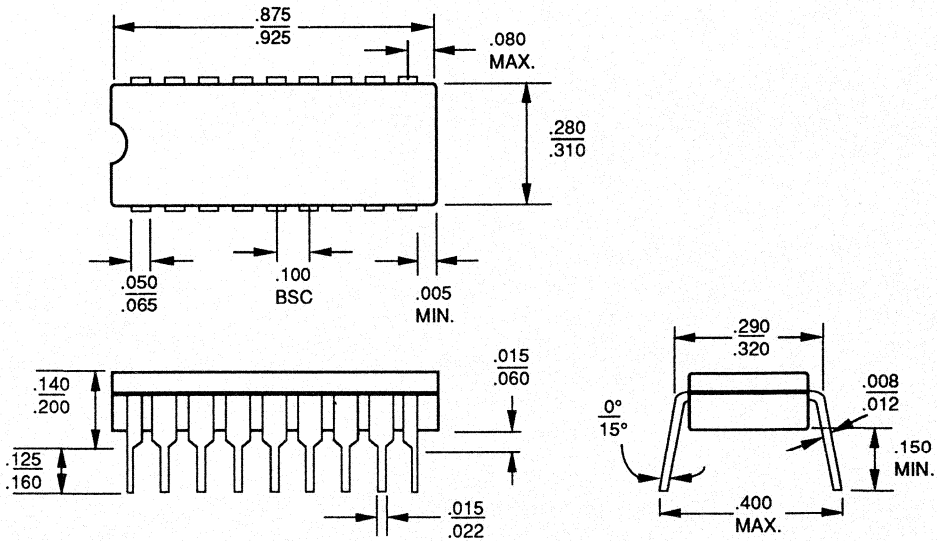
**PHYSICAL DIMENSIONS\***

**CD 016**



PID# 07319B

**CD 018**



07803C

\* For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.

# Am7200-40/50/65/80

High Density First-in First-out (FIFO) 256x9 CMOS Memory

## DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 256x9 organization
- Cycle times of 50/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption
  - 90 mA max, -50/65/80
  - 100 mA max, -40
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for  $\overline{XI}$  - CMOS threshold
- Functional and pin compatible with industry standard devices

## GENERAL DESCRIPTION

The Am7200 is a RAM-based CMOS FIFO that is 256 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 20 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7200 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7200 useful in communication, image processing, mass storage, DSP, and printing systems.

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## BLOCK DIAGRAM

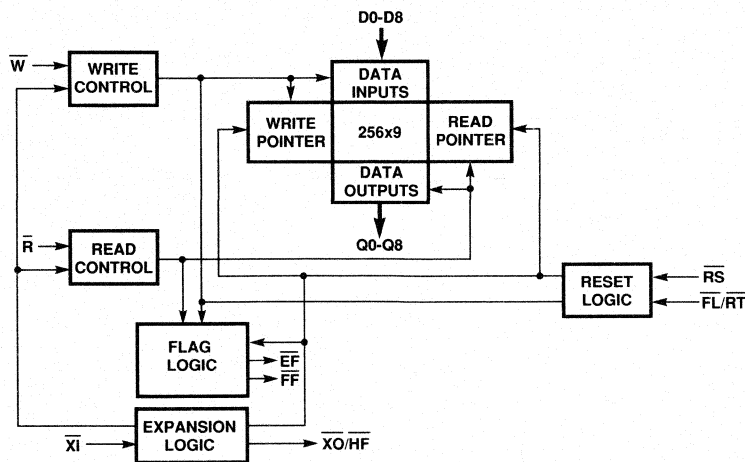
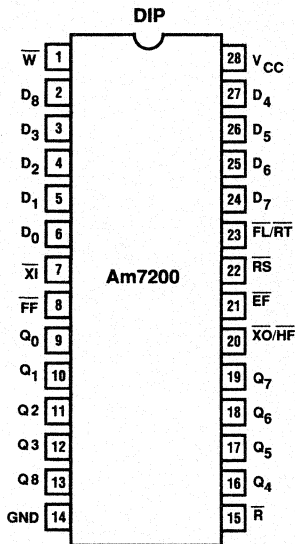


Figure 1.

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication #	Rev.	Amendment
10907	B	/0
Issue Date: February 1989		

## CONNECTION DIAGRAMS



**Pin Designations:**

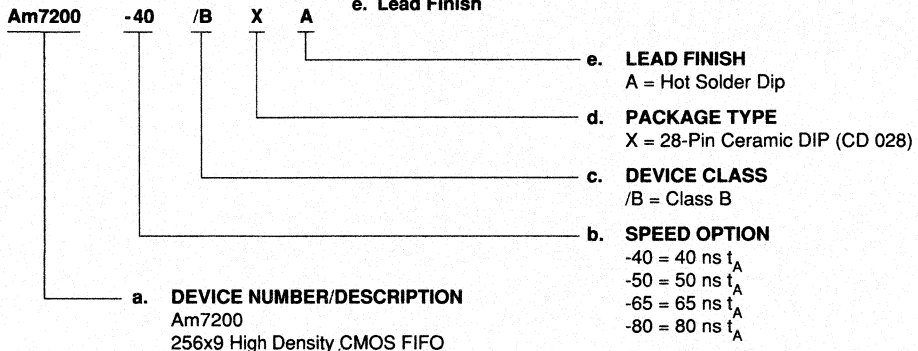
- $\overline{W}$  = Write
- $\overline{R}$  = Read
- RS = Reset
- FL/RT = First Load/Retransmit
- $D_x$  = Data In
- $Q_x$  = Data Out
- $\overline{XI}$  = Expansion In
- $\overline{XO}/\overline{HF}$  = Expansion Out/Half-Full Flag
- FF = Full Flag
- EF = Empty Flag
- $V_{CC}$  = Supply Voltage
- GND = Ground

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
Am7200-40	/BXA
Am7200-50	
Am7200-65	
Am7200-80	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.



## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to + 7.0 V
Input voltage .....	-0.5 V to $V_{CC} + 0.5$ V
Operating temperature .....	-55°C to +125°C
Storage temperature .....	-65°C to + 150°C
Power dissipation .....	2.0 W
DC output current .....	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## DC CHARACTERISTICS Military: $V_{CC} = 5 V \pm 10\%$ , $T_A^\dagger = -55^\circ\text{C to } +125^\circ\text{C}$

Parameter Symbol	Parameter Description	Am7200-40 $t_A = 40$ ns		Am7200-50 $t_A = 50$ ns		Am7200-65 $t_A = 65$ ns		Am7200-80 $t_A = 80$ ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$I_{IL}$	Input Leakage Current (any input) (Note 1)	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$I_{IO}$	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$V_{IH}$	Input High Voltage (all inputs except $\overline{XI}$ ) (Note 3)	2.2	—	2.2	—	2.2	—	2.2	—	V
$V_{IL}$	Input Low Voltage (all inputs except $\overline{XI}$ ) (Note 3)	—	0.8	—	0.8	—	0.8	—	0.8	V
$V_{IH\overline{XI}}$	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	—	3.5	—	3.5	—	3.5	—	V
$V_{IL\overline{XI}}$	Input Low Voltage, $\overline{XI}$ (Note 3)	—	1.5	—	1.5	—	1.5	—	1.5	V
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2$ mA	2.4	—	2.4	—	2.4	—	2.4	—	V
$V_{OL}$	Output Logic "0" voltage $I_{OL} = 8$ mA	—	0.4	—	0.4	—	0.4	—	0.4	V
$I_{CC1}$	Average $V_{CC}$ Power Supply Current (Note 4)	—	100	—	90	—	90	—	90	mA
$I_{CC2}$	Average Standby Current ( $\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$ ) (Note 4)	—	25	—	25	—	25	—	25	mA
$I_{CC3}$	Power Down Current (all inputs = $V_{CC} - 0.2$ V) (Note 4)	—	5	—	5	—	5	—	5	mA

- Notes: 1. Measurements with  $GND \leq V_{IN} \leq V_{CC}$ .  
 2.  $\overline{R} \geq V_{IH}$ ,  $GND \leq V_{OUT} \leq V_{CC}$ .  
 3.  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 4.  $I_{CC}$  measurements are made with outputs open.  
 † Instant-On Case Temperature.

**AC CHARACTERISTICS**  $V_{CC} = 5 V \pm 10\%$ ,  $T_A^\dagger = -55^\circ C$  to  $+125^\circ C$ 

Parameter Symbol	Parameter Description	Am7200-40		Am7200-50		Am7200-65		Am7200-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write and Flag Timing</b>										
$t_{WC}$	Write Cycle Time	50		65		80		100		ns
$t_{WPW}$	Write Pulse Width	40		50		65		80		ns
$t_{WR}$	Write Recovery Time	10		15		15		20		ns
$t_{DS}$	Data Setup Time	20		30		30		40		ns
$t_{DH}$	Data Hold Time	0		5		10		10		ns
$t_{WFF}$	Write LOW to Full Flag LOW		35		45		60		60	ns
$t_{WHF}$	Write LOW to Half-Full Flag LOW		50		65		80		100	ns
$t_{WEF}$	Write HIGH to Empty Flag HIGH		35		45		60		60	ns
$t_{WLZ}$	Write pulse HIGH to data bus at LOW Z (Note 1)	10		15		15		15		ns
<b>Read and Flag Timing</b>										
$t_{RC}$	Read Cycle Time	50		65		80		100		ns
$t_A$	Access Time		40		50		65		80	ns
$t_{RR}$	Read Recovery Time	10		15		15		20		ns
$t_{RPW}$	Read Pulse Width	40		50		65		80		ns
$t_{RLZ}$	Read pulse LOW to data bus at LOW Z (Note 1)	5		10		10		10		ns
$t_{DV}$	Data Valid from read pulse HIGH	5		5		5		5		ns
$t_{RHZ}$	Read pulse HIGH to data bus at HIGH Z (Note 1)		25		30		30		30	ns
$t_{RFF}$	Read HIGH to Full Flag HIGH		35		45		60		60	ns
$t_{RHF}$	Read HIGH to Half-Full-Flag HIGH		50		65		80		100	ns
$t_{REF}$	Read LOW to Empty Flag LOW		30		45		60		60	ns
<b>Reset Timing</b>										
$t_{RSC}$	Reset Cycle Time	50		65		80		100		ns
$t_{RS}$	Reset Pulse Width	40		50		65		80		ns
$t_{RSS}$	Reset Setup Time	40		50		65		80		ns
$t_{RSR}$	Reset Recovery Time	10		15		15		20		ns
$t_{EFL}$	Reset to Empty Flag LOW		50		65		80		100	ns
$t_{HFH}$	Reset to Half-Full Flag High		50		65		80		100	ns
$t_{FFH}$	Reset to Full Flag HIGH		50		65		80		100	ns
<b>Retransmit Timing</b>										
$t_{RTC}$	Retransmit Cycle Time	50		65		80		100		ns
$t_{RT}$	Retransmit Pulse Width	40		50		65		80		ns
$t_{RTR}$	Retransmit Recovery Time	10		15		15		20		ns

Notes: 1. Characterized parameters.

† Instant-On Case Temperature.

# Am7201-40/50/65/80

High Density First-in First-out (FIFO) 512x9 CMOS Memory

## DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 512x9 organization
- Cycle times of 50/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption
  - 90 mA max, -50/65/80
  - 100 mA max, -40
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for XI - CMOS threshold
- Functional and pin compatible with industry standard devices

## GENERAL DESCRIPTION

The Am7201 is a RAM-based CMOS FIFO that is 512 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 20 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7201 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7201 useful in communication, image processing, mass storage, DSP, and printing systems.

2

## BLOCK DIAGRAM

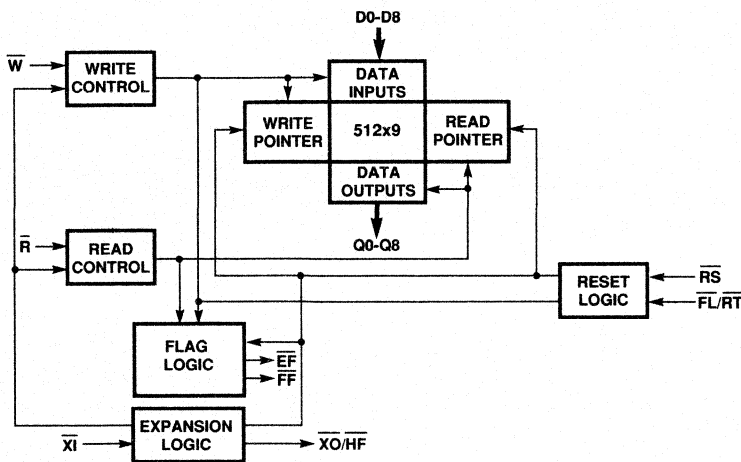
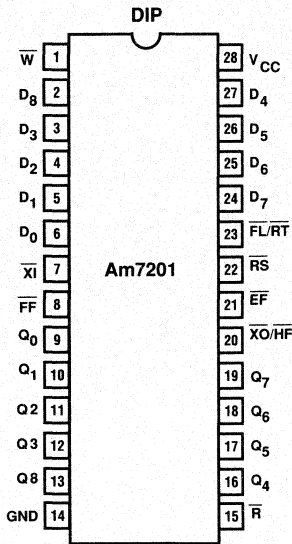


Figure 1.

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication #	Rev.	Amendment
10908	B	/0
Issue Date: February 1989		

## CONNECTION DIAGRAMS



**Pin Designations:**

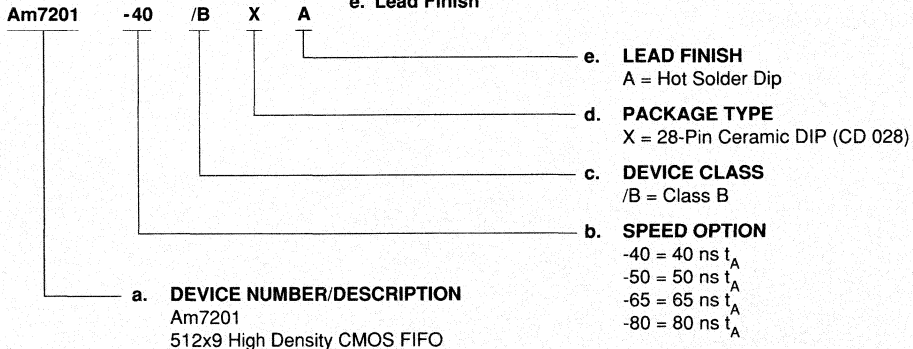
- $\overline{W}$  = Write
- $\overline{R}$  = Read
- $\overline{RS}$  = Reset
- FL/RT = First Load/Retransmit
- $D_x$  = Data In
- $Q_x$  = Data Out
- XI = Expansion In
- XO/HF = Expansion Out/Half-Full Flag
- FF = Full Flag
- EF = Empty Flag
- $V_{CC}$  = Supply Voltage
- GND = Ground

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
Am7201-40	/BXA
Am7201-50	
Am7201-65	
Am7201-80	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to + 7.0 V
Input voltage .....	-0.5 V to $V_{CC} + 0.5$ V
Operating temperature .....	-55°C to +125°C
Storage temperature .....	-65°C to + 150°C
Power dissipation .....	2.0 W
DC output current .....	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## DC CHARACTERISTICS Military: $V_{CC} = 5 \text{ V} \pm 10\%$ , $T_A^\dagger = -55^\circ\text{C to } +125^\circ\text{C}$

Parameter Symbol	Parameter Description	Am7201-40 $t_A = 40 \text{ ns}$		Am7201-50 $t_A = 50 \text{ ns}$		Am7201-65 $t_A = 65 \text{ ns}$		Am7201-80 $t_A = 80 \text{ ns}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$I_{IL}$	Input Leakage Current (any input) (Note 1)	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$I_{IO}$	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$V_{IH}$	Input High Voltage (all inputs except $\bar{X}$ ) (Note 3)	2.2	-	2.2	-	2.2	-	2.2	-	V
$V_{IL}$	Input Low Voltage (all inputs except $X$ ) (Note 3)	-	0.8	-	0.8	-	0.8	-	0.8	V
$V_{IH(X)}$	Input High Voltage, $\bar{X}$ (Note 3)	3.5	-	3.5	-	3.5	-	3.5	-	V
$V_{IL(X)}$	Input Low Voltage, $X$ (Note 3)	-	1.5	-	1.5	-	1.5	-	1.5	V
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2 \text{ mA}$	2.4	-	2.4	-	2.4	-	2.4	-	V
$V_{OL}$	Output Logic "0" voltage $I_{OL} = 8 \text{ mA}$	-	0.4	-	0.4	-	0.4	-	0.4	V
$I_{CC1}$	Average $V_{CC}$ Power Supply Current (Note 4)	-	100	-	90	-	90	-	90	mA
$I_{CC2}$	Average Standby Current ( $R = W = RS = FL/RT = V_{IH}$ ) (Note 4)	-	25	-	25	-	25	-	25	mA
$I_{CC3}$	Power Down Current (all inputs = $V_{CC} - 0.2 \text{ V}$ ) (Note 4)	-	5	-	5	-	5	-	5	mA

- Notes:
- Measurements with  $GND \leq V_{IN} \leq V_{CC}$ .
  - $R \geq V_{IH}$ ,  $GND \leq V_{OUT} \leq V_{CC}$ .
  - $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
  - $I_{CC}$  measurements are made with outputs open.
- † Instant-On Case Temperature.

**AC CHARACTERISTICS**  $V_{CC} = 5 V \pm 10\%$ ,  $T_A \dagger = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ 

Parameter Symbol	Parameter Description	Am7201-40		Am7201-50		Am7201-65		Am7201-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write and Flag Timing</b>										
$t_{WC}$	Write Cycle Time	50		65		80		100		ns
$t_{WPW}$	Write Pulse Width	40		50		65		80		ns
$t_{WR}$	Write Recovery Time	10		15		15		20		ns
$t_{DS}$	Data Setup Time	20		30		30		40		ns
$t_{DH}$	Data Hold Time	0		5		10		10		ns
$t_{WFF}$	Write LOW to Full Flag LOW		35		45		60		60	ns
$t_{WHF}$	Write LOW to Half-Full Flag LOW		50		65		80		100	ns
$t_{WEF}$	Write HIGH to Empty Flag HIGH		35		45		60		60	ns
$t_{WLZ}$	Write pulse HIGH to data bus at LOW Z (Note 1)	10		15		15		15		ns
<b>Read and Flag Timing</b>										
$t_{RC}$	Read Cycle Time	50		65		80		100		ns
$t_A$	Access Time		40		50		65		80	ns
$t_{RR}$	Read Recovery Time	10		15		15		20		ns
$t_{RPW}$	Read Pulse Width	40		50		65		80		ns
$t_{RLZ}$	Read pulse LOW to data bus at LOW Z (Note 1)	5		10		10		10		ns
$t_{DV}$	Data Valid from read pulse HIGH	5		5		5		5		ns
$t_{RHZ}$	Read pulse HIGH to data bus at HIGH Z (Note 1)		25		30		30		30	ns
$t_{RFF}$	Read HIGH to Full Flag HIGH		35		45		60		60	ns
$t_{RHF}$	Read HIGH to Half-Full-Flag HIGH		50		65		80		100	ns
$t_{REF}$	Read LOW to Empty Flag LOW		30		45		60		60	ns
<b>Reset Timing</b>										
$t_{RSC}$	Reset Cycle Time	50		65		80		100		ns
$t_{RS}$	Reset Pulse Width	40		50		65		80		ns
$t_{RSS}$	Reset Setup Time	40		50		65		80		ns
$t_{RSR}$	Reset Recovery Time	10		15		15		20		ns
$t_{EFL}$	Reset to Empty Flag LOW		50		65		80		100	ns
$t_{HFH}$	Reset to Half-Full Flag High		50		65		80		100	ns
$t_{FFH}$	Reset to Full Flag HIGH		50		65		80		100	ns
<b>Retransmit Timing</b>										
$t_{RTC}$	Retransmit Cycle Time	50		65		80		100		ns
$t_{RT}$	Retransmit Pulse Width	40		50		65		80		ns
$t_{RTR}$	Retransmit Recovery Time	10		15		15		20		ns

Notes: 1. Characterized parameters.

† Instant-On Case Temperature.

# Am7202-40/50/65/80

High Density First-in First-out (FIFO) 1024x9 CMOS Memory

## DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 1024x9 organization
- Cycle times of 50/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption
  - 90 mA max, -50/65/80
  - 100 mA max, -40
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for  $\bar{X}1$  - CMOS threshold
- Functional and pin compatible with industry standard devices

## GENERAL DESCRIPTION

The Am7202 is a RAM-based CMOS FIFO that is 1024 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 20 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7202 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7202 useful in communication, image processing, mass storage, DSP, and printing systems.

2

## BLOCK DIAGRAM

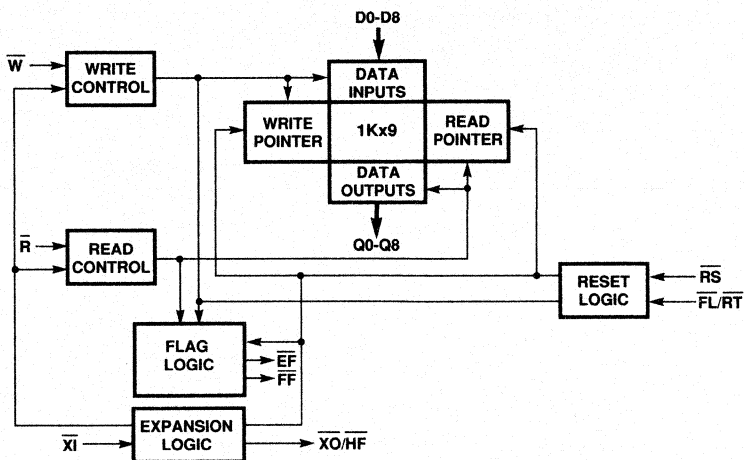
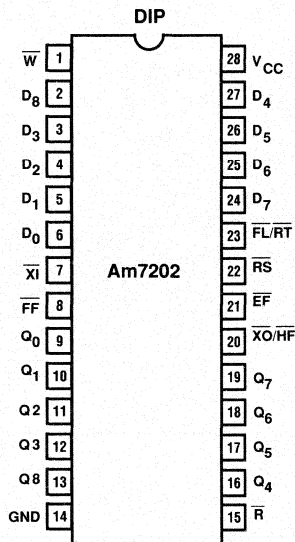


Figure 1.

## CONNECTION DIAGRAMS



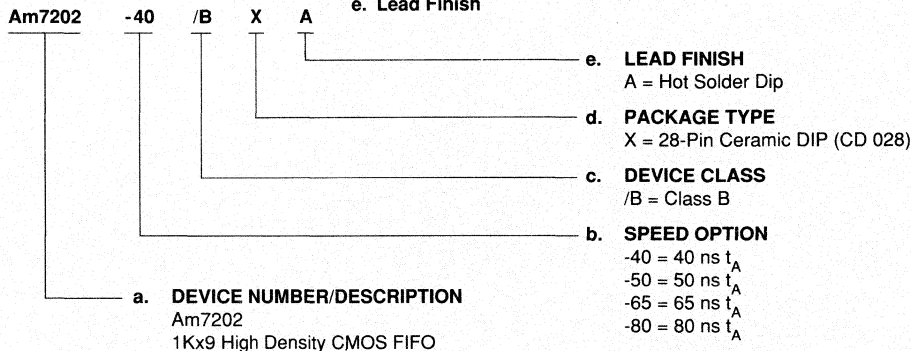
- Pin Designations:**
- $\bar{W}$  = Write
  - $\bar{R}$  = Read
  - $\bar{RS}$  = Reset
  - $\bar{FL}/\bar{RT}$  = First Load/Retransmit
  - $D_x$  = Data In
  - $Q_x$  = Data Out
  - $\bar{X}I$  = Expansion In
  - $\bar{X}O/\bar{H}F$  = Expansion Out/Half-Full Flag
  - $\bar{F}F$  = Full Flag
  - $\bar{E}F$  = Empty Flag
  - $V_{CC}$  = Supply Voltage
  - $GND$  = Ground

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
Am7202-40	/BXA
Am7202-50	
Am7202-65	
Am7202-80	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.



## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to + 7.0 V
Input voltage .....	-0.5 V to $V_{CC} + 0.5$ V
Operating temperature .....	-55°C to +125°C
Storage temperature .....	-65°C to + 150°C
Power dissipation .....	2.0 W
DC output current .....	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## DC CHARACTERISTICS Military: $V_{CC} = 5 \text{ V} \pm 10\%$ , $T_A^\dagger = -55^\circ\text{C to } + 125^\circ\text{C}$

Parameter Symbol	Parameter Description	Am7202-40 $t_A = 40 \text{ ns}$		Am7202-50 $t_A = 50 \text{ ns}$		Am7202-65 $t_A = 65 \text{ ns}$		Am7202-80 $t_A = 80 \text{ ns}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$I_{IL}$	Input Leakage Current (any input) (Note 1)	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$I_{IO}$	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$V_{IH}$	Input High Voltage (all inputs except $\overline{XI}$ ) (Note 3)	2.2	-	2.2	-	2.2	-	2.2	-	V
$V_{IL}$	Input Low Voltage (all inputs except $\overline{XI}$ ) (Note 3)	-	0.8	-	0.8	-	0.8	-	0.8	V
$V_{IH\overline{XI}}$	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	-	3.5	-	3.5	-	3.5	-	V
$V_{IL\overline{XI}}$	Input Low Voltage, $\overline{XI}$ (Note 3)	-	1.5	-	1.5	-	1.5	-	1.5	V
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2 \text{ mA}$	2.4	-	2.4	-	2.4	-	2.4	-	V
$V_{OL}$	Output Logic "0" voltage $I_{OL} = 8 \text{ mA}$	-	0.4	-	0.4	-	0.4	-	0.4	V
$I_{CC1}$	Average $V_{CC}$ Power Supply Current (Note 4)	-	100	-	90	-	90	-	90	mA
$I_{CC2}$	Average Standby Current ( $\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$ ) (Note 4)	-	25	-	25	-	25	-	25	mA
$I_{CC3}$	Power Down Current (all inputs = $V_{CC} - 0.2 \text{ V}$ ) (Note 4)	-	5	-	5	-	5	-	5	mA

- Notes:
1. Measurements with  $\text{GND} \leq V_{IN} \leq V_{CC}$ .
  2.  $\overline{R} \geq V_{IH}$ ,  $\text{GND} \leq V_{OUT} \leq V_{CC}$ .
  3.  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
  4.  $I_{CC}$  measurements are made with outputs open.
- † Instant-On Case Temperature.

**AC CHARACTERISTICS**  $V_{CC} = 5 V \pm 10\%$ ,  $T_A^\dagger = -55^\circ\text{C to } +125^\circ\text{C}$ 

Parameter Symbol	Parameter Description	Am7202-40		Am7202-50		Am7202-65		Am7202-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write and Flag Timing</b>										
$t_{WC}$	Write Cycle Time	50		65		80		100		ns
$t_{WPW}$	Write Pulse Width	40		50		65		80		ns
$t_{WR}$	Write Recovery Time	10		15		15		20		ns
$t_{DS}$	Data Setup Time	20		30		30		40		ns
$t_{DH}$	Data Hold Time	0		5		10		10		ns
$t_{WFF}$	Write LOW to Full Flag LOW		35		45		60		60	ns
$t_{WHF}$	Write LOW to Half-Full Flag LOW		50		65		80		100	ns
$t_{WEF}$	Write HIGH to Empty Flag HIGH		35		45		60		60	ns
$t_{WLZ}$	Write pulse HIGH to data bus at LOW Z (Note 1)	10		15		15		15		ns
<b>Read and Flag Timing</b>										
$t_{RC}$	Read Cycle Time	50		65		80		100		ns
$t_A$	Access Time		40		50		65		80	ns
$t_{RR}$	Read Recovery Time	10		15		15		20		ns
$t_{RPW}$	Read Pulse Width	40		50		65		80		ns
$t_{RLZ}$	Read pulse LOW to data bus at LOW Z (Note 1)	5		10		10		10		ns
$t_{DV}$	Data Valid from read pulse HIGH	5		5		5		5		ns
$t_{RHZ}$	Read pulse HIGH to data bus at HIGH Z (Note 1)		25		30		30		30	ns
$t_{RFF}$	Read HIGH to Full Flag HIGH		35		45		60		60	ns
$t_{RHF}$	Read HIGH to Half-Full-Flag HIGH		50		65		80		100	ns
$t_{REF}$	Read LOW to Empty Flag LOW		30		45		60		60	ns
<b>Reset Timing</b>										
$t_{RSC}$	Reset Cycle Time	50		65		80		100		ns
$t_{RS}$	Reset Pulse Width	40		50		65		80		ns
$t_{RSS}$	Reset Setup Time	40		50		65		80		ns
$t_{RSR}$	Reset Recovery Time	10		15		15		20		ns
$t_{EFL}$	Reset to Empty Flag LOW		50		65		80		100	ns
$t_{HFH}$	Reset to Half-Full Flag High		50		65		80		100	ns
$t_{FFH}$	Reset to Full Flag HIGH		50		65		80		100	ns
<b>Retransmit Timing</b>										
$t_{RTC}$	Retransmit Cycle Time	50		65		80		100		ns
$t_{RT}$	Retransmit Pulse Width	40		50		65		80		ns
$t_{RTR}$	Retransmit Recovery Time	10		15		15		20		ns

Note: 1. Characterized parameters.

† Instant-On Case Temperature.



# Am7203-40/50/65/80

High Density First-in First-out (FIFO) 2048x9 CMOS Memory

## DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 2048x9 organization
- Cycle times of 50/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption
  - 90 mA max, -50/65/80
  - 100 mA max, -40
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for  $\bar{X}1$  - CMOS threshold
- Functional and pin compatible with industry standard devices

## GENERAL DESCRIPTION

The Am7203 is a RAM-based CMOS FIFO that is 2048 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 20 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7203 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7203 useful in communication, image processing, mass storage, DSP, and printing systems.

## BLOCK DIAGRAM

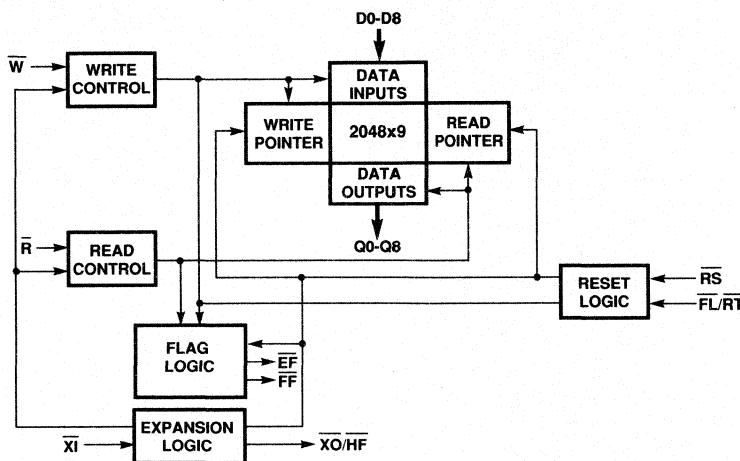
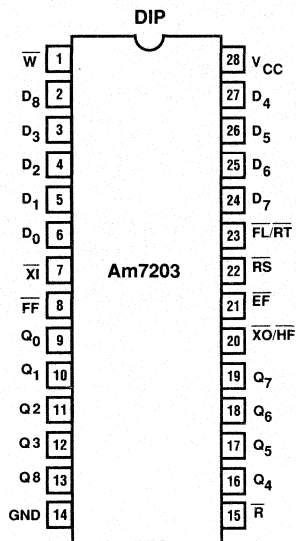


Figure 1.

## CONNECTION DIAGRAMS



**Pin Designations:**

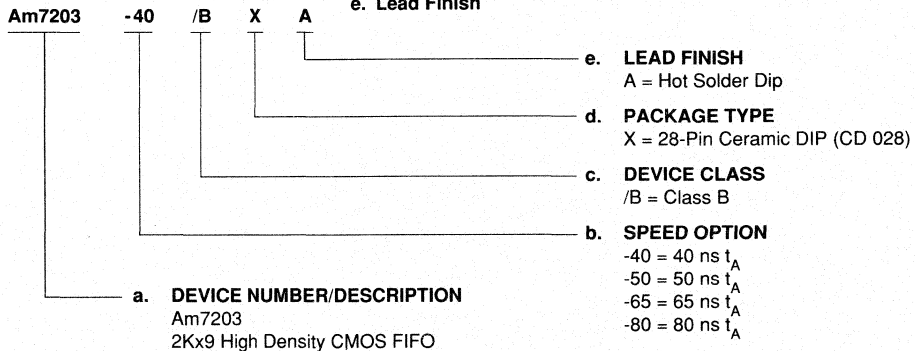
- $\overline{W}$  = Write
- $\overline{R}$  = Read
- $\overline{RS}$  = Reset
- $\overline{FL/RT}$  = First Load/Retransmit
- $D_x$  = Data In
- $Q_x$  = Data Out
- $XI$  = Expansion In
- $XO/HF$  = Expansion Out/Half-Full Flag
- $\overline{FF}$  = Full Flag
- $\overline{EF}$  = Empty Flag
- $V_{CC}$  = Supply Voltage
- GND = Ground

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
Am7203-40	/BXA
Am7203-50	
Am7203-65	
Am7203-80	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{CC}$ .....	-0.5 V to + 7.0 V
Input voltage .....	-0.5 V to $V_{CC} + 0.5$ V
Operating temperature .....	-55°C to +125°C
Storage temperature .....	-65°C to + 150°C
Power dissipation .....	2.0 W
DC output current .....	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

## DC CHARACTERISTICS Military: $V_{CC} = 5 \text{ V} \pm 10\%$ , $T_A^\dagger = -55^\circ\text{C to } + 125^\circ\text{C}$

Parameter Symbol	Parameter Description	Am7203-40 $t_A = 40 \text{ ns}$		Am7203-50 $t_A = 50 \text{ ns}$		Am7203-65 $t_A = 65 \text{ ns}$		Am7203-80 $t_A = 80 \text{ ns}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$I_{IL}$	Input Leakage Current (any input) (Note 1)	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$I_{IO}$	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	$\mu\text{A}$
$V_{IH}$	Input High Voltage (all inputs except $\overline{XI}$ ) (Note 3)	2.2	-	2.2	-	2.2	-	2.2	-	V
$V_{IL}$	Input Low Voltage (all inputs except $\overline{XI}$ ) (Note 3)	-	0.8	-	0.8	-	0.8	-	0.8	V
$V_{IHXI}$	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	-	3.5	-	3.5	-	3.5	-	V
$V_{ILXI}$	Input Low Voltage, $\overline{XI}$ (Note 3)	-	1.5	-	1.5	-	1.5	-	1.5	V
$V_{OH}$	Output Logic "1" Voltage $I_{OH} = -2 \text{ mA}$	2.4	-	2.4	-	2.4	-	2.4	-	V
$V_{OL}$	Output Logic "0" voltage $I_{OL} = 8 \text{ mA}$	-	0.4	-	0.4	-	0.4	-	0.4	V
$I_{CC1}$	Average $V_{CC}$ Power Supply Current (Note 4)	-	100	-	90	-	90	-	90	mA
$I_{CC2}$	Average Standby Current ( $R = W = RS = FL/RT = V_{IH}$ ) (Note 4)	-	25	-	25	-	25	-	25	mA
$I_{CC3}$	Power Down Current (all inputs = $V_{CC} - 0.2 \text{ V}$ ) (Note 4)	-	5	-	5	-	5	-	5	mA

- Notes: 1. Measurements with  $GND \leq V_{IN} \leq V_{CC}$ .  
 2.  $R \geq V_{IH}$ ,  $GND \leq V_{OUT} \leq V_{CC}$ .  
 3.  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 4.  $I_{CC}$  measurements are made with outputs open.  
 † Instant-On Case Temperature.

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**AC CHARACTERISTICS**  $V_{CC} = 5 V \pm 10\%$ ,  $T_A \dagger = -55^\circ C$  to  $+ 125^\circ C$ 

Parameter Symbol	Parameter Description	Am7203-40		Am7203-50		Am7203-65		Am7203-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write and Flag Timing</b>										
$t_{WC}$	Write Cycle Time	50		65		80		100		ns
$t_{WPW}$	Write Pulse Width	40		50		65		80		ns
$t_{WR}$	Write Recovery Time	10		15		15		20		ns
$t_{DS}$	Data Setup Time	20		30		30		40		ns
$t_{DH}$	Data Hold Time	0		5		10		10		ns
$t_{WFF}$	Write LOW to Full Flag LOW		35		45		60		60	ns
$t_{WHF}$	Write LOW to Half-Full Flag LOW		50		65		80		100	ns
$t_{WEF}$	Write HIGH to Empty Flag HIGH		35		45		60		60	ns
$t_{WLZ}$	Write pulse HIGH to data bus at LOW Z (Note 1)	10		15		15		15		ns
<b>Read and Flag Timing</b>										
$t_{RC}$	Read Cycle Time	50		65		80		100		ns
$t_A$	Access Time		40		50		65		80	ns
$t_{RR}$	Read Recovery Time	10		15		15		20		ns
$t_{RPW}$	Read Pulse Width	40		50		65		80		ns
$t_{RLZ}$	Read pulse LOW to data bus at LOW Z (Note 1)	5		10		10		10		ns
$t_{DV}$	Data Valid from read pulse HIGH	5		5		5		5		ns
$t_{RHZ}$	Read pulse HIGH to data bus at HIGH Z (Note 1)		25		30		30		30	ns
$t_{RFF}$	Read HIGH to Full Flag HIGH		35		45		60		60	ns
$t_{RHF}$	Read HIGH to Half-Full-Flag HIGH		50		65		80		100	ns
$t_{REF}$	Read LOW to Empty Flag LOW		30		45		60		60	ns
<b>Reset Timing</b>										
$t_{RSC}$	Reset Cycle Time	50		65		80		100		ns
$t_{RS}$	Reset Pulse Width	40		50		65		80		ns
$t_{RSS}$	Reset Setup Time	40		50		65		80		ns
$t_{RSR}$	Reset Recovery Time	10		15		15		20		ns
$t_{EFL}$	Reset to Empty Flag LOW		50		65		80		100	ns
$t_{HFH}$	Reset to Half-Full Flag High		50		65		80		100	ns
$t_{FFH}$	Reset to Full Flag HIGH		50		65		80		100	ns
<b>Retransmit Timing</b>										
$t_{RTC}$	Retransmit Cycle Time	50		65		80		100		ns
$t_{RT}$	Retransmit Pulse Width	40		50		65		80		ns
$t_{RTR}$	Retransmit Recovery Time	10		15		15		20		ns

Notes: 1. Characterized parameters.

† Instant -On Case Temperature.



# FIFOs: Rubber-Band Memories to Hold Your System Together

Chuck Hastings

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Data-rate matching problems are a very basic part of the life of a builder of digital systems. Today there are components called "FIFOs" which lets you keep your hardware design simple, and lets each portion of your system see the data rate which it wants to see, and yet lets you avoid hobbling the performance of your software by constantly interrupting or intermittently halting your microprocessor. FIFO is one of those made-up words, or acronyms, formed from the initials of a phrase – in this case, "First-In,

First-Out." FIFOs may be thought of as "elastic storage" devices – "logical rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-by-microsecond basis, but only need to average out to be the same over a much longer period of time. This tutorial paper both describes what FIFOs are in general, and introduces the 64x4 and 64x5 AMD's FIFOs in particular.

# FIFOs: Rubber-Band Memories to Hold Your System Together

Chuck Hastings

## Introduction

Data-rate matching problems are a very basic part of the life of a builder of digital systems. Some important electromechanical devices such as disk drives produce or absorb data at totally inflexible rates governed by media recording densities and by the speeds at which small electric motors are naturally willing to rotate. Other devices such as letter-quality printers have maximum data rates beyond which they cannot be hurried up, and which are relatively slow compared to the rates of other devices in the system.

Microprocessors and their associated main memories are generally faster and more flexible than the other system components, but they often operate with severely degraded efficiency if they must be diverted from their main tasks every few milliseconds to handle data-ready interrupts for individual dribs and drabs of data. While "one day at a time" may be a sound principle by which to live your life, "one bit at a time" or even "one byte at a time" is not a philosophy by which to make your microprocessor live if you want the best possible service from it.

Today there are components called "FIFOs" which let you keep your hardware design simple, and let each portion of your system see the data rate which it wants to see, and yet let you avoid hobbling the performance of your software by constantly interrupting your microprocessor, or even by intermittently halting it in order to let DMA (Direct Memory Access) circuits take over control of the main memory for a short time. FIFOs may be thought of as "elastic storage" devices — "logical rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-by-microsecond basis, but only need to average out to be the same over a much longer period of time.

This tutorial paper both describes what FIFOs are in general, and introduces the 64x4 and 64x5 FIFOs in particular.

## What is a FIFO?

FIFO is one of those made-up words, or *acronyms*, formed from the initials of a phrase — in this case, "First-In, First-Out." Originally, the phrase "First-In, First-Out" came from the field of operations research, where it describes a *queue discipline* which may be applied to the processing of the elements of any *queue* or waiting line. There is also a LIFO, or "Last-In, First-Out" queue discipline. The terms FIFO and LIFO have also been used for many years by accountants to describe formal procedures for allocating the costs of items withdrawn from an inventory, where these items have been bought over a period of time at varying prices.

You can probably think of some simple, everyday objects which in some manner behave according to the FIFO queue discipline. For instance, little two-seater cable-drawn boats are drawn through an amusement park tunnel of love one by one, and must emerge from the other end in the same order in which they entered the tunnel — "First-In, First-Out." The old-time coin dispensers used by the attendants at such amusement park features, or by city bus drivers, are "buffer storage" devices which handle coins in this same manner. (See Figure 1.)

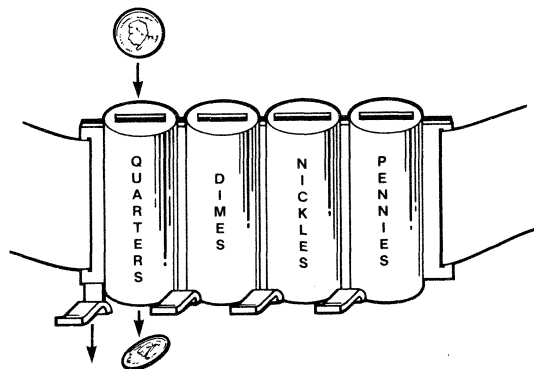


Figure 1. Primitive Mechanical FIFO Device

Notice also that the input of a coin into one of the tubes of such a coin dispenser through the slot at the top, and the output of a coin at the bottom of that tube when the lever for that tube is pushed, are completely independent events which do not have to be synchronized in any way, as long as the tube is neither totally empty nor totally full. However, if the tube fills up completely, a coin inserted into the slot will not go into the tube. Likewise, if the tube empties out completely, no coin is released from the tube at the bottom when the lever is pressed. The coin tube thus behaves as an *asynchronous* FIFO. Keep this homely example in mind.

In computer technology, both the FIFO queue discipline and the LIFO queue discipline are frequently used to control the insertion and withdrawal of information from a buffer memory, or from a dedicated buffer region of some larger memory. In input/output programming practice, a FIFO memory region is sometimes referred to as a *circular buffer*, and in programming for computer-controlled telephone systems it is called a *hopper*. A LIFO memory region is usually referred to as a *stack*.



## FIFOs: Rubber-Band Memories to Hold Your System Together

Both FIFO and LIFO memories have frequently been implemented as special-purpose digital systems or subsystems, but as of the present time only FIFO memories are commonly implemented as individual, self-contained semiconductor devices.

### Representative FIFOs

To give you the flavor of what these semiconductor devices are like, I'll describe the type 67401 64x4 FIFO and type 67402 64x5 FIFO which have been available for several years from Advanced Micro Devices. ("64x4" here means containing 64 words of 4 bits each.) These parts have a basic, easy-to-understand architecture and control philosophy. They also happen to be the fastest FIFOs available through normal commercial channels as of this writing, and they are in widespread use for applications ranging from microcomputers up to IBM-lookalike mainframes and large special-purpose military radar processors. A 67401 is internally organized as follows:

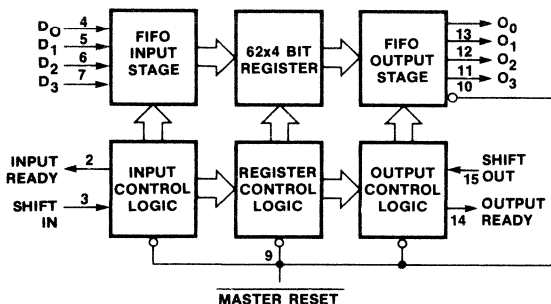


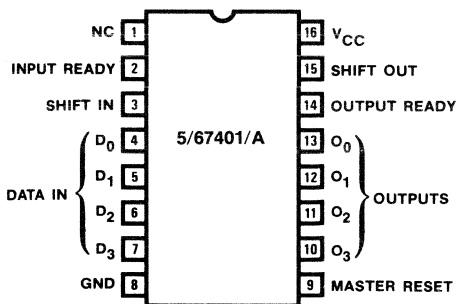
Figure 2. Architecture of the 67401 FIFO

The list of signals/pins for the 67401 is:

TYPE	HOW MANY	(CUM.)	I/O/V
Data In	4	4	I
Output	4	8	O
Control:			
Shift In	1	9	I
Shift Out	1	10	I
Master Reset	1	11	I
Status:			
Input Ready	1	12	O
Output Ready	1	13	O
Not Connected	1	14	—
Voltage:			
V <sub>CC</sub> (+5V)	1	15	V
Ground	1	16	V

The corresponding list for the 67402 differs only in that there are 5 Data In lines rather than 4, and 5 Output lines rather than 4. The reason that there is an unused pin is that the 67401 was

originally designed as a faster bipolar upgrade of a MOS part, the Fairchild 3341, which needs a second power-supply voltage (-12V) as well as V<sub>CC</sub>. Much of the description to be given here of the 67401 also applies to the 3341, except for data rate — the 67401 can operate at 5 to 35 MHz depending on the exact version, compared with approximately 1 MHz for the 3341. Pinouts are:



(Note: "NC" pin is -12V for 3341.)

Figure 3. 67401/3341 Pinout

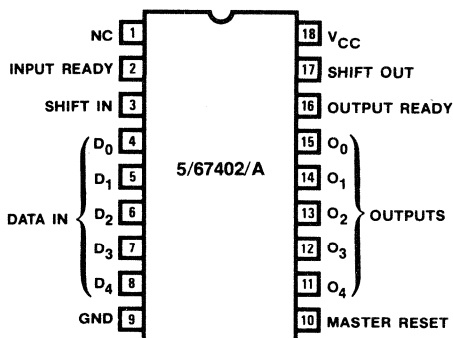
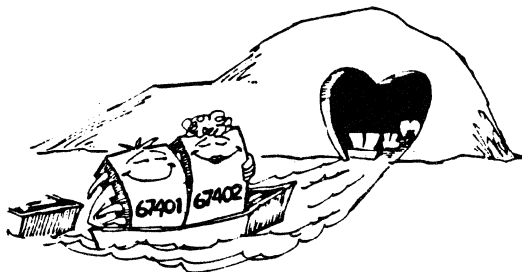


Figure 4. 67402 Pinout



"FIRST-IN, FIRST-OUT" ... DESCRIBES A QUEUE DISCIPLINE WHICH MAY BE APPLIED TO THE PROCESSING OF THE ELEMENTS OF ANY QUEUE ..."

2

## FIFOs: Rubber-Band Memories to Hold Your System Together

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The reason for having a 5-bit model as well as a 4-bit model of basically the same part is that if two 4-bit FIFOs are placed side-by-side they make only an 8-bit FIFO, and many people have FIFO applications which entail using a parity bit with each byte, and/or a frame-marker bit with the last byte of a frame or block, which means that they want 9-bit or 10-bit FIFOs. A 67402 next to a 67401 makes a 9-bit FIFO, and two 67402s make a 10-bit FIFO. But I'm getting ahead of myself.

A logic HIGH signal on the Input Ready line indicates that there is at least one vacant memory location within the FIFO into which a new data word may be inserted. Likewise, a logic HIGH on the Output Ready line indicates that there is at least one data word currently stored within the FIFO and available for reading at the outputs. The operation of the FIFO is such that, once a data word has been inserted at the Data In lines (the *top* of the FIFO, as it were), this word automatically *sinks all the way to the bottom* (assuming that the FIFO was previously empty) and forthwith appears at the Output lines. (Remember the synonym *hopper*?) In keeping with the FIFO queue discipline, the first word which was inserted is the first one available at the outputs, and additional words may be withdrawn *only* in the order in which they were originally inserted.

There is no provision for *random access* in these FIFOs, since their internal implementation uses one particular variation of shift-register technology. Each FIFO word consists of 4 (for the 67401) or 5 (for the 67402) data bits, plus a control or "presence" bit which indicates whether or not the word contains significant information. There are thus 4 or 5 data "tracks" and one presence "track" if you look at a FIFO *from a magnetic-tape perspective*. What the Master Reset input does is to clear all of the bits in the presence track, and in addition to clear the very last data word (at the "bottom") which controls the Output lines. The other 63 data words are not cleared, but it doesn't really matter; their status is like unto that of operating-system files whose Directory entries have been deleted, in that they can no longer be read out and will get written over as soon as new information comes in.

We now return to what happens when a new data word gets inserted at the "top" of the FIFO. A mark (call it a "one") is made in the presence bit for word 00, the first word. Assume now that word 01 is vacant, so that there is a "zero" in its presence bit. The internal logic of the FIFO then operates so that the data from word 00 is automatically written into word 01, the presence bit for word 01 is automatically set to "one," and the presence bit for word 00 is automatically reset to "zero." If word 02 is likewise vacant, the process gets repeated, and so forth until the same piece of data has settled into the lowest *vacant* word in the FIFO — the next lower word, and all the rest, have "ones" in their presence bits, blocking further changes.

Conversely, now assume that at the moment no data word is being input, but that one has just been output. Then the bottom word in the FIFO — word 63 — has a "zero" in its presence bit, but there are a number of other words above it which have "ones" in their presence bits. The data in word 62 then moves into word 63 in the same manner described above, and the data in word 61 moves into word 62, and so forth, until there is no longer any word in the FIFO having a "one" in its presence bit which is above a word having a "zero" in its presence bit. The effect is that of empty locations bubbling up to the top of the FIFO. Or, in case you are one of those elite individuals who has

been exposed to the concepts and jargon of modern semiconductor theory, you may prefer to think of the FIFO operation as one in which data ("electrons") flow from the top of the FIFO to the bottom, and vacancies ("holes") flow from the bottom of the FIFO to the top. In the general case, of course, new data words are being input at the top and old ones are being output at the bottom at random times, and there is a dynamic and continually changing situation within the FIFO as the new data words drop towards the bottom and the vacancies bubble up towards the top, and they intermix along the way.

An obvious consequence of this manner of operation in shift-register-technology FIFOs is that it takes quite a bit longer for a data word to pass all the way through the FIFO than the minimum time between successive input or output operations. There are various versions of the 67401 and 67402, rated at 5, 7, 10, 15, 167 or 35 MHz over commercial (0° C to +75° C) or military (-55° C to +125° C) temperature ranges. Thus, for instance, a 15-MHz FIFO can input data words at the top and/or output data words at the bottom at a sustained rate of a word every 66-2/3 nanoseconds. However, the "fall-through time"  $t_{PT}$  for these same FIFOs is stated in the data sheet as 1.6 microseconds, which is a long enough time for 24 words to be input or 24 words to be output! There is in principle also a "bubble-through" time for a single vacancy to travel from word 63 all the way back to word 00, which should be identical to  $t_{PT}$ , and probably is although as *measured* on a semiconductor tester it may differ by as much as 50 nanoseconds, which is probably due to artifacts of measurement. By the way, the stated operating frequencies and the  $t_{PT}$  value are "worst-case" (guaranteed) numbers; the "typical" values observed in actual parts are necessarily somewhat better, since semiconductor manufacturers are obliged to take any parts back which customers can prove do not meet the worst-case numbers, and some margin of safety is always nice (see reference 1).

Besides AMD, other manufacturers of high-speed FIFOs include National Semiconductor, Mostek, National Semiconductor, RCA, Texas Instruments, and TRW LSI Products. Slow MOS FIFOs are available from National Semiconductor, Texas Instruments, Western Digital, and Zilog. FIFOs in development or available at just about all of these vendors also offer new bells and whistles which I haven't discussed, such as three-state outputs, serial (one-bit-at-a-time) as well as parallel data ports, and additional status flags. TRW's new FIFO, for instance, has a "half-full" flag which tells when half of the FIFO's words contain data. AMD now has the 67413 FIFO which supplies not only this flag, but also a second flag which indicates that the FIFO is either "almost full" (within eight words of full) or "almost empty" (within eight words of empty, reminiscent of the "yellow warning interrupt" in Digital Equipment Corporation's PDP-11 computers. This "almost-full/empty flag" can be used as an interrupt to a microprocessor to indicate that *some* action must be taken, and the microprocessor can then examine the "half-full flag" to see what it actually has to do.

There are also other design approaches to the insides of a FIFO besides the one based on shift-register technology which has been described here. For instance, a FIFO may be organized as a random-access memory ("RAM") with two counters capable of addressing the RAM right within the chip, an "in-pointer" and an "out-pointer." The counting sequences, of course, "wrap

## FIFOs: Rubber-Band Memories to Hold Your System Together

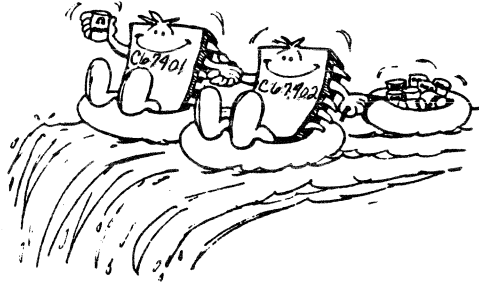
around" from the highest RAM address back to zero. The out-pointer chases the in-pointer, the region just traversed by the in-pointer but not yet by the out-pointer contains significant data, and the complementary region is logically "empty." This approach involves good news and bad news: the good news is that the long fall-through time goes away, but the bad news is that now reading and writing typically interfere with each other — unless the RAM is "two-port," they cannot be done simultaneously at all. Also, since this approach is more costly in "silicon area" than the shift-register approach, it would not result in as large FIFO capacities for the same size die or the same power consumption. In practice, this approach has only been used for MOS FIFOs which have turned out to be quite slow.

Another design approach is somewhat intermediate between the pure RAM approach as just described and the shift-register approach. It uses "ring counters" on the chip instead of full-blown binary counters. What this means in practice is that there are now two extra "tracks" along with the data tracks within the FIFO, plus also an input data bus and an output data bus. Single "one" bits move along the in-pointer track and the out-pointer track, and the out-pointer chases the in-pointer as before. The RAM is effectively two-port, and the two parallel buses both go to each and every word. Texas Instruments has announced some small (16x4) bipolar FIFOs based on this technical approach. Like the pure RAM approach, it gets rid of the fall-through time but needs proportionally more silicon area to store a given number of bits.

### Designing with FIFOs

Returning now to the 67401 and 67402, if what you really need is a "deeper" FIFO, say 128x4 instead of just 64x4, these parts are designed to cascade using a simple "handshaking" procedure, without any external logic at all! If FIFO B follows FIFO A in the cascading sequence, the Shift In control input of FIFO B is connected to the Output Ready status output of FIFO a, and

likewise the Shift Out control input of FIFO A is connected to the Input Ready status output of FIFO B, and the Master Reset control inputs are all tied together. (See Figure 5.) That's all there is to it. Any number of FIFOs may be cascaded in this manner.



"...THE 67401 AND 67402... ARE DESIGNED TO CASCADE USING A SIMPLE "HANDSHAKING" PROCEDURE..."

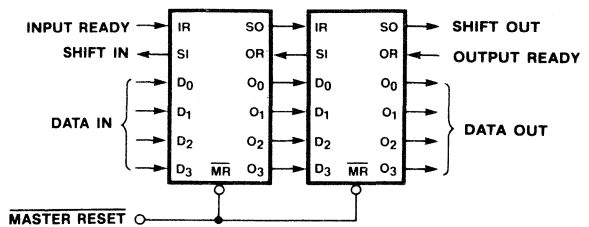


Figure 5. Cascading FIFOs to Form 128x4 FIFO

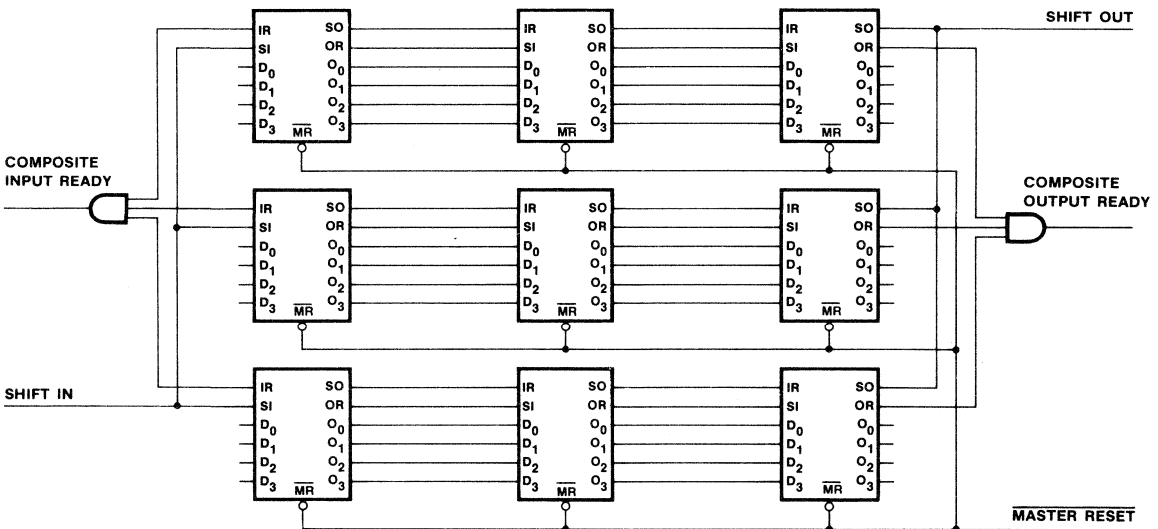


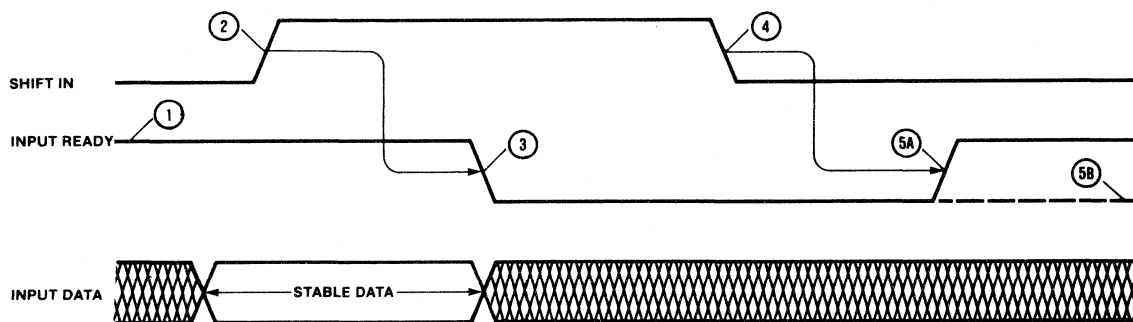
Figure 6. 192x12 FIFO

## FIFOs: Rubber-Band Memories to Hold Your System Together

If what you *really* need is a “wider” FIFO, then you simply arrange 64x4 or 64x5 FIFOs side-by-side up to the required width. Then, you use an external AND gate such as a 74S08 or 74S11 to AND the Input Ready signals of the first rank of FIFOs if there is more than one rank, or of the only rank of FIFOs if there isn't. (See Figure 6.) Likewise, a similar AND gate is also needed to AND the Output Ready signals of the last rank of FIFOs. If you didn't provide these AND gates and just took the Input Ready signal of one FIFO as representative of when the whole array was ready, you would be taking the rather large gamble that you had correctly chosen the slowest row in this array — and if you chose wrong, 4-bit or 5-bit chunks of your input word might not get read correctly into the FIFO where they were supposed to go. Ditto on the output side. So like use the AND gates.

Although a humungous number of 67401s and 67402s are in use worldwide giving hassle-free service, it should be kept in mind that these devices are *asynchronous sequential circuits*. (One

definition of “asynchronous sequential circuit” is “a fortuitous collection of race conditions,” but that definition is unduly sardonic for very carefully designed parts such as these.) If your board is subject to noise, or if certain data sheet setup-time and hold-time conditions are occasionally not met, errors may occur. It is prudent system-design practice to every so often allow an array of FIFOs to empty out completely, and then issue a Master Reset. (I'm assuming, of course, to start with that you're not the kind of turkey who has to be *told* to issue a Master Reset as part of your power-up sequence.) In the event that you still get what appear to be occasional errors, very small (say from 22 to 68 picofarads) capacitors from both the Shift In control input and the Shift Out input of a FIFO to ground will often eliminate these. But by all means start with a *good* circuit board — these are high-speed-Schottky-technology circuits, and like to see a lot of ground-plane metal on the board, along with other reputable interconnection practices such as 0.1-microfarad disk capacitors between  $V_{CC}$  and ground for each chip to bypass switching noise.



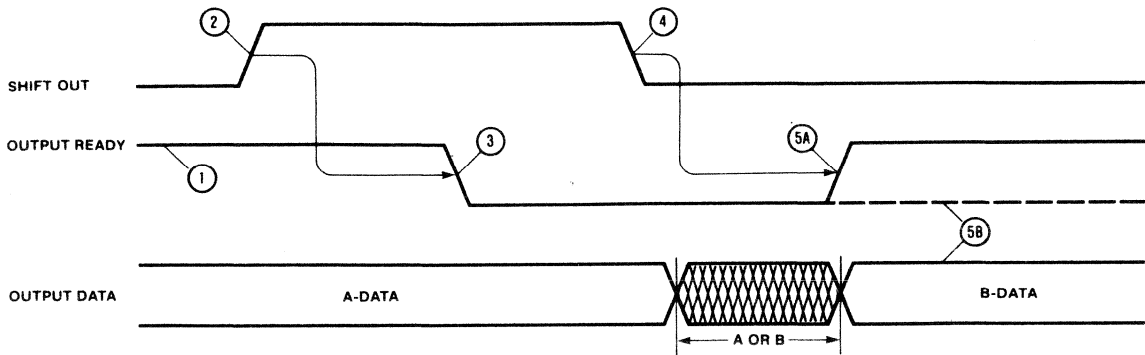
- ① Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
- ② Input Data is loaded into the first word.
- ③ Input Ready goes LOW indicating the first word is full.
- ④ The Data from the first word is released for “fall-through” to second word.
- ⑤A The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.
- ⑤B If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

Figure 7. Sequence of Events When a Data Word is Shifted into a FIFO

The sequence of events which occurs during the operation of shifting a new data word into the “top” of a FIFO is shown in Figure 7, and the corresponding sequence of events for shifting out the bottom word is shown in Figure 8. In both of these figures, it has been assumed that the external logic — whether it

be the rest of your system, or just another FIFO — refrains from raising the respective Shift line to HIGH until the respective Ready line has gone HIGH, if the Shift line is raised any earlier, it simply gets ignored.

## FIFOs: Rubber-Band Memories to Hold Your System Together



- ① Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
- ② Shift Out goes HIGH causing the next step.
- ③ Output Ready goes LOW.
- ④ Contents of word 62 (B-DATA) are released for "fall through" to word 63.
- ⑤A Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
- ⑤B If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

**Figure 8. Sequence of Events When a Data Word is Shifted Out of a FIFO.**

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When two FIFOs are cascaded as shown in Figure 5, the sequences of events shown in Figures 7 and 8 are subject to the additional ground rule that the Output Ready line of the FIFO on the left in Figure 5 (call it "FIFO A") is identically the Shift In line of the FIFO on the right (call it "FIFO B"). And likewise, the Input Ready line of FIFO B is identically the Shift Out line of FIFO A. In the terminology we have been using, FIFO A is the "upper" FIFO and FIFO B is the "lower" FIFO. Although you do not normally need to be concerned about what happens when two FIFOs are hooked together for cascaded operation in this manner, since the "handshake" occurs quite automatically without the rest of your logic having to do anything to make it happen, it is an illuminating exercise to consider Figures 7 and 8 together in this light and see why the cascading works.

In the general case, both FIFO A and FIFO B are neither completely full nor completely empty. Thus, from the description already given of FIFO internal operation, after some period of time there will be a significant piece of data in word 63 of FIFO A and a "one" in the presence bit for that word. Since the word-63 presence bit is what controls the Output Ready signal, the latter will at some point in time go HIGH, and at that same point in time the data word in FIFO A word 63 is present at the output lines. Likewise, after some period of time there will be a vacancy in word 00 of FIFO B, and a "zero" in the presence bit for that word which in turn results in the Input Ready signal going HIGH. Remembering now that each of these Ready signals is in fact the respectively-opposite Shift signal for the other FIFO, it may be seen from Figure 7 that the conditions for inputting a word into FIFO B have now been met, and from Figure 8 that the conditions for outputting a word from FIFO A and allowing the next available piece of data from somewhere further "up" in FIFO A to enter FIFO A word 63 have also been

met. The time delays shown in both Figure 7 and Figure 8 from the event at 2 to the event at 3, and from the event at 4 to the event at 5A, are asynchronous internal-logic-determined times of the order of 4 or 5 gate delays, where the gates in question are high-speed-Schottky LSI *internal* gates and have significantly less propagation delay than the SSI gates you can read about in data sheets.

After a single data word has made it across the interface from FIFO A into FIFO B, each FIFO from then on behaves in accordance with the operating rules already described, with the exact sequence of events depending on the rate at which new data words are input into FIFO A and the rate at which old data words are withdrawn from FIFO B. The net effect is that the combination of FIFO A and FIFO B with this hookup behaves almost exactly like a single integrated 128x4 FIFO. In fact, the "handshake" timing/control sequence for getting a data word from FIFO A across FIFO B is almost a replica of that which occurs within each FIFO, when the internal logic associated with word *n* interfaces with that associated with word *n+1* for the purpose of allowing a data word to advance from occupying word *n* to filling a vacancy in word *n+1*.

Returning now to applying the timing analysis shown in Figures 7 and 8 to the case of FIFO A and FIFO B operating in cascaded mode, notice that each movement (rising or falling) of the Ready signal for one FIFO is activated by the movement in the opposite sense (falling or rising, that is) for the Ready signal from the other part. The two signals, ORA/SIB (meaning "Output Ready A" which is the same signal as "Shift In B") and IRB/SOA, cannot both remain HIGH at the same time for more than a few nanoseconds, since if they are both HIGH a data word will pass between the two FIFOs as already described. So, at the point

## FIFOs: Rubber-Band Memories to Hold Your System Together

when *both* the sequence of events shown in Figure 7 and the sequence of events shown in Figure 8 have been completed, and consequently ORA/SIB and IRB/SOA have both gone HIGH again, another similar sequence of events occurs for both FIFOs and another word is passed, and so forth. This process continues apace until either ORA/SIB sticks LOW, which can happen if FIFO A gets completely emptied out of data words and has "zeroes" everywhere in its presence track; or until IRB/SOA sticks LOW, which can likewise happen if FIFO B gets completely filled and has "ones" everywhere in its presence track. When such a deadlock situation occurs, it lasts until a new data word has been input into FIFO A and has had time to "fall all the way through" and settle into FIFO A word 63, or until the data word in word 63 of FIFO B has been read out and the resulting vacancy has had time to "bubble all the way back up" into FIFO B word 00, as the case may be.

### Various Uses for FIFOs

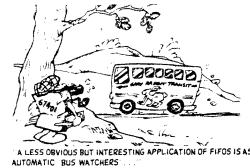
The classical FIFO application, as already mentioned at the beginning of this paper, is that of matching the instantaneous data rates of two digital systems in a simple, economical way. One of the two systems may, for reasons of design economics or even of utter necessity, want to emit or absorb data words in ultra-high-speed bursts, whereas the other one may prefer to operate at a slow-but-steady data rate or even at an erratic rate which varies between ultra-slow and slow or even between slow and fast. No matter — it's all the same to an asynchronous FIFO such as the 67401 or 67402, as long as the input rate and the output rate do match up over a long period of time so that it neither fills up nor empties out.

There are, however, some additional uses for FIFOs which arise from other, rather different circumstances. For instance, your digital system may simply need some extra buffer storage scattered around locally at different points on your block diagram, and you and your system may really just not care whether this storage is accessed on a random or on a queue basis. Under these circumstances, it is ordinarily less hassle to use a FIFO than to use a small RAM and come up with some extra logic to generate addresses and timing signals for it. Often the FIFO modulus operand is in fact the natural one for the application; as for instance when your system must accumulate a block of 64 characters and then run them by all at once in order to examine them for the presence of some control character, using some scanning logic — or perhaps even a microprocessor — which is otherwise occupied most of the time.

A less obvious but interesting application of FIFOs is as automatic "bus-watchers" for jump-history recording for hardware or even software diagnostic purposes. A FIFO whose inputs are connected to a minicomputer's program counter or microprogram counter, or to a microcomputer's main address bus, may be operated so as to record every new jump address generated by the program. This way, if at some point the hardware freaks out or the operating system crashes, a record exists of the last 64 jumps which were taken before the system was halted, assuming of course that you have provided some way for the system to sense that all is not well and halt itself. Such a record of jumps can be very valuable in tracing out what

happened just before everything went haywire. FIFOs may be used in this way either as part of built-in self-monitoring features in digital systems, or as part of various kinds of external test equipment.

FIFOs may also be used as controllable delay elements for digital information which cannot be used immediately upon receipt — perhaps it must be matched against other information which is not yet available, or perhaps it must be synchronized with other streams of information which are out of phase by a varying amount. An example of the latter situation is deskewing several bit-streams off a parallel-format magnetic tape, which commonly has to be done when high recording densities are used. One FIFO *per bit-stream* is required — but the net resulting logic may still be the most reliable and economical way to get the job done, when compared with other possible digital designs. Another example is that of using FIFOs as data memories in digital correlators; the lag in an autocorrelation operation can be set simply by controlling how many words are in the FIFO at one time, and so forth. There are even some applications in which it is advantageous to operate a FIFO with all of its input and output cycles synchronized, so that absolutely all it does is to delay the data by some certain number of clock intervals.



### References

1. *Bipolar LSI 1982 Databook*, Monolithic Memories Inc.
2. "First In First Out Memories... Operations and Applications," applications note published March 1978 by Monolithic Memories Inc. A good survey with some thought-provoking ideas. I have to mention one error, however; one circuit diagram shows paralleled FIFO operation in the manner of that of Figure 6 in this paper, but without the use of the AND gates for the composite Ready signals. As I already warned you, that's *dangerous*.
3. "Understanding FIFO's," applications note published by Monolithic Memories Inc. The author, Alan Weisberger, has also had a modified version of this note published as a magazine article, "FIFOs Eliminate the Delay when Data Rates Differ," in *Electronic Design*, November 27, 1981. Despite the general title, the emphasis is on digital communications applications.
4. "PROMs, PALs, FIFOs and Multipliers Team Up to Implement Single-Board High-Performance Audio Spectrum Analyzer," applications note published by Monolithic Memories Inc. The author, Richard Wm. Blasco, also had this note published in *Electronic Design* in two installments, in the issues of August 20 and September 3, 1981 under the titles "PAL Shrinks Audio Spectrum Analyzer" and "PAL Improves Spectrum Analyzer Performance" respectively.



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AR-154

# FIFO RAM Controller Tackles Deep Data Buffering

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# FIFO RAM controller tackles deep data buffering

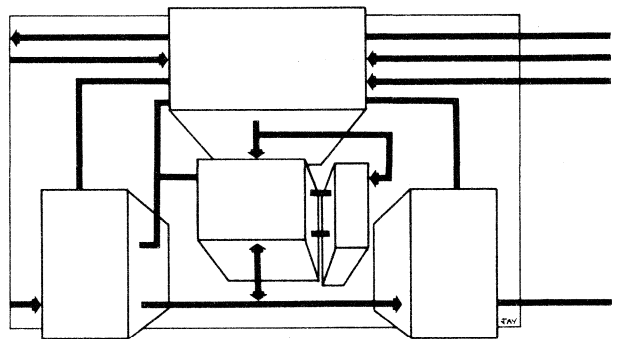
**Buffering large amounts of data has long been a source of design headaches. Extra large FIFO buffers minimize system bottlenecks with an implementation as easy as it is cost-effective.**

Designers are turning to innovative architectures to extend the performance of computer systems. Pipelining is one of these innovations. In pipeline architectures, data is buffered temporarily between a system's processing elements. This allows these processing elements to work more efficiently. Since data transfers can occur asynchronously, designers can minimize bottlenecks in data paths and boost overall performance.

Data buffering, however, is sometimes difficult and costly to implement. In multiprocessing and data communications applications, for example, designers encounter the problem of how to buffer large blocks of sequential data temporarily with minimum cost and trouble. Often, a few thousand to tens of thousands of words must be buffered.

In multiprocessing applications, large blocks of data and instructions are passed between the various processors. Storing information between the processors for a short time lets a sender pass data on without waiting for a receiver to finish its current task, so the sender can more quickly move on to its next task.

For data communications applications, large blocks of data must be transferred from one node to another along a data channel. Temporary buffering on and off the data channel permits each



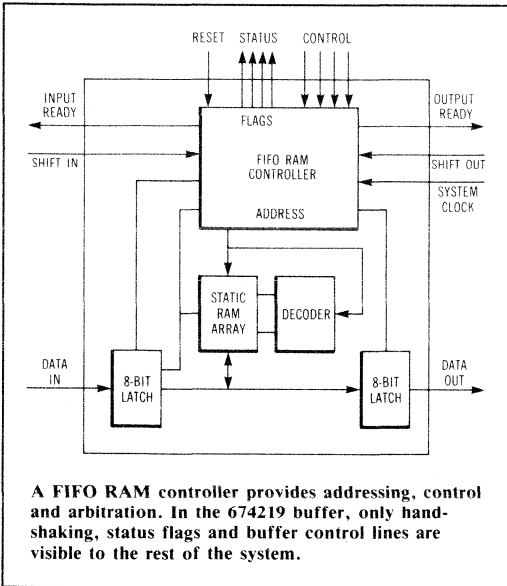
device in the network to work more efficiently. Data can be transferred to the buffer when ready, and the device is free to move on to the next task without waiting for the data channel to be free.

Buffering large amounts of data, often called deep data buffering, can be accomplished through several methods. One technique, direct memory access (DMA), sets aside blocks of main memory as temporary data buffers. When a request for data transfer is received, the DMA controller interrupts the processor and takes control of the memory bus. The controller then moves the data into memory that has been allocated for temporary buffering.

Looking at the advantages of this buffering method, DMA controller chips are relatively inexpensive. Since they require little extra logic, the controllers are simple to implement. The DMA approach, however, has several drawbacks. First, the processor is interrupted every time a data block

Tom Pai





transfer request is made. To transfer data, the processor must hand over control of the memory bus. When many data block transfers occur, system performance is severely degraded. Large blocks of data degrade performance even more.

DMA also limits rates and formats of data. Using this technique, the maximum data rate is limited to the system bus data rate. Bursts of rapid data can't be directly accommodated. Besides, DMA operation is synchronous with system operation, which means that all data transfers—both input and output—must be synchronous with the system clock. Asynchronous data can't be directly accommodated. Another drawback of DMA is that it doesn't allow for simultaneous input and output

operation. This greatly limits the ability of a DMA buffer to act as a pipelining element.

The DMA approach is best suited for systems in which low cost is a top priority, and performance degradation, caused by interruptions to processors during the transfer of data, is tolerable. In effect, designers opting for DMA trade overall system performance, considerations about the rate and format of data and immediate access to information for inexpensive implementation and simple design.

**RAM approach eases bottlenecks**

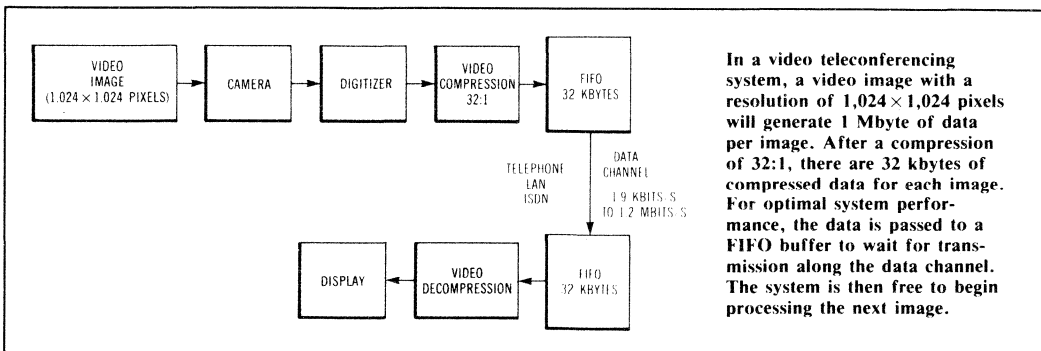
Another approach to deep data buffering involves dual-port RAM devices. A dual-port RAM is placed along the data transfer path and acts as temporary storage for incoming or outgoing data. These devices overcome many of the limitations of DMA. Thanks to two independent ports, data transfers can be completely asynchronous and simultaneous. Since one port can be isolated from the data bus, processors don't have to hand over control of the memory bus during data transfer.

Using dual-port RAMs for data buffering does have its disadvantages; to work as a data buffer, it requires a lot of external and control logic. Counters, comparators and control logic must be added to make the dual-port RAM read and write data sequentially and prevent buffer overflows and underflows from occurring. This external logic can add up to large amounts of valuable board real estate and limits the data rate of the buffer.

Another disadvantage is cost. Dual-port RAMs are 10 times the price of comparable conventional static RAMs; a 1-k × 8-bit device costs \$25 to \$30. Implementing a 4-k × 16-bit buffer will cost approximately \$200 for the RAM device alone.

A third method of buffering data uses first-in, first-out buffers between elements as temporary storage sites. These FIFO devices store and output the data sequentially. Like dual-port RAMs, they

2



## Deep Data Buffering

have two independent asynchronous ports. But one port is dedicated to input, the other to output.

FIFO buffers offer an extremely efficient approach for data buffering. Virtually no external control is required since control and arbitration is performed with on-chip logic. Addressing is eliminated because data is sequential. The streamlined buffering afforded by FIFOs maximizes the data rate, which makes this approach a natural for high-performance systems.

For maximum data rate and design ease, FIFO buffers offer advantages over DMA and dual-port RAM methods. But the devices are geared for data buffering of shallow-to-medium depth. Large data blocks are buffered only by using an array of FIFOs, which requires large amounts of board space, making FIFO buffers too expensive and inefficient for applications with large data amounts.

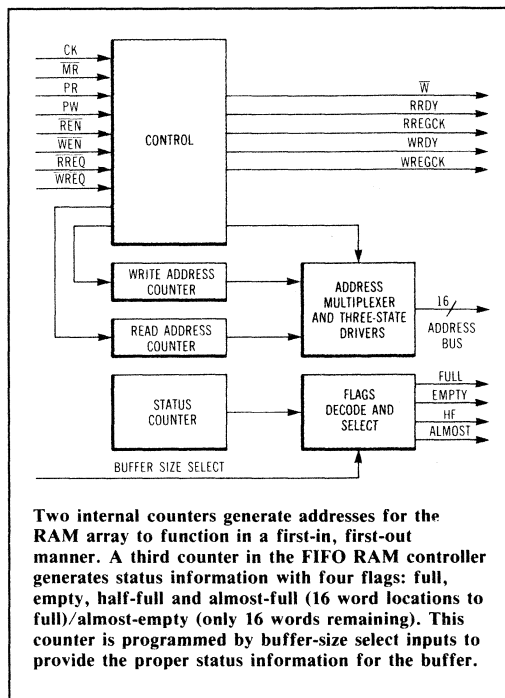
### FIFO RAM controllers tackle deep data

When deep buffering is required, very large FIFO RAM buffers reduce the costs and space problems of conventional FIFO techniques. Devices such as the 674219 FIFO RAM controller can accommodate large amounts of data in high-performance systems. These devices provide the addressing, control, and arbitration logic that enables an array of RAMs to function as a FIFO buffer.

One advantage of this kind of device is the large amount of data it can handle. Using inexpensive single-port static RAMs (or dynamic RAMs with additional external logic), designers can implement a fast, fully asynchronous buffer that can temporarily store from 512 to 65,536 words. In the case of the 674219 FIFO RAM controller, a performance of 12 MHz can be attained. During simultaneous input and output operation, a data rate of 6 MHz is possible.

With two registers for data latching, a few logic gates and a RAM array, these devices can replace any system function block calling for large data buffers. All of the control, arbitration and status logic is placed on a single device, greatly simplifying large FIFO buffer designs. Information about the buffer is provided by four status flags: full, empty, half-full and almost-full/almost-empty. The full and empty flags buffer overflow and underflow. When the buffer is full, attempts to write data into the buffer won't be acknowledged. Data already in the buffer, however, won't be lost. Similarly, the empty flag prevents false data from being read out.

Status flags also help increase the efficiency of buffers and optimize system performance. Together, the half-full and almost flags can in-



Two internal counters generate addresses for the RAM array to function in a first-in, first-out manner. A third counter in the FIFO RAM controller generates status information with four flags: full, empty, half-full and almost-full (16 word locations to full)/almost-empty (only 16 words remaining). This counter is programmed by buffer-size select inputs to provide the proper status information for the buffer.

dicating when the buffer is almost empty and trigger a signal to the source for more data. This ensures a steady stream of data to the receiver. In systems where a receiver, such as a peripheral, is operating at a much slower rate than the source, such as a processor, the processor can send data in high-speed bursts to the buffer and then attend to other tasks while a peripheral accepts the data in a steady, uninterrupted stream.

### Dual-pointer FIFO architecture

FIFO RAM controllers implement a RAM-based FIFO architecture, which uses two pointers. The write pointer contains the address of the next available location in the RAM array to be written and the read pointer has the address of the next location for data to be read. When either pointer is used to access the memory array, it's incremented automatically to point to the next available location. When the pointer reaches the last location, it's reset to zero and the procedure continues.

A third counter provides status information, generates flag logic and prevents overflow and underflow. The -size select inputs program this counter to give the proper status information to the buffer.

In the cycle of a typical system, the buffer is reset with the Master Reset (MR) pin. This sets the read and write pointers to zero and activates the empty flag. A write cycle is initiated by a Write Request (WREQ). The Write Ready (WRDY) line goes low, acknowledging the request. A Write Register Clock (WREGCK) pulse from the FIFO RAM controller latches the data into the write register. Data is then written to the RAM array at the address location provided by the write pointer. When the buffer has valid data, the empty flag will go low, indicating that a read can take place. The read cycle follows the same sequence as the write cycle.

Since a FIFO RAM controller uses low-cost, single-port RAMs, arbitration is needed to resolve simultaneous read and write requests. On-chip arbitration logic determines which request is serviced first. The second request is acknowledged, but will not be serviced until the first request is completed.

Conventional FIFO buffers are based on shift registers. Data is shifted from register to register to the top of the stack, and then to the output port. The time it takes for a word to move from the input port to the output port is called “fall-through,”

and it is dependent on the depth of the FIFO buffer.

By contrast, FIFO RAM controllers implement a RAM-based buffer. In this scheme, pointers are incremented as each read or write occurs. Since data doesn't physically move, fall-through time is eliminated. What's more, external control of the RAM array buffer is possible by disabling both the Write Enable (WEN) and the Read Enable (REN) to impose three states on the address lines from the FIFO RAM controller to the RAMs.

By reducing the cost and space requirements of FIFO buffering, FIFO RAM controllers offer systems designers an efficient and cost-effective method to buffer large amounts of data. Using these devices, designers can minimize system bottlenecks in data paths and processing elements and can boost overall system performance. **CD**

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## PAL Devices, PROMs, FIFOs, and Multipliers Team up to Implement Single-Board High-Performance Audio Spectrum Analyzer

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This application note illustrates a high-performance audio spectrum analyzer. This circuit can analyze high fidelity audio signals with a resolution of 20 Hz and an input bandwidth of 20 kHz. It is useful in production test, performance evaluation, or adjustment of high-fidelity audio equipment. The analyzer provides a sweep generator output for rapid analysis of audio filter frequency response.

The design techniques used to implement the analyzer are quite general, and can be applied to a wide variety of DSP tasks. An

understanding of the approach used will suggest solutions to a number of DSP problems. The architecture chosen for the spectrum analyzer is controlled by a microprogram stored in PROM. Many other applications can be accommodated by changing the microprogram. The high performance of this architecture provides an attractive price/performance alternative to other DSP approaches.

# PAL Devices, PROMs, FIFOs, and Multipliers Team up to Implement Single-Board High-Performance Audio Spectrum Analyzer

AN-100

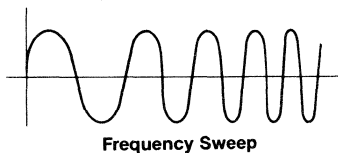
## Introduction

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## Spectrum Analyzer Functions

The spectrum analyzer requires many of the functions commonly used in DSP. Figure 1 shows the analyzer functions. An input signal is mixed with a swept audio sine wave oscillator (below).



The frequency sweep acts as a sampler, starting from DC and increasing to its maximum frequency.

Mixing is accomplished by multiplying the input signal by the sine wave. From basic trigonometry:

$$\cos w_1 t \times \cos w_2 t = 1/2 \cos (w_1 + w_2)t + 1/2 \cos (w_1 - w_2)t \quad (1)$$

The mixing process generates two new sinewaves whose frequencies are the sum and difference of the input sinewave frequencies. When the sinewave oscillator matches the frequency of an input signal component, a DC term is generated in proportion to the amplitude of that component:

$$\cos w_1 t \times \cos w_1 t = \cos^2 w_1 t = 1 + 2 \cos w_1 t$$

The DC term is extracted by a narrow lowpass filter. Due to the finite bandwidth of this lowpass filter, mixer output signals whose frequencies fall within the filter passband also appear at the filter output. As a result, the analyzer output will represent the energy contained in a range of frequencies, from the sine-wave frequency minus the filter cutoff frequency, to the sine-wave frequency plus the filter cutoff frequency. The effective bandwidth of the analyzer is twice the lowpass filter bandwidth.

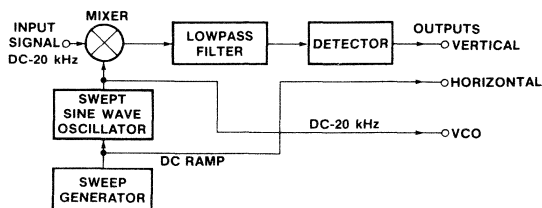


Figure 1. Spectrum Analyzer Functions

A detector converts the lowpass filter output to a DC voltage representing the total energy in the filter passband. If this DC voltage is plotted on a vertical axis with the sine wave oscillator frequency (represented by the sweep voltage) controlling the horizontal axis, a spectrum of the input signal results.

Other mixing schemes can be used to extract the spectrum. However, this "direct conversion" approach has two significant advantages. As shown in Figure 2, the swept oscillator output can be used to plot the frequency response of an audio filter. Other schemes require additional mixing to achieve the same results.

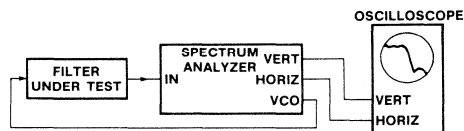


Figure 2. Filter Test Mode Setup

The direct conversion scheme confines the frequencies of all signals following the mixer to the lowpass filter bandwidth. Limiting the signal bandwidth has great benefit when the analyzer is implemented digitally. This benefit can be better understood with a brief review of DSP theory.

## Digital Signal Processing Theory Review

Digital signal processing is accomplished by first converting the continuous analog input signal to a series of digital numbers. The digital numbers are then manipulated to perform the required signal processing. The processed digital numbers are then converted back to a continuous analog signal, completing the processing. The functions required for DSP are shown in Figure 3.

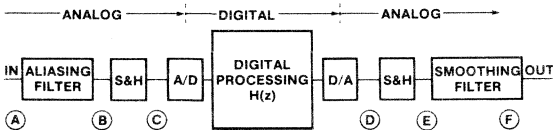


Figure 3. DSP Functions

### Sampling

Representing a continuous input signal would require an infinite array of digital numbers. A finite collection of digital numbers can be obtained by considering the signal amplitude at discrete, periodic points in time. This process is called *sampling*, and is equivalent to multiplying the input signal by a periodic train of impulses of unit amplitude. The *sampling theorem* states that the input signal can be reconstructed without distortion if the input is bandlimited to contain no frequency components greater than half the sampling frequency. The sampling theorem means that the discrete samples completely represent the input signal, as long as the bandwidth constraint is met.

### Aliasing

What is really happening during the sampling process? Consider the Fourier series representation of a periodic unit impulse train. It can be shown that:

$$f(t) = \sum_{k=-\infty}^{k=\infty} \cos(2\pi k f_s t), \quad k = 0, 1, 2, 3, \dots \quad (2)$$

where  $f_s = \frac{1}{\text{sample period}}$

The periodic impulse train is equivalent to a series of sinusoids consisting of all harmonics of the sampling frequency, including

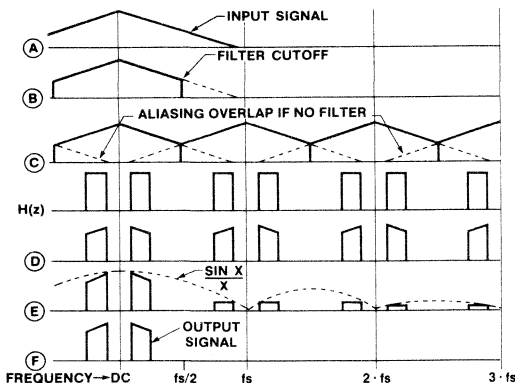


Figure 4. Aliasing Spectra of Figure 3 DSP Functions

a DC term. Recalling Eq. (1) all possible sum and difference frequencies will be generated when the impulse train and the input signal are multiplied. This process is shown graphically in Figure 4. Observe that if the input contains frequencies greater than half the sampling frequency, the spectra in Figure 4 will overlap. This overlap phenomenon is known as *aliasing distortion*, and introduces noise in the signal.

Another consequence of the sampling process is that high-frequency signal components near a harmonic of the sampling frequency will be mixed to produce new signal components near DC. These new components have frequencies within the desired signal passband, but are really "alias" high-frequency components. The phenomenon is called *aliasing*.

To eliminate the undesirable effects of aliasing, a continuous analog lowpass filter is placed before the sampler. This *aliasing filter* removes frequency components beyond the  $f_s/2$  limit.

### Quantizing

The input samples are converted to a series of digital numbers by an analog-to-digital (A/D) converter. The A/D converter operates by *quantizing* the continuous sample amplitude into a finite number of amplitude ranges, and then assigning a digital number to represent the quantized amplitude value. As might be expected, this process introduces noise in the signal, known as *quantization distortion*. The quantization distortion is in the form of a "white" or broadband random noise, whose RMS amplitude is:

$$\sigma^2 = \frac{1}{12} 2^{-2b} \quad (3)$$

where  $b$  is the number of bits in the output digital word, excluding the sign bit

The effect of aliasing on quantization noise is to alias high frequency noise components to the DC to  $f_s/2$  range. The resulting noise spectral density is equivalent to a white noise of amplitude  $\sigma^2$ , bandlimited to  $f_s/2$ .

### Dynamic Range

The A/D output contains a finite number of bits. *Dynamic range* is defined as the ratio of the maximum-to-minimum signal amplitude that can be represented by the digital numbers. Dynamic range is determined by the number of bits in the digital numbers, and by the noise "floor."

For a digital number containing  $b$  bits plus a sign bit, the dynamic range would be:

$$\text{Dynamic range (dB)} = 10 \log_{10} 2^{2b} \quad (4)$$

The noise floor is the sum of all noise components that can appear at the DSP output. The primary noise factors are quantization noise and limit cycle noise (to be discussed shortly). Digital filtering will affect the noise floor by eliminating components of the noise signal. For example, the quantization noise at the DSP output is:

$$N_Q \text{ (dB)} = 10 \log_{10} \left[ \frac{\sigma^2 \text{ BW}}{f_s/2} \right] \quad (5)$$

where  $\text{BW}$  is the net bandwidth of the digital filters

The noise components are uncorrelated, and are therefore combined by adding the power of each noise component. Remember that

$$\text{Power (absolute)} = \log_{10}^{-1} \left[ \text{Power (dB)} / 10 \right] \quad (6)$$

The resulting dynamic range is:

$$\text{Dynamic range (dB)} = 10 \log_{10} \frac{0.5}{\Sigma \text{ Noise Power}} \quad (7)$$

where 0.5 = the maximum mean-squared amplitude

The overall dynamic range is the lesser of the result given by Eq. (4) or Eq. (7). In a practical system, the width of the digital numbers can vary. The dynamic range is usually calculated for all critical points in a digital system, with the overall dynamic range being the worst case value.

### Digital Processing

The digital numbers from the A/D converter are manipulated to process the signal. Carrier generation, filtering, and nonlinear operations are performed by appropriate "number crunching".

Generation of sinusoidal carriers is easily accomplished using a linear ramp function (digital up/down counter) and converting the results to sinusoidal samples using ROM lookup tables. Alternately, recursive equations can produce the desired carriers.

Nonlinear operations on the digital numbers must be handled with care. Since aliasing is always present in the sampled domain, harmonics generated by nonlinear operations can alias to lower frequencies. The aliasing occurs "immediately," since it can be shown that performing a nonlinear operation in the sampled domain is equivalent to first performing the nonlinear operation on a continuous signal and then sampling the result without bandlimiting the sampler input.

The sampling rate can be changed to improve the efficiency of the digital processing. For example, discarding every other digital number would reduce the effective sampling rate by a factor of two. If the processing at the higher sample rate includes digital aliasing filters to remove components greater than half the lower sample rate, the requirements of the sampling theory are still met. The sampling rate can be increased by repeating digital sample values. This repetition is equivalent to a "sample and hold" operation, and modifies the signal spectrum by

$$F'(j\omega) = F(j\omega) \times \frac{\sin(\omega T/2)}{\omega T/2} \quad (8)$$

where  $\omega = 2\pi \times \text{freq}$   
 $T = \text{input (longer) sample period}$

The effects of changing the sampling rate are best determined by plotting the resulting aliasing spectra.

### Digital Filtering

Digital filtering is accomplished using multiplication, addition, and delay. For example, consider the biquadratic filter section in Figure 5. If  $z^{-1}$  is defined to be a unit sample period delay operator, then the input-to-output transfer function of the biquadratic section is:

$$H(z) = \frac{1 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \quad (9)$$

The biquadratic sections can be cascaded to implement higher-order filters.

The Laplace transform of a unit delay is  $e^{-sT}$ , where  $T$  is the delay period. Remember that  $z^{-1}$  represents an inverse operator, so that  $z \times z^{-1} = 1$ . Thus,

$$z = e^{sT}, \text{ where } s = \alpha + j\omega \quad (10)$$

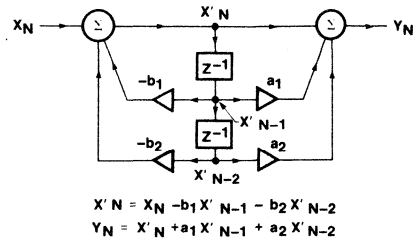


Figure 5. Digital Biquadratic Filter Section

Digital filter poles and zeroes (in the z-plane) can be mapped into the s-plane to determine the equivalent analog filter function, and vice-versa. The digital filter section of Eq. (9) corresponds to an analog biquadratic filter section with,

$$H(s) = \frac{s^2 + \alpha_0 \omega_0 s + \omega_0^2}{s^2 + \alpha_1 \omega_1 s + \omega_1^2} \quad (11)$$

However, the periodic nature of the  $e^{sT}$  function causes the digital filter passband to repeat periodically. The effect is the same as aliasing. The analog filter response is mixed with the sampling frequency harmonics to generate the true digital filter response.

### Designing Digital Filters

How does one go about designing a digital filter? One approach is to perform a least mean squared error optimization using a computer. The desired function is specified, and the computer adjusts the  $a_n$  and  $b_n$  values until the desired response is achieved.

A second approach is to design an equivalent analog filter and then convert that design to a digital filter. This approach has great merit, since analog filter design theory is well developed. However, the digital passband will be distorted if the analog equivalent filter has significant response to frequencies greater than  $f_s/2$ . The aliased passbands overlap at that point.

To circumvent this problem, the analog filter function can be modified to compensate for the aliasing effects. The analog transfer response is modified using several transforms to compensate for aliasing. Unfortunately, the nature of the s-plane to z-plane mapping is such that no transform can compensate for all aliasing effects without introducing other forms of distortion.

The *standard (or impulse invariant) z-transform* represents a direct mapping to the z-plane. No frequency, amplitude, or phase distortion is introduced, but aliasing effects are not compensated. This transform should be used when the analog filter has negligible response to frequencies greater than  $f_2/2$ .

The *bilinear z-transform* preserves the filter amplitude response in the presence of aliasing. However, the bilinear transform introduces a distortion or *warping* of the frequency axis. As a result, only the filter cutoff frequency can be accurately transformed, using a *pre-warping* technique. Frequencies within the filter passband remain warped, introducing phase distortion in the digital filter response. The bilinear transform is used when the filter amplitude response is more critical than the phase response.



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The *matched z-transform* preserves the filter phase response at the expense of amplitude response distortion. However, this amplitude distortion, unlike the aliasing distortion, can be corrected by placing additional zeroes in the transfer function. The matched transform is used when the filter phase response is critical, and either the amplitude response is not critical or the additional compensation zeroes can be accommodated. Performing the transforms by hand is quite tedious. Fortunately, computer programs are widely available which handle the complete filter synthesis procedure, including z-transforms and pre-warping.

### Limit Cycle Noise

An effect of using digital numbers with a finite number of bits is the generation of quantization noise. When implementing digital filters, the quantization noise introduces oscillations that are analogous to ringing in analog filters. These oscillations are called *limit cycles*. The limit cycle generates a noise which peaks at frequencies corresponding to the filter pole frequencies. The noise power is roughly proportional to pole Q. Limit cycle noise for a second order filter section of Equation (11) is given by:

$$N_L \text{ (dB)} = 10 \log_{10} \left( \frac{2}{12} 2^{-2b} \frac{1+r^2}{1-r^2} \frac{1}{r^4 + 1 - 2r^2 \cos 2w} \right) \quad (12)$$

where  $b$  = number of digital number bits (excluding sign bit)  
 pole freq. =  $w_1$   
 pole  $Q = 1/r_1$

$$w = 2\pi \frac{\text{pole freq.}}{f_s} \quad r = \exp\left(\frac{-w}{2 \cdot \text{pole } Q}\right)$$

The limit cycle noise must be calculated for each complex pole pair, and adjusted to reflect the response of subsequent filter stages to the limit cycle frequency. Computer programs can calculate limit cycle noise power, including all of these considerations.

### Output Signal Reconstruction

Once manipulation of the digital sample numbers is complete, the resulting digital numbers must be converted back to a

continuous analog signal. Referring back to Fig. 3, a digital-to-analog (D/A) converter transforms the digital numbers to a series of analog output pulses.

A sample-and-hold (S&H) circuit eliminates transients that are introduced during the D/A conversion process. The spectrum of the S&H output is modified as follows:

$$\text{S\&H } F'(jw) = F(jw) \frac{t}{T} \frac{\sin(wt/2)}{wt/2}$$

where  $t$  = hold time     $T$  = sample period

An output smoothing filter completes the reconstruction by removing all components with frequencies greater than  $f_s/2$ . The smoothing filter is often optional, depending on the importance of removing the high-frequency output components.

The spectral effects of reconstruction are shown in Figure 4.

### Implementing the Spectrum Analyzer

The architecture used for the spectrum analyzer is shown in Fig. 6. Input signals are digitized and buffered with FIFOs before interface with a common 16-bit data bus. The 16-bit arithmetic unit (AU) provides multiply and accumulate operations. A 16-bit wide RAM stores intermediate results. A 16-bit temporary register facilitates  $z^{-1}$  delays and data movement. Outputs are provided using a D/A converter and S&H circuits.

The VCO output is buffered using FIFOs to provide a uniform high-speed sample rate. The VCO output is 12 bits wide, providing a signal-to-quantization noise ratio of 91 dB, using Equations (5) and (7). The calculation assumes a 500-Hz bandwidth. A smoothing filter at the VCO output is not necessary. The filter test configuration of Figure 2 allows the input aliasing filter to remove the effects of VCO high-frequency components, as long as the filter under test is a linear analog circuit.

The vertical and horizontal outputs are intended to interface an oscilloscope or X-Y plotter. The sampling of these outputs can be non-uniform, as long as the outputs track each other. The elastic storage at the input and VCO interfaces permits arbitrary non-uniform processing of the analyzer functions.

The 16-bit resolution of the internal data word provides 90-dB dynamic range according to Equation (4), or 115-dB dynamic range according to Equations (5) and (7), assuming 500-Hz bandwidth and no limit cycle noise and aliasing.

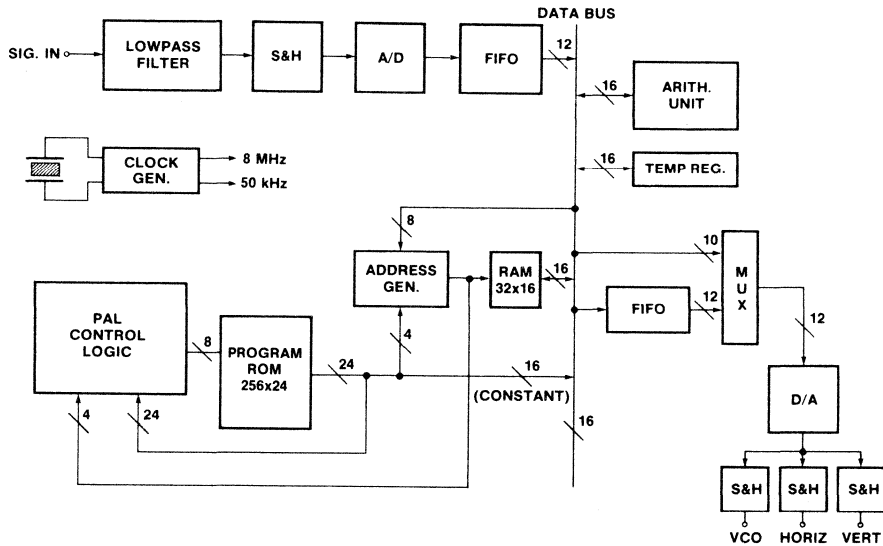


Figure 6. Analyzer Architecture

Microprogram control was selected for the analyzer. PAL devices can efficiently implement sequential state machines. It is possible to encode all control information in PAL devices, but only three packages would be saved (one PROM and two buffers). Distributing the control among several PAL devices would reduce flexibility and make corrections very difficult. The few extra packages required for microprogram control provide an extremely flexible architecture and greatly simplify the PAL device functions.

With the theoretical background and architecture in mind, the spectrum analyzer functions can be defined in detail. The objective is to realize a circuit capable of high-resolution analysis of audio signals in the DC to 20-kHz range. Selectable bandwidth and linear/logarithmic output display are highly desirable. Detailed functions are shown in Figure 7.

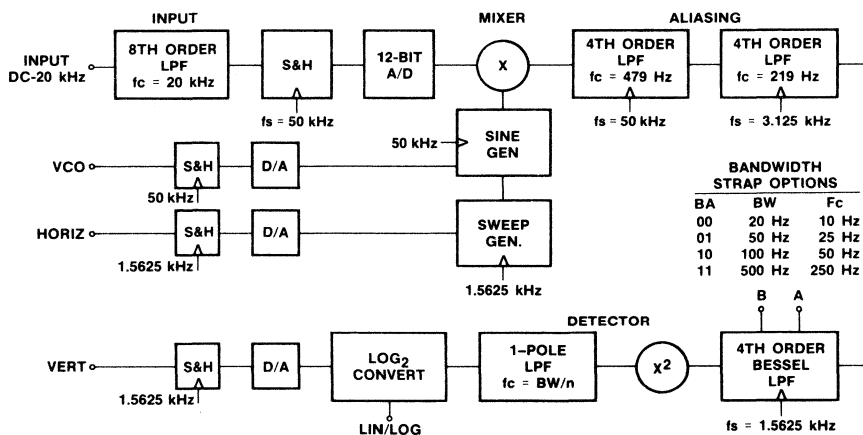


Figure 7. Detailed Functional Diagram

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### Input Aliasing Filter

An analog lowpass filter removes high-frequency components from the input signals. With a sample frequency of 50 kHz and a maximum input frequency of 20 kHz, the lowest aliasing frequency is  $(50-20) = 30$  kHz.

An eighth-order Chebyshev filter with 0.1-dB passband ripple will provide 44 dB of attenuation at 30 kHz, and 86 dB attenuation at 50 kHz. It is desirable to provide at least 60-dB overall dynamic range for high-performance analysis. To eliminate spurious responses above the -60-dB "floor," the input signal should have all components above 30 kHz suppressed by at least  $(60-44) = 16$  dB. Most input signals will meet this requirement. If not, additional filtering must be provided.

### S&H and A/D Converter

The input S&H maintains a constant sampled signal level while the A/D conversion is in progress. No  $\sin X/X$  correction is made for this S&H since the net effect of the S&H plus A/D action is an impulse sample at the start of the "hold" period.

The A/D conversion time should be less than 16  $\mu$ s. The A/D converter output digital number should "saturate" when the input signal exceeds the maximum level. The digital numbers should be in inverted two's complement form. The S&H acquisition time should be less than 4  $\mu$ s.

For a full 60-dB overall dynamic range, a 12-bit A/D is required.

### Mixer

The mixer multiplies the A/D output by the swept sinuswave oscillator value. The multiplication produces sum and difference frequencies, according to equation (1).

Two's complement fractional arithmetic is used throughout the analyzer. Multiplication cannot overflow, since all numbers are less than 1 in magnitude.

### Swept Sinusoidal Oscillator (VCO)

A precision swept sinusoid from DC to 20 kHz must be generated to mix with the input signal. A technique particularly well suited to this application is solving the two equations:

$$\sin(x+y) = \sin x \cos y + \cos x \sin y \quad (13)$$

$$\cos(x+y) = \cos x \cos y - \sin x \sin y \quad (14)$$

These two trigonometric identities generate a new  $\sin$  and  $\cos$  value with  $y$  representing the phase shift per sample period. The technique is a "CORDIC" algorithm, based on coordinate rotation. Exact results are produced, but truncation and round-off errors due to the finite digital word length can cause a slow change or "drift" of carrier amplitude. Fortunately, the swept sinusoid is periodically reset in the spectrum analyzer, arresting this amplitude drift.

The VCO frequency is swept by varying the value of  $y$ . However, since equations (13) and (14) require  $\sin y$  and  $\cos y$ , an identical CORDIC algorithm is used to obtain these values. To sweep the VCO, then,  $\sin \Delta$  and  $\cos \Delta$  are placed in RAM, selected by the bandwidth setting. These are two fixed numbers originally stored in PROM, and represent the frequency shift per sample time. Equations (13) and (14) are then applied to calculate  $\sin y$  and  $\cos y$ , which represent the desired phase shift per sample time. Equations (13) and (14) are executed again to generate the actual sinusoidal output.

The calculation of  $\sin y$  and  $\cos y$  can take place at a reduced sample rate to save processing time. Only the last execution of equations (13) and (14) must be performed at the full 50-kHz sample rate.

A linear ramp is generated to provide horizontal drive for an oscilloscope or X-Y plotter. The ramp is incremented each time the  $\sin y$  and  $\cos y$  values are updated, tracking the VCO sweep. When the ramp value overflows, the analyzer sweep cycle is re-initialized.

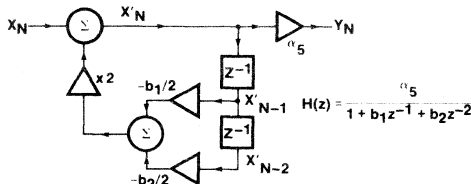


Figure 8. All-Pole Digital Filter Section

### Digital Filters

Fig. 8 shows the implementation of the all-pole digital filter sections. Because of the low pole Q values in all filters, the second order sections can be simply cascaded to implement high-order filters. Fig. 8 shows a technique for handling coefficients greater than 1 with fractional number representation.

Scaling must be performed to ensure maximum dynamic range. Filter sections with high-Q poles will show peaking of signals near the pole frequencies. The input to such sections must be scaled down to prevent overflow of the arithmetic. For a second-order all-pole section, this peaking factor is exactly the Q of the poles. Thus, when a given second-order section has a pole Q of 2, the input signal to that section must be multiplied by 0.5 to prevent overflow. When the Q is less than or equal to 1, no scaling is performed.

Saturation arithmetic is not provided in this architecture. Careful scaling eliminates the need for saturation arithmetic, since the A/D will saturate at a precisely known value.

### Aliasing Filters

Two 4th-order Chebyshev filters permit reduction of the sample rate following the mixer. Each filter provides 0.3 dB passband ripple and at least 68 dB attenuation of aliasing components. The slightly high passband ripple is acceptable, since subsequent filters will dominate the composite passband shape.

The first filter permits a sample rate reduction factor of 16. It is designed with a passband cutoff frequency of 479 Hz and a sample rate of 50 kHz. Eq. (12) predicts the limit cycle noise for this filter to be -58 dB.

The second filter permits a second sample rate reduction factor of two. Its cutoff frequency is 219 Hz, with a sample rate of 3.125 kHz. Equation (12) predicts the limit cycle noise for this filter to be -83 dB. This filter also provides an additional 14-dB attenuation of the limit cycle noise generated in the first aliasing filter, reducing the limit cycle noise from the first filter to -72 dB.

These two filters permit an overall  $f_s$  reduction factor of 32 before processing the Bessel filter, detector, and linear-to-log<sub>2</sub> functions. This results in a very substantial throughput improvement. Net execution time is determined by the time to execute a given function multiplied by the sample rate for that function. Thus 32 instructions at the reduced rate will increase the net execution time by an amount equivalent to only 1 instruction at the full sample rate.

Fig. 9 shows the aliasing spectra of the sample rate reduction process.

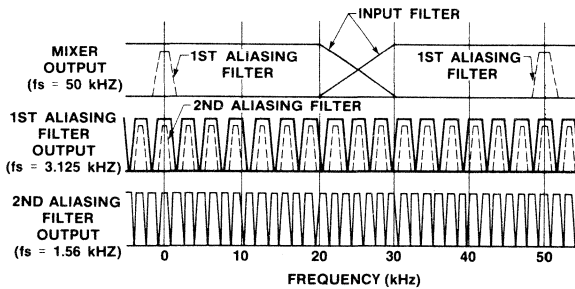


Figure 9. Aliasing Spectra for  $f_s$  Reduction

### Lowpass Filter

A 4th-order Bessel lowpass filter determines the overall bandwidth of the analyzer. The overall bandwidth is twice the bandwidth of this filter. Overall bandwidths of 20, 50, 100 or 500 Hz are provided by loading the proper set of filter coefficients into RAM when the bandwidth is selected.

The Bessel filter provides an optimal transient response for the analyzer. Good transient response is important, especially at narrow bandwidths, since the spectral peaks are swept with respect to the filter passband. The net effect is similar to pulsing the filter input. Because the phase response is critical, the matched-z transform is used to convert the analog Bessel design to the z-domain.

The second aliasing filter provides 3 dB of attenuation at 250 Hz. When cascaded with the Bessel filter, which also provides 3 dB attenuation at 250 Hz in the 500 Hz bandwidth mode, the response at this bandwidth is modified. However, since the overall bandwidth is relatively broad, good transient response is still achieved. Cascading these two filters provides a "transitional" filter with a Bessel response at low attenuation and a Chebyshev response at high attenuation. At bandwidths less than 500 Hz, the combination produces an optimal tradeoff between transient response and resolution.

Analysis of Equation (12) reveals that limit cycle noise increases exponentially as the pole frequency is reduced. Operating the lowpass filter at the lowest possible sampling frequency (1.5625 kHz) minimizes limit cycle noise, in addition to improving throughput. Limit cycle noise for the lowpass filter will be -95 dB

at the 500-Hz bandwidth, increasing to -67 dB at the 20-Hz bandwidth.

### Detector

A square-law detector provides a DC signal corresponding to the energy at the lowpass filter output. From trigonometry:

$$(A \cos wt)^2 = \frac{A^2}{2} (1 + \cos 2wt) \quad (15)$$

The detector output contains the desired DC term and a single undesired term at frequency  $2w$ . If the square law is ideal (easy in the digital domain), no additional terms are produced. The elimination of harmonics ensures the accuracy of the detector with  $f_s/32 = 1.5625$  kHz. The highest component is always less than  $f_s/64$  with a 250 Hz maximum lowpass filter cutoff frequency. However,  $2w$  can be anywhere from DC to 500 Hz as the VCO sweeps past the spectral component.

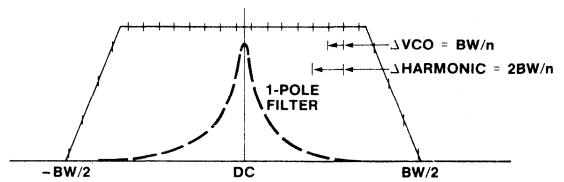


Figure 10. Detector Sweep Filtering

Fig. 10 illustrates a technique to render the effects of the  $2w$  terms negligible. The analyzer passband is divided into  $n$  equal intervals. The VCO sweep rate is controlled so that the VCO sweeps  $BW/n$  per  $f_s/32$  interval. The detector is followed by a single-pole lowpass filter with a 3 dB frequency of  $BW/n$ . As the VCO sweeps a component through the passband, the DC term is present in all  $n$  intervals, but the  $2w$  term can affect only one interval. The worst-case DC error is  $1/n$  for an ideal cutoff, and is multiplied by  $(2^0 + 2^{-1} + 2^{-3} + 2^{-4} + 2^{-5} + 2^{-5.5} + 2^{-6} + 2^{-6.5} + 2^{-7} + 2^{-7.25} + \dots) = 1.85$  due to the finite 6 dB/octave rolloff of the single-pole filter. Further analysis reveals that:

$$n = \frac{1.85}{10^{e/10} - 1} \quad (16)$$

where  $e$  represents the resulting error in dB. For  $e = 0.1$  dB,  $n = 80$ .

In the filter test mode, the signal frequency and VCO frequency are the same, forcing  $w = 0$ . The detector has no error in this mode, but has a 3 dB gain due to the second DC term.

The detector output represents signal energy. Each bit in the detector output word thus represents only 3 dB, and 21 bits are required to reflect a 60 dB dynamic range. Double precision arithmetic is required for the detector output and the single-pole filter. The 67C7560 multiplier will handle double precision calculations with a time penalty. Fortunately, the calculations to be performed are simple and the operations take place at the minimum sample rate, reducing the impact on throughput.

### Linear-to-Log Conversion

The architecture of Figure 6 is customized to provide an efficient algorithm for linear-to-logarithmic output conversion. The RAM address generator monitors the 8 MSBs of the data bus, and can provide a number indicating the MSB position of a positive

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number. This output is used to retrieve a lookup table value. This value is used to scale the data word to quickly left-justify the MSB. A second 4-point lookup table is then used to improve the accuracy of the resulting  $\log_2$  conversion. A  $\log_2$  conversion is adequate, since:

$$\log_{10} x = \frac{\log_2 x}{\log_2 10} \quad (17)$$

Equation (17) demonstrates that the output can be displayed in decibels by setting the oscilloscope or X-Y plotter Y-axis gain to the proper value.

Two lookup tables provide .027 dB accuracy for output values from 0 to -45 dB, and 3 dB accuracy from -45 to -84 dB. The logarithmic accuracy is limited by the 10-bit output word length to the D/A. This output can represent 0 to -84 dB in .082 dB increments. The accuracy of the 4-point lookup is therefore sufficient.

The logarithmic conversion procedure is as follows:

- 1) If the MSB of the data word is not among the 8 MSBs into the address generator, multiply the word by  $2^7 = 128$ , and increment the output number by 7. Repeat until the data word is greater than  $2^{-7}$ , but no more than three times. Set a flag if this step is executed more than once.

- 2) Look up the appropriate scale factor, from  $2^0$  to  $2^6$ . Add  $\log_2$  of the scale factor to the output word. The conversion is now accurate to 3 dB.
- 3) If the flag was not set during step 1, multiply the data word by the scale factor to left-justify the MSB position.
- 4) If the flag was not set during step 1, retrieve an intercept and slope value from the 8-word lookup table (four pairs available). Perform a linear interpolation using:

$$x' = a \times i + b$$

where a is the slope value (18)  
b is the intercept value

The conversion is now accurate to .027 dB.

- 5) Scale the result to provide 84-dB output range with a 10-bit word.
- 6) Subtract  $2^{-1}$  from the output to convert it to two's complement form for the D/A.

The calculations are double precision for steps 1, 2, and 3, and single precision thereafter. The conversion sequence can be bypassed using a strap option to provide a linear amplitude output from 0 to -30 dB.

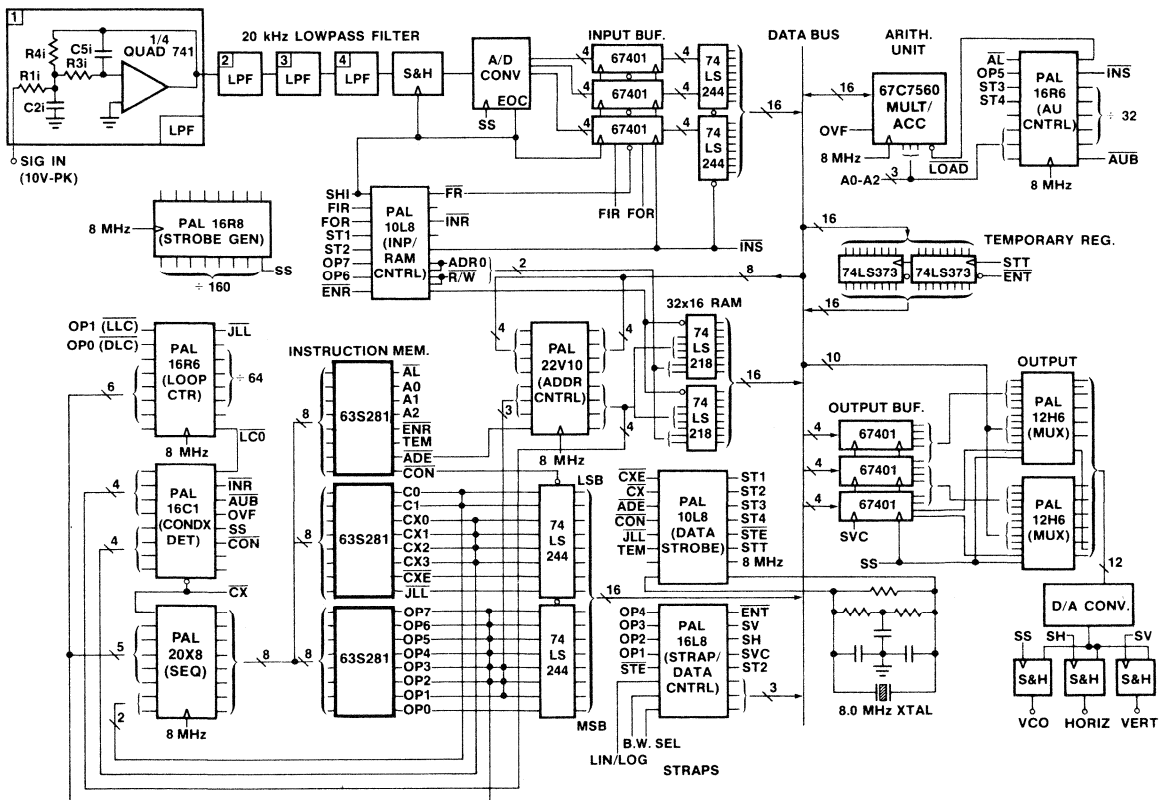


Figure 11. Simplified Schematic Hi-Fi Audio Spectrum Analyzer

### Control Logic

Figure 11 shows a simplified schematic of the analyzer. All critical components are shown. Bypass capacitors and some component input connections are omitted for clarity.

The microprogram is stored in three 63S281 PROMs. The microcode word formats are shown in Figure 12. A wide, highly-parallel instruction word ensures maximum flexibility and program efficiency.

Eight PAL devices interpret the instruction word and control the analyzer. Two additional PAL devices generate a 50-kHz strobe from the 8-MHz master clock, and implement the output D/A multiplexer. The control PAL devices function as follows:

**Sequencer:** A PAL20X8 implements an 8-bit instruction sequencer. The sequencer performs the following operations:

C1	C0	CX	Operation
0	0	X	Increment by 1 (execute next instruction)
0	1	0	Increment by 2 (skip next instruction)
1	0	0	Jump to address
1	1	0	No increment (repeat current instruction)

The  $\overline{CX}$  input conditions the sequencer. Conditional branches or skip operations can be implemented. The sequencer will increment if the conditional requirement is not met.

**Condition detector:** A PAL16C1 monitors up to twelve status flags, and generates CX. The microcode word includes a 4-bit

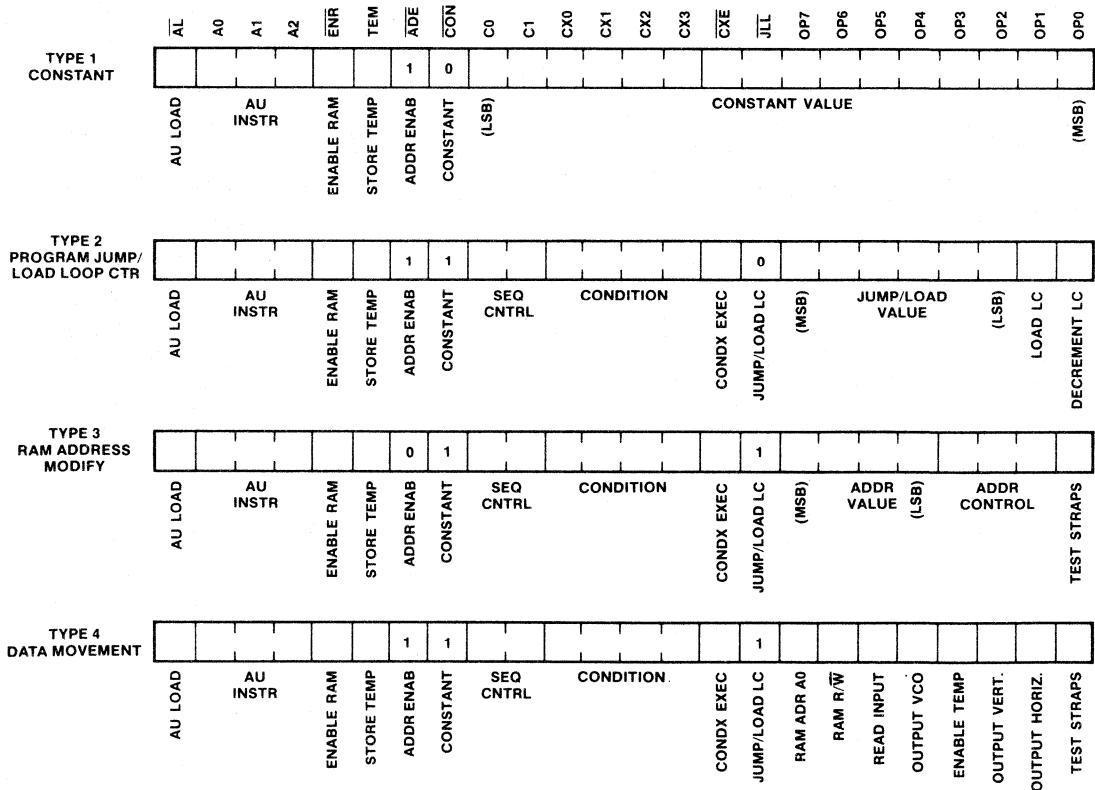


Figure 12. Microinstruction Word Formats

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condition word, CX0 through CX3.  $\overline{CX}$  will be zero under the following conditions:

CX3	CX2	CX1	CX0	Condition for $\overline{CX} = 0$
0	0	0	0	Always (unconditional operation)
0	0	0	1	Sample strobe (SS) = 1
0	0	1	0	AU overflow (OVF) = 1
0	0	1	1	AU busy (AUB) = 1
0	1	0	0	Input sample ready (INR) = 0
0	1	0	1	Loop counter timeout (LLC) = 0
0	1	1	0	LLC = 1
0	1	1	1	Address control (AC3-AC0) = 0
1	0	0	0	AC0 = 0
1	0	0	1	AC0 = 1
1	0	1	0	AC1 = 0
1	0	1	1	AC1 = 1
1	1	0	0	AC2 = 0
1	1	0	1	AC2 = 1
1	1	1	0	AC3 = 0
1	1	1	1	AC3 = 1

The assignment is made using the flexible PAL device coding, and is optimized for the analyzer. The user can select a different set of conditions by reprogramming the PAL device.

When the microcode represents a constant (Type 1 microinstruction — see Figure 12) the  $\overline{CON}$  input forces  $\overline{CX} = 1$  to suppress conditional operations.  $\overline{CX}$  is also used to suppress certain strobes in the analyzer, providing conditional arithmetic operations.

**Loop counter:** A PAL16R6 implements a 6-bit programmable down counter. This counter controls iteration loops and provides a timeout signal to the condition detector. The counter is preset via a Type 2 microinstruction, and can be decremented by other Type 2 microinstructions. The counter will halt when zero count is reached. Up to 64 iterations can be accommodated with minimal overhead.

**Address control:** A PAL22V10 provides indexed addressing for the 32x16 RAM, and analyzes the eight MSBs of the data bus for conditional operations. If D15 represents the data bus sign bit, then OP1-OP3 will provide the following functions:

OP3	OP2	OP1	AC3-AC0	Output Function
0	0	0		Clear (0000)
0	0	1		Increment
0	1	0		Decrement
0	1	1		Preset to D15-D12 (Sign + 3 MSB)
1	0	0		Preset to D14-D11 (4 MSB)
1	0	1		Preset to D11-D8 (Address load)
1	1	0		MSB position
1	1	1		No change

The  $\overline{ADE}$  input enables a change in the address word. The address word will not change if  $\overline{ADE} = 1$ .

The MSB position function indicates the position of the MSB for positive numbers. AC3 represents sign bit D15. This output should be zero. AC2-AC1 represent the position of the first 1 following the sign bit. Code 0000 indicates that D15-D8 are all 0.

**Input/RAM control:** Miscellaneous FIFO input and RAM control is provided by a PAL 10L8. The 67401 FIFO includes input ready (FIR) and output ready (FOR) signals, which are latched using the input/output shift clocks to generate two flags. The first flag ( $\overline{FR}$ ) resets the FIFO when input ready (latched) goes low, indicating the FIFO capacity is exhausted. The latched output ready signal flag represents input sample ready (INR). The INR

flag is used as a sequencer condition to synchronize wait loops. Use of the FR and INR flags maintains proper fill of the FIFO.

The RAM address LSB (A0) and read-write line ( $R/\overline{W}$ ) are decoded and latched. These signals are provided directly by Type IV microinstructions.

Notice that a clocked register function requires two PAL combinatorial outputs per bit, while a transparent latch function requires only one PAL output per bit.

**Arithmetic unit control:** The variety of functions listed in Table 3 indicate the utility of the arithmetic unit (AU). A PAL16R6 provides simplified control of the AU.

The PAL devices and AU load signal provide conditional arithmetic operations. Gating the load input will suppress the start of a new arithmetic operation. When  $\overline{CXE}$  is high, the operation is performed unconditionally. When  $\overline{CXE}$  is low, the operation is performed only if  $\overline{CX}$  is low. Combining conditional jumps and conditional AU operations provides a high degree of program flexibility.

The PAL device monitors the AU instructions and generates a busy signal ( $\overline{AUB}$ ). A counter in the PAL device keeps track of variable-length operations to provide the correct output for any instruction sequence. The  $\overline{AUB}$  signal conditions the sequencer to synchronize the microprogram to the AU operation. Microprogramming is simplified as a result.

The PAL device also gates the input FIFO shift out clock ( $\overline{INS}$ ) to eliminate transients while providing a full 125-ns pulse for proper FIFO operation.

**Data strobe generator:** A PAL10L8 provides a number of transient-free, gated strobes. These strobes provide control of the analyzer data flow. The PAL device interprets the microinstruction to determine the proper microinstruction type, and generates the strobes accordingly.

The PAL device also generates an 8-MHz buffered clock, as shown in Figure 11. The crystal oscillator circuit provides independent AC and DC feedback, permitting reliable operation with the PAL device.

**Strap/output sample control:** A PAL16L8 generates additional control strobes for the output sample-and-hold circuits.

The PAL device also provides a tristate buffer function, connecting control straps to the data bus for certain conditional jump operations. Two straps select the desired analyzer bandwidth/sweep rate, and the third strap selects linear or logarithmic output.

### Signal output

The VCO output must be sampled at precise intervals to avoid phase modulation effects. Three 67401 FIFOs buffer the VCO samples, which are generated during the 50-kHz input processing. A 12-bit D/A converter provides better than 91 dB signal-to-distortion ratio. The S&H circuit provides VCO outputs at precise 50-kHz intervals, and removes spikes that are generated in the D/A converter. All necessary control signals are generated by the strap/output data control PAL device.

The horizontal and vertical outputs normally drive an X-Y plotter or oscilloscope. There is no need to buffer these signals as long as the two outputs track each other. The D/A used for the VCO output is shared by adding two PAL12H6 chips programmed as multiplexers. Use of PAL devices requires fewer packages than a TTL multiplexer. Additional S&H circuits decode the multiplexed D/A output to separate the output signals.

### Microprogram

The architecture can implement a variety of DSP functions. A microprogram, stored in 63S281 PROMs, customizes the architecture to perform the spectrum analyzer tasks. The microinstruction formats were summarized in Figure 12. The algorithms to be implemented were discussed in the previous section. The step-by-step implementation of these algorithms is converted to a sequence of microinstructions to form the microprogram. The procedure is analogous to programming a microprocessor.

Operation of the microprogram is better understood by considering the allocation of the 74S218 RAM locations, shown in Figure 13. The microprogram consists of two parts. High-speed input processing provides the carrier generation, mixing, aliasing filter and lowpass filter functions. Figure 13a shows the RAM allocation during input processing. The input segment includes an efficient iteration loop, using the PAL device loop counter, to process the 50-kHz functions. The carrier frequency shift and lowpass filter functions are processed at the  $f_s/32$  reduced sample rate for maximum throughput efficiency.

The values of  $\sin \Delta$ ,  $\cos \Delta$ , and the Bessel filter coefficients depend on the analyzer bandwidth strap selection. These values are stored in a "table" area in Fig. 13, and can be easily changed. The fixed aliasing filter coefficients are stored as constants in the microprogram itself.

Once the input processing is complete, coefficients located in the table area can be changed. This area is re-used by the output program segment to hold the scale factors for the linear-to-log conversion routine. The detector functions are processed, and the logarithmic conversion is started with the RAM allocation of Figure 13(b). The table area is then reloaded with the interpolation coefficients (Figure 13(c)) to complete the logarithmic conversion. Shaded areas in Figure 13 provide temporary data and flag storage for the routines.

The microprogram samples the strap settings and loads the table area with the appropriate coefficients for input processing. The detector filter coefficient ( $b_1$ ) is also determined and loaded. The input processing is then repeated. This sequence repeats indefinitely. The coefficient loading technique makes efficient use of RAM capacity while eliminating elaborate jump sequences. All coefficient table updates are processed at the minimum sample rate for best efficiency.

The PAL device controllers simplify the microprogram. A PAL device provides hardware iteration loops. The AU controller eliminates wasteful "NO-OP" instructions otherwise required to allow completion of AU operations. The input control PAL device simplifies handshaking with the input logic. With the benefit of the PAL device controllers, the analyzer microprogram easily fits into the 256-instruction capacity of the PROMs.

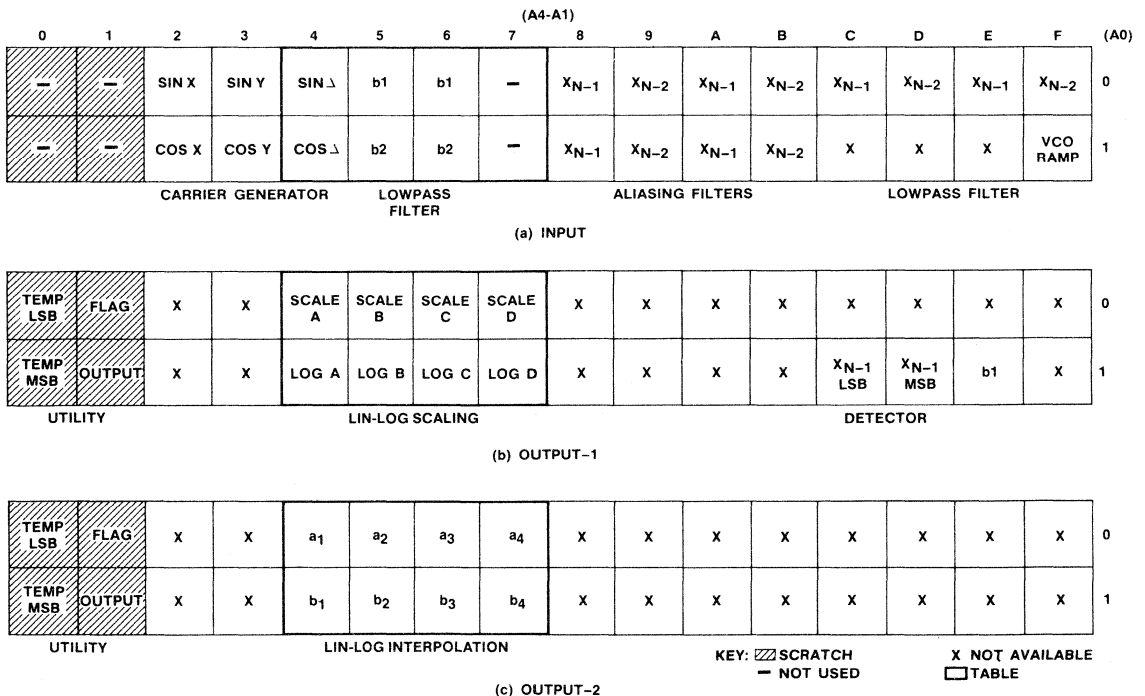


Figure 13. RAM Allocation



# Audio Spectrum Analyzer

TITLE AN-100 DSP Counter  
 PATTERN DSPCOUNT  
 REVISION 1  
 AUTHOR Marc Baker  
 COMPANY Monolithic Memories  
 DATE August 20, 1987

CHIP DSPCOUNT PAL20X8

CLK NC OP3 OP4 OP5 OP6 OP7 C0 C1 /CX NC GND  
 /OE NC A7 A6 A5 A4 A3 A2 A1 A0 /LOAD VCC

## EQUATIONS

```

LOAD = /C0* C1* CX ;FED BACK TO EQUATIONS

/A0 := /LOAD*/A0 ;HOLD/INCREMENT BY 2
      + /C0* C1* CX ;LOAD 0
      ++: /C0*/C1 ;INCREMENT BY 1

/A1 := /LOAD*/A1 ;HOLD
      + /C0* C1* CX ;LOAD 0
      ++: /C0*/C1* A0 ;INCREMENT BY 1
      + C0*/C1* CX*/A0 ;INCREMENT BY 2

/A2 := /LOAD*/A2 ;HOLD
      + /C0* C1* CX ;LOAD 0
      ++: /C0*/C1* A1* A0 ;INCREMENT BY 1
      + C0*/C1* CX* A1*/A0 ;INCREMENT BY 2

/A3 := /LOAD*/A3 ;HOLD
      + /C0* C1* CX*/OP3 ;LOAD
      ++: /C0*/C1* A2* A1* A0 ;INCREMENT BY 1
      + C0*/C1* CX* A2* A1*/A0 ;INCREMENT BY 2

/A4 := /LOAD*/A4 ;HOLD
      + /C0* C1* CX*/OP4 ;LOAD
      ++: /C0*/C1* A3* A2* A1* A0 ;INCREMENT BY 1
      + C0*/C1* CX* A3* A2* A1*/A0 ;INCREMENT BY 2

/A5 := /LOAD*/A5 ;HOLD
      + /C0* C1* CX*/OP5 ;LOAD
      ++: /C0*/C1* A4* A3* A2* A1* A0 ;INCREMENT BY 1
      + C0*/C1* CX* A4* A3* A2* A1*/A0 ;INCREMENT BY 2

/A6 := /LOAD*/A6 ;HOLD
      + /C0* C1* CX*/OP6 ;LOAD
      ++: /C0*/C1* A5* A4* A3* A2* A1* A0 ;INC BY 1
      + C0*/C1* CX* A5* A4* A3* A2* A1*/A0 ;INC BY 2

/A7 := /LOAD*/A7 ;HOLD
      + /C0* C1* CX*/OP7 ;LOAD
      ++: /C0*/C1* A6* A5* A4* A3* A2* A1* A0 ;INC BY 1
      + C0*/C1* CX* A6* A5* A4* A3* A2* A1*/A0 ;INC BY 2
  
```

SIMULATION

```

TRACE_ON CLK A7 A6 A5 A4 A3 A2 A1 A0      ;Trace CLK and outputs

SETF OE /C0 C1 CX /OP7 /OP6 /OP5 /OP4 /OP3
CLOCKF CLK                                ;Load all 0s
CHECK /A7 /A6 /A5 /A4 /A3 /A2 /A1 /A0

SETF C0 /C1
CLOCKF CLK                                ;Increment by 2
CHECK /A7 /A6 /A5 /A4 /A3 /A2 A1 /A0      ;to 2

CLOCKF CLK                                ;Increment by 2
CHECK /A7 /A6 /A5 /A4 /A3 A2 /A1 /A0      ;to 4

CLOCKF CLK                                ;Increment by 2
CHECK /A7 /A6 /A5 /A4 /A3 A2 A1 /A0      ;to 6

SETF /C0
CLOCKF CLK                                ;Increment by 1
CHECK /A7 /A6 /A5 /A4 /A3 A2 A1 A0        ;to 7

CLOCKF CLK                                ;Increment by 1
CHECK /A7 /A6 /A5 /A4 A3 /A2 /A1 /A0      ;to 8

SETF C0 C1
CLOCKF CLK                                ;Hold
CLOCKF CLK                                ;Hold
CHECK /A7 /A6 /A5 /A4 A3 /A2 /A1 /A0      ;to 8

TRACE_OFF

```

## Audio Spectrum Analyzer

---

TITLE AN-100 DSP Condition  
PATTERN DSPCOND  
REVISION 1  
AUTHOR Marc Baker  
COMPANY Monolithic Memories  
DATE August 20, 1987

CHIP DSPCOND PAL16C1

CX3 CX2 CX1 CX0 SS OVF AUB INR /LLC GND  
/CON AC0 AC1 AC2 /CX COMP\_CX AC3 NC NC VCC

### EQUATIONS

CX = /CX3\*/CX2\*/CX1\*/CX0\* CON  
+ /CX3\*/CX2\*/CX1\* CX0\* SS\* CON  
+ /CX3\*/CX2\* CX1\*/CX0\* OVF\* CON  
+ /CX3\*/CX2\* CX1\* CX0\* AUB\* CON  
+ /CX3\* CX2\*/CX1\*/CX0\*/INR\* CON  
+ /CX3\* CX2\*/CX1\* CX0\* LLC\* CON  
+ /CX3\* CX2\* CX1\*/CX0\*/LLC\* CON  
+ /CX3\* CX2\* CX1\* CX0\*/AC3\*/AC2\*/AC1\*/AC0\* CON  
+ CX3\*/CX2\*/CX1\*/CX0\*/AC0\* CON  
+ CX3\*/CX2\*/CX1\* CX0\* AC0\* CON  
+ CX3\*/CX2\* CX1\*/CX0\*/AC1\* CON  
+ CX3\*/CX2\* CX1\* CX0\* AC1\* CON  
+ CX3\* CX2\*/CX1\*/CX0\*/AC2\* CON  
+ CX3\* CX2\*/CX1\* CX0\* AC2\* CON  
+ CX3\* CX2\* CX1\*/CX0\*/AC3\* CON  
+ CX3\* CX2\* CX1\* CX0\* AC3\* CON

### SIMULATION

SETF /CON ;SET /CX HIGH  
CHECK /CX

SETF CON /CX3 /CX2 /CX1 /CX0 ;CX3-CX0=0 - SET /CX LOW  
CHECK CX

SETF CX0 SS ;CX3-CX0=1 - SET /CX LOW  
CHECK CX

SETF CX1 /CX0 OVF ;CX3-CX0=2 - SET /CX LOW  
CHECK CX

SETF CX0 AUB ;CX3-CX0=3 - SET /CX LOW  
CHECK CX

SETF CX2 /CX1 /CX0 /INR ;CX3-CX0=4 - SET /CX LOW  
CHECK CX

SETF CX0 LLC ;CX3-CX0=5 - SET /CX LOW  
CHECK CX

SETF CX1 /CX0 /LLC CHECK CX	;CX3-CX0=6 - SET /CX LOW
SETF CX0 /AC3 /AC2 /AC1 /AC0 CHECK CX	;CX3-CX0=7 - SET /CX LOW
SETF CX3 /CX2 /CX1 /CX0 CHECK CX	;CX3-CX0=8 - SET /CX LOW
SETF CX0 AC0 CHECK CX	;CX3-CX0=9 - SET /CX LOW
SETF CX1 /CX0 CHECK CX	;CX3-CX0=10 - SET /CX LOW
SETF CX0 AC1 CHECK CX	;CX3-CX0=11 - SET /CX LOW
SETF CX2 /CX1 /CX0 CHECK CX	;CX3-CX0=12 - SET /CX LOW
SETF CX0 AC2 CHECK CX	;CX3-CX0=13 - SET /CX LOW
SETF CX1 /CX0 CHECK CX	;CX3-CX0=14 - SET /CX LOW
SETF CX0 AC3 CHECK CX	;CX3-CX0=15 - SET /CX LOW

# Audio Spectrum Analyzer

TITLE AN-100 DSP Address Control  
PATTERN ADDCONT  
REVISION 1  
AUTHOR Marc Baker  
COMPANY Monolithic Memories  
DATE August 21, 1987

CHIP ADDCONT PAL22V10

CLK OP3 OP2 OP1 /ADE D15 D14 D13 D12 NC NC GND  
NC NC D11 D10 AC0 AC1 AC2 AC3 D9 D8 NC VCC  
GLOBAL

## EQUATIONS

```
AC0 := /OP3*/OP2* OP1*/AC0* ADE ;INC
      + /OP3* OP2*/OP1*/AC0* ADE ;DEC
      + /OP3* OP2* OP1* D12* ADE ;D12
      + OP3*/OP2*/OP1* D11* ADE ;D11
      + OP3*/OP2* OP1* D8 * ADE ;D8
      + OP3* OP2*/OP1* D14* ADE ;MSB EQUATIONS
      + OP3* OP2*/OP1*/D14*/D13* D12* ADE
      + OP3* OP2*/OP1*/D14*/D13*/D12*/D11* D10* ADE
      + OP3* OP2*/OP1*/D14*/D13*/D12*/D11*/D10*/D9*D8* ADE
      + OP3* OP2* OP1* AC0 ;HOLD
      + AC0*/ADE ;HOLD

AC1 := /OP3*/OP2* OP1* AC1*/AC0* ADE ;INC
      + /OP3*/OP2* OP1*/AC1* AC0* ADE ;INC
      + /OP3* OP2*/OP1* AC1* AC0* ADE ;DEC
      + /OP3* OP2*/OP1*/AC1*/AC0* ADE ;DEC
      + /OP3* OP2* OP1* D13* ADE ;D13
      + OP3*/OP2*/OP1* D12* ADE ;D12
      + OP3*/OP2* OP1* D9 * ADE ;D9
      + OP3* OP2*/OP1* D14* ADE ;MSB EQUATIONS
      + OP3* OP2*/OP1*/D14* D13* ADE
      + OP3* OP2*/OP1*/D14*/D13*/D12*/D11* D10* ADE
      + OP3* OP2*/OP1*/D14*/D13*/D12*/D11*/D10* D9* ADE
      + OP3* OP2* OP1* AC1 ;HOLD
      + AC1*/ADE ;HOLD
```

```

AC2 := /OP3*/OP2* OP1*/AC2* AC1* AC0* ADE ;INC
      + /OP3*/OP2* OP1* AC2*/AC1* ADE ;INC
      + /OP3*/OP2* OP1* AC2* /AC0* ADE ;INC
      + /OP3* OP2*/OP1*/AC2*/AC1*/AC0* ADE ;DEC
      + /OP3* OP2*/OP1* AC2* AC1* ADE ;DEC
      + /OP3* OP2*/OP1* AC2* AC0* ADE ;DEC
      + /OP3* OP2* OP1* D14* ADE ;D14
      + OP3*/OP2*/OP1* D13* ADE ;D13
      + OP3*/OP2* OP1* D10* ADE ;D10
      + OP3* OP2*/OP1* D14* ADE ;MSB EQUATIONS
      + OP3* OP2*/OP1* D13* ADE
      + OP3* OP2*/OP1* D12* ADE
      + OP3* OP2*/OP1* D11* ADE
      + OP3* OP2* OP1* AC2 ;HOLD
      + AC2*/ADE ;HOLD

AC3 := /OP3*/OP2* OP1*/AC3* AC2* AC1* AC0* ADE ;INC
      + /OP3*/OP2* OP1* AC3*/AC2* ADE ;INC
      + /OP3*/OP2* OP1* AC3* /AC1* ADE ;INC
      + /OP3*/OP2* OP1* AC3* /AC0* ADE ;INC
      + /OP3* OP2*/OP1*/AC3*/AC2*/AC1*/AC0* ADE ;DEC
      + /OP3* OP2*/OP1*/AC3* AC2* ADE ;DEC
      + /OP3* OP2* OP1*/AC3* AC1* ADE ;DEC
      + /OP3* OP2*/OP1*/AC3* AC0* ADE ;DEC
      + /OP3* OP2* OP1* D15* ADE ;D15
      + OP3*/OP2*/OP1* D14* ADE ;D14
      + OP3*/OP2* OP1* D11* ADE ;D11
      + OP3* OP2* OP1* AC3 ;HOLD
      + AC3*/ADE ;HOLD
  
```

SIMULATION

TRACE\_ON CLK AC3 AC2 AC1 AC0

```

SETF ADE /OP3 /OP2 /OP1
CLOCKF CLK ;CLEAR TO 0
CHECK /AC3 /AC2 /AC1 /AC0
  
```

```

SETF OP1
CLOCKF CLK ;INCREMENT TO 1
CHECK /AC3 /AC2 /AC1 AC0
  
```

```

CLOCKF CLK ;INCREMENT TO 2
CHECK /AC3 /AC2 AC1 /AC0
  
```

```

CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK ;INCREMENT TO 8
CHECK AC3 /AC2 /AC1 /AC0
  
```

## Audio Spectrum Analyzer

---

```
SETF OP2 /OP1
CLOCKF CLK ;DECREMENT TO 7
CHECK /AC3 AC2 AC1 AC0

CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK ;DECREMENT TO 3
CHECK /AC3 /AC2 AC1 AC0

SETF OP1 /D15 D14 /D13 D12 /D11
CLOCKF CLK ;SET TO D15-D12
CHECK /AC3 AC2 /AC1 AC0

SETF OP3 /OP2 /OP1
CLOCKF CLK ;SET TO D14-D11
CHECK AC3 /AC2 AC1 /AC0

SETF OP1 D10 /D9 D8
CLOCKF CLK ;SET TO D11-D8
CHECK /AC3 AC2 /AC1 AC0

SETF OP2 /OP1
CLOCKF CLK ;CHECK MSB
CHECK /AC3 AC2 AC1 AC0

SETF /D14
CLOCKF CLK ;CHECK MSB
CHECK /AC3 AC2 /AC1 AC0

SETF OP1
CLOCKF CLK ;HOLD
CHECK /AC3 AC2 /AC1 AC0

SETF /OP3 /OP2 /OP1 /ADE
CLOCKF CLK ;HOLD
CHECK /AC3 AC2 /AC1 AC0

TRACE_OFF
```

---





# First-In First-Out Memories: Operations and Applications

Zwie Amitai and Nusra Lodhi

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In many digital systems, high-speed transfers of data or instructions take place between sources and destinations that have different data rates. In other cases, the source and destination cannot operate simultaneously thereby needing some kind of data buffer at either source or destination. First-In First-Out (FIFO) memories are devices used to provide both data buffering

and data rate matching between source and destination in digital systems. A family of FIFO devices, available from AMD, covers a wide range of data rates as well as different applications such as high-speed data acquisition, and serial to/from parallel format conversions.

2

# First-In First-Out Memories: Operations and Applications

Zwie Amitai and Nusra Lodhi

## What's a FIFO?

### Definition

FIFO means First-In First-Out. In this case FIFO refers to a First-In First-Out, 2-port memory device. The data stored in a FIFO memory is provided at the output port in the same sequence that the data was written via the input port. Writing and reading data can be completely independent operations except when the FIFO is full or empty. The FIFO is empty and no more words can be read whenever the total number of words read since reset is equal to the total number of words written. The FIFO is full and no more words can be written whenever the total number of words written is equal to the number of words read plus the capacity of the FIFO.

### FIFO Operation

FIFO memories are used to assemble incoming data in a word serial buffer to be read out later in the order written, usually at a different rate. A simple mechanical analogy is the old fashioned coin dispenser used by the ice cream vendor or amusement park arcade vendor (Figure 1). Each coin tube has storage space for a number of coins, say sixty-four coins for example. Coins are dropped into each tube one at a time through a slot in the top of the tube. When a coin is entered, it falls to the top of the stack of coins already stored in the tube. When change is needed, the vendor pushes a lever near the bottom of the tube. This releases a single coin each time the lever is depressed and released. The coin dispenser is clearly a FIFO memory for coins because coins are released at the bottom of the tube in the same order they were entered at the top, but usually at a different rate.

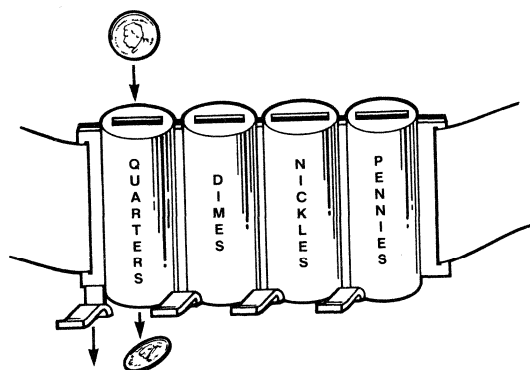


Figure 1. A FIFO Buffer for Coins

Each time a coin is removed from the bottom of the tube, the coin directly above it moves down to fill the vacant space. The same happens to each of the other coins in the stack. There is no restriction on loading and delivering coins asynchronously or simultaneously except for the empty and full conditions. If the tube is empty or if a coin has not yet fallen to the bottom of the tube, nothing will happen when the coin release lever is pressed. When the tube has sixty-four coins stored, it is not possible to stuff another coin into the tube. The operation of the 67401 FIFO is directly analogous to the coin changer except that the 67401 has four coin tubes that operate together rather than four independent tubes in the coin changer.

### Using a FIFO Do You Need a FIFO?

If you are designing or using a digital system involving high-speed transfers of data or instructions from sources to destinations, you may find a FIFO memory to be useful and economically beneficial. Many digital devices such as computers and peripherals have natural or fixed rates for transmitting and receiving data. The most efficient transfers occur when both the source device and the destination device can operate at the same high speed, and when both perform data transfers simultaneously. Unfortunately this is seldom the case, and either the source or the destination device must spend some time waiting or attending to other chores: Data rate matching, and data buffering, to provide the delay between source transmit to destination receive, are two of the principal applications for FIFO memories.

You should consider the possibility of using a FIFO whenever your system requires transferring data, commands, or instructions from any of the following sources to any of the following destinations. Table 1 shows the family of FIFOs available from Monolithic Memories.

SOURCES	DESTINATIONS
Computer CPU	Computer CPU
RAM or ROM	RAM
Disk Memory Unit	Disk Memory Unit
Magnetic Tape Unit	Magnetic Tape Unit
Paper Tape Reader	Paper Tape Punch
Keyboard	CRT Display
Analog-to-Digital Converter	Digital-to-Analog Converter
Telephone Communications Modem	Telephone Communications Modem
Radio Transmitter	Radio Receiver
Timeshare Computer System	Timeshare Computer System
Data Bus Within Computer	Printer
Address Bus Within Computer	Panel Meter Display
Electromechanical Device	Electromechanical Devices

## First-In First-Out Memories: Operations and Applications

PART NUMBER	ORGANIZATION	FEATURES
67L401	64x4	5 MHz Com
57401		7 MHz Mil
57401A		10 MHz Mil
67401		10 MHz Com
67401A		15 MHz Com
57402	64x5	7 MHz Mil
57402A		10 MHz Mil
67402		10 MHz Com
67402A		15 MHz Com
67413	64x5	Standalone 25 MHz Com
5/67413A		Standalone 35 MHz Com, 25 MHz Mil
74S225	16x5	10 MHz Com
74S225A	16x5	20 MHz Com
67417A	64x8/9	Serializing FIFO 28 MHz serial rate 10 MHz parallel rate

Table 1. FIFO Family

### Classes of FIFO Applications

The two principal uses for the 67401 FIFO are data rate matching and data buffering. Actually these classes overlap somewhat because data rate matching implies data buffering within the FIFO in order to achieve the objective of writing into the FIFO at one rate and reading out of the FIFO at another rate. It is also apparent that you cannot write at one rate and read at another rate continuously without eventually filling (fast write, slow read) or emptying (slow write, fast read) any fixed length

FIFO memory. Once the FIFO is full, it cannot accept additional data until it begins to empty due to reading or clearing its contents.

In the other case, once the FIFO has been emptied, it makes no sense to continue reading until more data has been written. This limitation implies that the faster rate operation (whether reading or writing) must be done in bursts with gaps between bursts to allow time for empty storage space to be created within the FIFO by the slower rate operation.

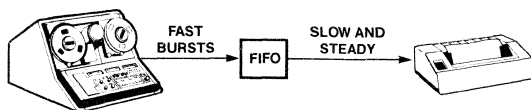


Figure 2. Data Transfer from Magnetic Tape Unit to Printer

### High-Speed Burst to Lower Speed Steady Rate

Figure 2 shows a magnetic tape unit supplying data to a line printer. The printer prints characters at a regular rate that is slower than the magnetic tape unit can supply characters (Figure 3).

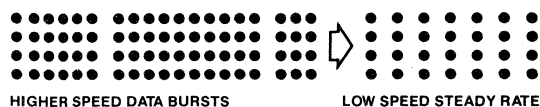


Figure 3. Fast Rate to Slow Rate

## First-In First-Out Memories: Operations and Applications

It is usually inconvenient and expensive to require the MTU to stop and start between characters to wait for the printer. The MTU operates more efficiently by writing a burst of characters at its fixed high rate into the FIFO then waiting for the printer to read the FIFO at its fixed low-speed rate. When the FIFO buffer becomes empty (or almost empty), it can notify the MTU to supply another burst of data. The FIFO's Output Ready signal can be used as an interrupt. It may be convenient to size the FIFO at the maximum line length so that the MTU can reload the FIFO whenever it sees a carriage return. Figure 4 shows a similar application where the printer is being driven from a high-speed computer. By sending bursts of data to the printer, the computer is free between bursts to perform other tasks, such as processing the data to be printed. The practice of storing high-speed bursts in the FIFO and reading at a slower steady rate is useful for many high-speed burst data sources such as disk memories, random access memories, and high-speed data communications links. The printer is typical of a number of fixed rate slow-speed devices such as a paper tape punch, analog-to-digital converter, or a telephone data link.

Direct Memory Access (DMA) is often used as a solution to this kind of rate matching problem. With DMA, the computer stores data in its RAM at the high-speed burst rate. The slow-speed device then reads the RAM directly at its leisure. This method, however, requires a considerable amount of hardware to implement the DMA operation. Because of its simple logic structure the FIFO permits a reduction in hardware.

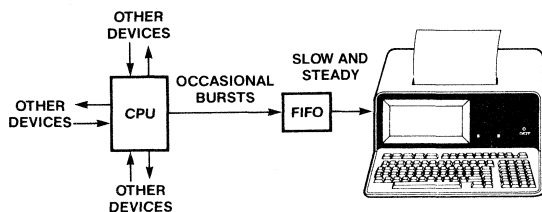


Figure 4. Data Transfer from Computer CPU to Printer

### Low-Speed Steady Rate to High-Speed Burst

Another common situation in digital data transmission is shown in Figure 5. Here the source of data operates at a slow steady rate, while the data destination device is capable of higher speed burst reception. This is illustrated by a paper tape reader supplying data to a high-speed CPU in Figure 6. If the computer were required to read the paper tape reader directly in a programmed I/O operation, it would spend most of its time waiting for the reader to advance. This is a common occurrence in microcomputer software development systems. If the computer can be used for other tasks while it is reading the tape, its operation becomes more efficient and its throughput is higher. Using the FIFO, the tape reader stores the incoming data at its natural rate. The computer reads the FIFO at its maximum input rate until the FIFO is empty or until the computer turns its attention to another task. This slow rate to fast burst operation is appropriate for source devices such as analog-to-digital converters and telephone modems. The destination devices could be a magnetic tape, disk, or CRT display operating at speeds up to 15 MHz.

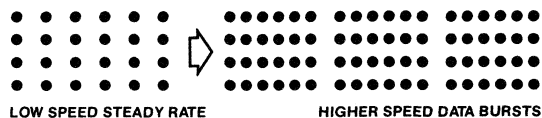


Figure 5. Slow Rate to Fast Rate

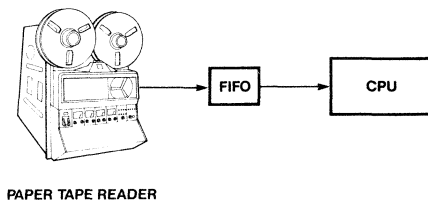


Figure 6. Data Transfer from Paper Tape Reader to CPU

### Steady Rate to Erratic Rate

Figure 7 illustrates a situation where data is available from a source at a fixed rate, but is used by the destination devices at an erratic or unpredictable rate. One example of this situation is a printing terminal receiving data from a telephone modem connected to a timeshare computer (Figure 8). The computer and modem transmit the data at a steady rate, say 300 baud. The printer prints at a steady rate until it gets a carriage return character. The printer may then require several character times to execute the carriage return before it can print the characters that follow. This problem can be solved using the FIFO as a buffer so that the characters following the CR are stored in the FIFO and printed at the natural rate of the terminal. Note that the interval between printing successive characters must actually be slightly faster than 300 baud so that the printer can catch up after each carriage return. Otherwise, the FIFO would gradually fill up and overflow. This is a fundamental characteristic of FIFO buffers. In all cases the average input data rate over a long period of time cannot exceed the average output data rate. In practice the size of the FIFO is determined by the duty cycle of the higher data rate as well as the ratio of input rate to output rate.

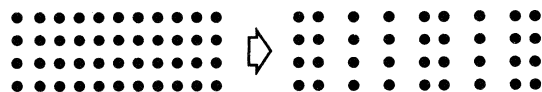


Figure 7. Steady Rate to Erratic Rate

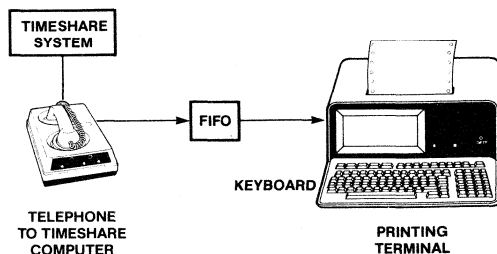


Figure 8. Timeshare Computer System to Printing Terminal

Another example of steady to erratic data rate is the interface to a machine tool such as the turret drill shown in Figure 9. The FIFO is used to store commands received from magnetic tape at a steady rate or a high-speed burst. The execution of these commands varies depending on the mechanical operation required. Changing drills may require much longer than drilling a series of holes.

In some numeric control systems the instructions for a whole shop full of machine tools may be provided by a single shared computer. In this case, FIFOs can be used in each machine tool to store a burst of instructions. Then the computer is free to control other machines, check status, or execute maintenance operations while each machine continues executing commands stored in its own FIFO memory.

The example in Figure 12 shows a digital system using a large high-speed host computer to control a multitude of slower slave computers (possibly microprocessors). The host computer transmits high-speed bursts of commands and data to microprocessors connected to its I/O bus. These are stored in FIFOs and executed by the microprocessors at their own rates. The host computer can control a large number of microprocessors and service its own peripheral devices in either timeshared or multiprocessing mode. Each individual microprocessor uses FIFOs to accumulate results and status information to be polled by the host periodically. In addition each microprocessor operates at its effective rate by buffering its I/O operations in FIFOs. The whole system is connected to a remote control radio link using a FIFO to adjust the data rate between the receiver and the host computer.

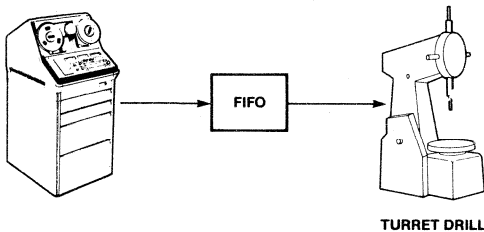


Figure 9. Magnetic Tape Unit to Turret Drill



Figure 10. Erratic Rate to Steady Rate with Gaps

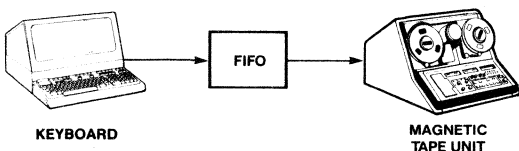


Figure 11. Keyboard to Magnetic Tape Unit

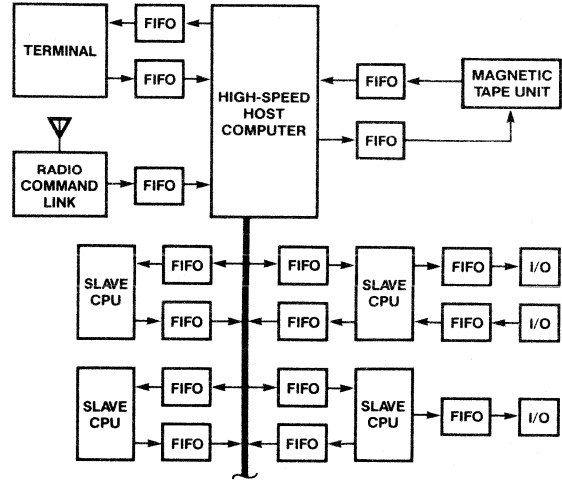


Figure 12. Multiple Processors Receive High-Speed Burst Commands, Execute at Slower Rate, Accumulate Status Information at Slow Rate and Transmit Status at Burst Rate when Polled

## Erratic Rate to Steady Rate

In many cases data is transmitted at an erratic or unpredictable rate, but must be formed into steady high-speed bursts (Figure 10) to be efficiently used by the receiving device. A typical example of this situation is the keyboard to tape machine shown in Figure 11. The information is generated by the keyboard operator at a very erratic rate. The FIFO is used to avoid starting and stopping the tape at irregular intervals to record single characters. As a result, the tape unit can record data in longer records, thereby saving tape and saving the higher cost of an incremental tape recorder.

## Skew Buffering

Up to this point all the examples we have considered have involved parallel words of digital data where each bit in each word was transmitted simultaneously with the other bits in that word. In high-speed magnetic tape readers and other high-speed devices, this may not be a realistic assumption. Figure 13 shows a hypothetical 4-bit magnetic tape system reading four parallel tracks from a tape. Before this data can be used in a digital system, it must be amplified, properly formatted and stored in an output register. Usually the individual bits of a given data word have been skewed with respect to each other during the record and playback operations. The actual data from the tape heads may look something like Figure 14. In some systems individual bits may be skewed as much as three words away from their companion bits. Deskewing the signals from the tape is an ideal application for the high speed of the 67401/A/B FIFO. In such systems there is usually other information about the skewed bits that can be detected and used to help deskew the data. In this application a separate FIFO must be used for each parallel bit of raw data. The remaining three bits of the FIFO may be used to buffer other data relating to the raw data. In our 4-bit example, skewed data is stored in bit zero of four parallel FIFOs and deskewed data is read at their outputs at the same average word rate for input and output.

# First-In First-Out Memories: Operations and Applications

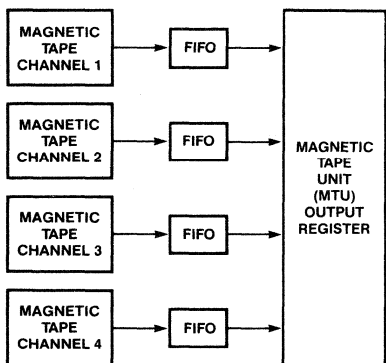


Figure 13. Magnetic Tape Lead to MTU Output

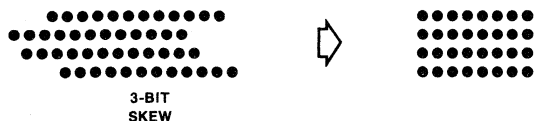


Figure 14. Magnetic Tape Deskewing

## Data Buffering for Delay

In many applications the read and write rates of the FIFO are the same and may even be synchronized. This occurs when the data originating from the source must be delayed before it can be accepted by the destination device. If the destination for the data is a computer and it is occupied by controlling the source while the data is being generated, then the source data can be stored in the FIFO until the computer is freed from that task. Then it can immediately begin processing the data from the FIFO in the order that it was generated.

## FIFO Detailed Description of Operation

The Monolithic Memories' 67401 (Figure 15) is a high-speed, bipolar FIFO with a capacity of sixty-four 4-bit words. Four data lines, an active high READY status signal, and a clock input are

provided for both the input port and output port. Also provided is a master reset signal that logically clears the FIFO to the empty condition.

Data is entered into the first stage of the FIFO whenever the "AND" of the INPUT READY output signal and the SHIFT IN signal makes a LOW-to-HIGH transition. The device acknowledges the acceptance of data into the first stage by providing a LOW output on the INPUT READY line. The data then remains in the first stage until the SHIFT IN signal and INPUT READY signal are both LOW, and the next memory cell is empty. The device then passes the data from the input stage to the next memory cell thus freeing the input stage to accept another word. The device indicates the ability to accept the next word by providing a HIGH output on the INPUT READY pin.

Internally the data is passed from one cell to the adjacent downstream cell, as soon as the adjacent downstream cell is empty. This internal transfer operation occurs at a higher rate than data can be written into and read from the device.

The output stage is loaded with new data whenever it is empty and the next stage upstream is not empty. The loading of the output stage is indicated by the OUTPUT READY signal making a LOW-to-HIGH transition. A specified delay time after both OUTPUT READY and SHIFT OUT signals are HIGH, the OUTPUT READY signal will go LOW. The output becomes empty when the SHIFT OUT signal makes a high-to-low transition. The timing diagram for these operations is shown in Figures 16 and 17.

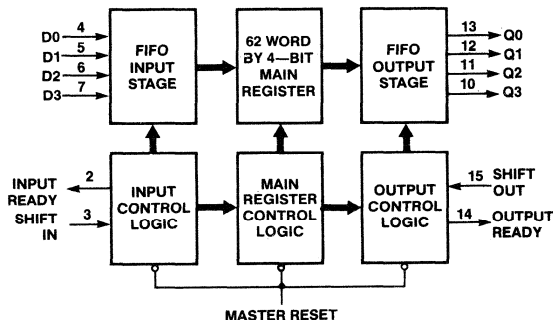


Figure 15. Logic Diagram 67401 FIFO

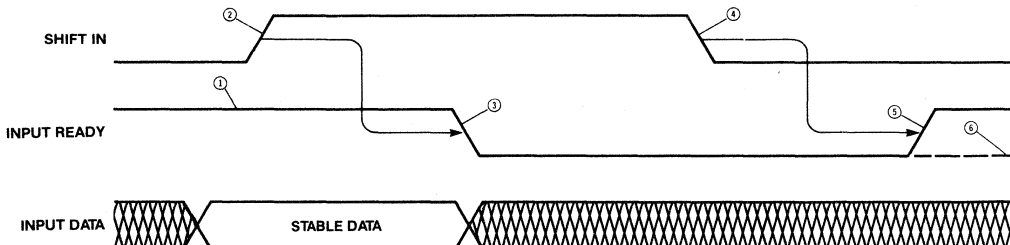
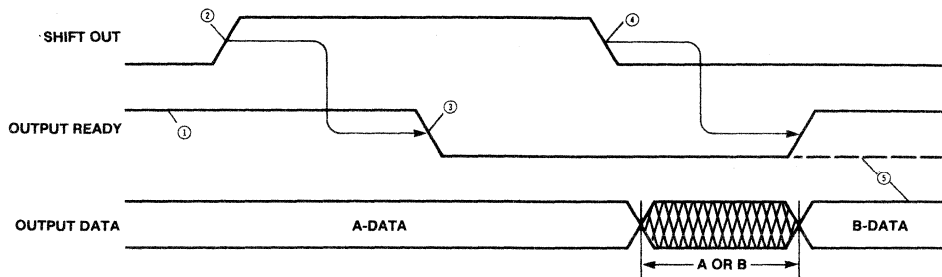


Figure 16. The Mechanism of Shifting Data Into the FIFO

- ① Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
  - ② Input Data is loaded into the first word.
  - ③ Input Ready goes LOW indicating the first word is full.
  - ④ The Data from the first word is released for "fall-through" to second word.
  - ⑤ The Data from the first word is transferred to the second word. The first word is now empty as indicated by Input Ready HIGH.
  - ⑥ If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
- Note: Shift In pulses applied while Input Ready is LOW will be ignored.

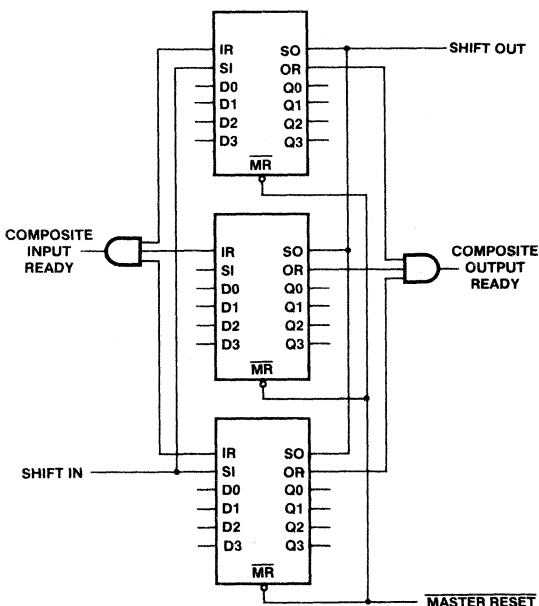


**Figure 17. The Mechanism of Shifting Data Out of the FIFO**

- ① Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
- ② Shift Out goes HIGH causing the next step.
- ③ Output Ready goes LOW.
- ④ Contents of word 62 (B-DATA) is released for "fall-through" to word 63.
- ⑤ Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
- ⑥ If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

## On Cascading Issues

FIFOs sometimes have insufficient depth or width for a particular application. These FIFOs can be cascaded to increase the depth and expanded to increase the width of the data word. In order to expand the width the shift-ins of all the FIFOs should be tied together. Figure 18 shows the technique for implementing a 64x12 FIFO with 67401/A/B. IR and OR signals from all the FIFOs should be tied separately as shown. Also the shift-out clocks and the master resets of all the FIFOs should be tied together.



**Figure 18. 64x12 FIFO with 67401/A/B**

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags due to the different fall-through times of the FIFOs.

For a greater depth (increasing the number of words that can be stored in the FIFO) the technique is shown in Figure 19. The Output Ready of the first FIFO becomes the Shift-In for the second FIFO, while the Input Ready of the second FIFO becomes the Shift-Out for the first FIFO. Figure 19 shows the implementation of a 128x4 FIFO. The handshake which takes place between the two FIFOs is shown in Figure 20. After the master reset is asserted LOW the input ready of both the FIFOs goes HIGH waiting for data to be shifted in. When a word is shifted into the first FIFO it ripples to the outputs of the first FIFO, which are actually tied to the inputs of the second FIFO.

Once the data has rippled to the outputs of the first FIFO, it finds that Shift-Out was already HIGH (since it is connected to Input Ready 2, which was HIGH to indicate the second FIFO's ability to accept another piece of data). Thus, Output Ready 1 goes HIGH.

This instantly causes Shift-In 2 to go HIGH, telling the second FIFO to accept the data on its inputs. After a time t<sub>IRL</sub>, then Input-Ready 2 goes LOW. This means Shift-Out 1 also goes LOW, telling the first FIFO it can place the next data on its outputs.

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

## First-In First-Out Memories: Operations and Applications

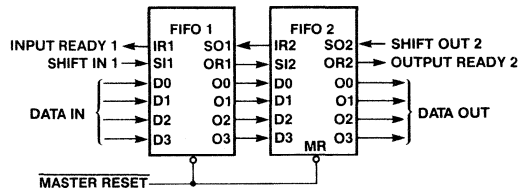


Figure 19. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

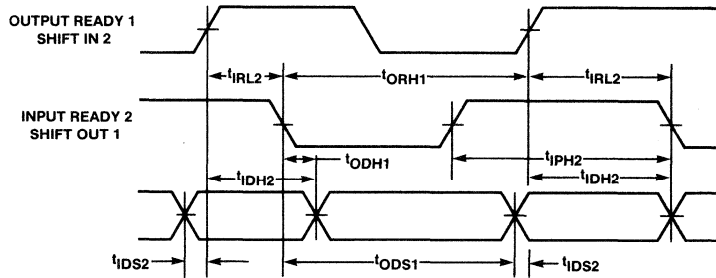


Figure 20. Handshake Timing

### Some Design Considerations

A FIFO is an asynchronous device, hence great care should be exercised in designing with FIFOs. VCC should be clean, as noise on VCC can cause multiple shift cycles, internally. A recommendation is to add an 0.1- $\mu$ F disk capacitor between VCC and GROUND. FIFOs should not be used to drive long lead lengths because of sensitivity to reflections. Always Master reset before starting any FIFO operation. Shift-In (SI) and Shift-Out (SO) rise and fall times are also important. It is recommended to use a Schottky device as a driver, to avoid multiple shift-ins.

### Application Examples UART to CPU Data Buffer

A UART is an MOS/LSI device designed to provide the data interface between a serial communication link and data processing equipment. When transmitting serial data the UART

accepts parallel data bytes from the computer's data bus, converts to serial data, and adds start, parity, and stop bits. The receiver section of the UART accepts serial data from a transmission line, modem, or terminal, validates the data by checking proper start, parity and stop bits, and converts the data to parallel bytes to be read by the computer on its data bus. In effect, the UART is a monolithic serial I/O port for the computer. Serial data rates up to 9600 baud are permitted by the UART, but much slower rates (110 to 300 baud) are commonly used to interface terminals. 110 baud corresponds to 10 bytes per second at the data bus. FIFOs can be used between the computer's data bus and the UART in both receive and transmit mode to match the low serial transmission rates to high speed bursts that make much more efficient use of the computer's time and memory space. A logic diagram for this interface is shown in Figure 21. Four 67401 FIFOs are connected in a series/parallel arrangement for both the transmit and the receive buffers. This arrangement permits a 128-byte buffer capacity for transmit and 128 bytes for receive. The buffers can be expanded easily in both width and length to accommodate different computers or greater buffer capacity.



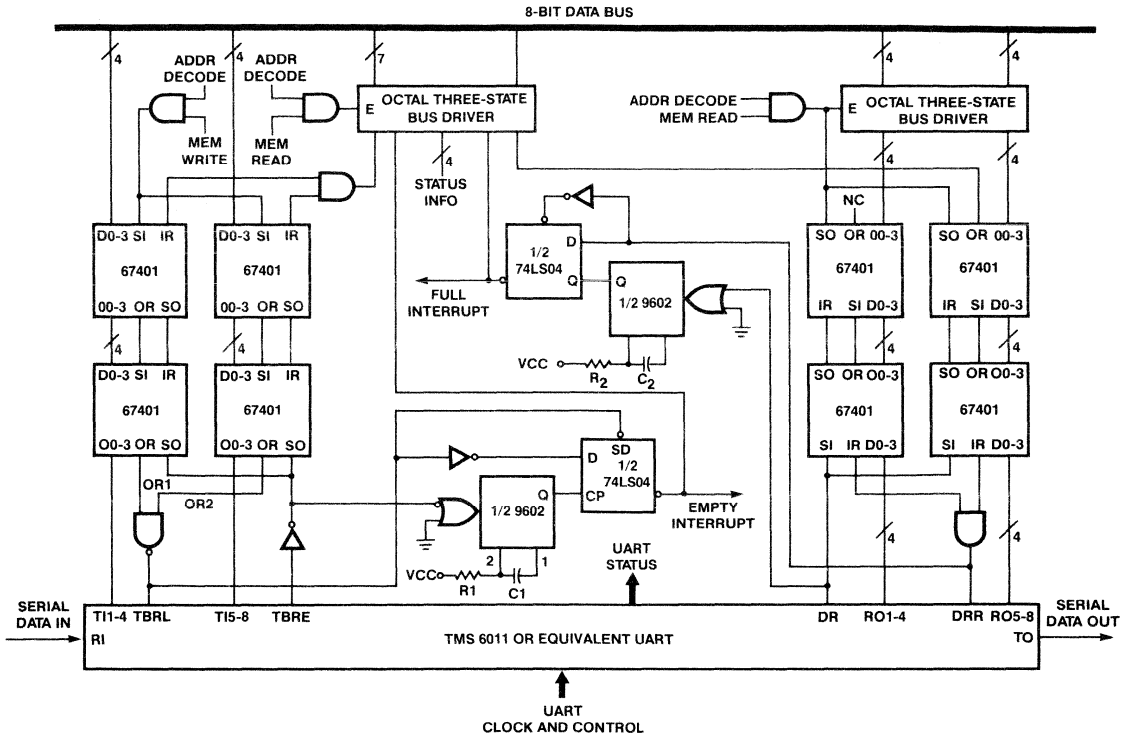


Figure 21. UART Data Buffer Logic for XMIT and RCV Using 67401 FIFOs

**Transmit Buffer Operation**

The interface shown in Figure 21 allows the computer to write bursts of up to 128 bytes at the maximum data rate of the computer into the 67401 FIFO array. The input ready signals are ANDed together and fed back through a status port to the computer data bus so that burst data may be written under program control as rapidly as the write program will allow. The UART reads the outputs of the FIFO array one byte at a time, adds start, stop and parity bits and serializes the data to the serial output at the desired transmission rate (assumed to be much slower than the input burst rate). Assuming that the FIFO array is initially empty, the operation proceeds in accordance with the timing diagram in Figure 22. When the first parallel byte reaches the output of the buffer, the Output Ready lines go high. When both OR1 and OR2 have gone high, the NAND gate drives the UART's Transmit Buffer Register Load (TBRL) signal low. After the tPHL delay in the UART, the Transmit Buffer Register Empty (tBRE) signal goes LOW, causing the UART to

begin shifting out the serial data. tBRE is inverted and a HIGH signal is fed back to the shift out (SO) inputs causing the Output Ready lines to go LOW. When all bits have been shifted out of the transmit buffer register and tBRE is returned HIGH, SO is driven LOW. After the internal FIFO delay tORH the OR lines return HIGH if a new byte is available at the output of the FIFO and the process repeats until the buffer is emptied.

**Transmit Buffer Empty Logic**

In many applications of the 67401 FIFO it is necessary to determine when the transmit buffer is empty or the receive buffer is full. The logic required to provide both these signals is shown in Figure 21.

The 67403D from AMD features two status flags: a Half-Full flag and an Almost-Full/Empty flag. These status flags can be used to signal to the system that the FIFO is approaching an empty state or a full state.

# First-In First-Out Memories: Operations and Applications

## Receive Operation

The receive buffer logic is shown in the right hand portion of Figure 21 and the timing diagram is shown in Figure 23. The UART receives serial data with start, stop, and parity bits, evaluates parity, and converts the data to parallel bytes to be stored in the FIFO at the slow or erratic receive rate. The Data Ready (DR) signal of the UART is tied to SI on the two FIFOs and the two IR lines are ANDed together to drive the Data Ready Reset (DRR) line of the UART. When the FIFO is ready to accept a byte of data from the UART, the AND of the two IR signals holds DRR HIGH. If the UART has a new byte, it sets DR HIGH, driving SI HIGH to enter the new data into the input register of the FIFOs. After the  $t_{IRL}$  delay, IR goes LOW driving DRR LOW. After the  $t_{PHL}$  delay in the UART, DR goes LOW driving SI LOW. If the FIFO is not full, IR returns HIGH after  $t_{IRH}$  indicating to the UART that the FIFO

is ready for the next byte. This cycle repeats until the UART has no more data or the FIFO buffer is full.

Within the FIFOs each new data byte propagates to the top of the available storage until the computer decides to read the stored words at its higher burst rate. The FIFO outputs drive a three-state bus driver interface to the computer data bus. 67403 has a three-state capability. The OR signal is available to the computer via the status port which can be sampled periodically by the computer to determine when new data is available. The computer program initiates data transfers to the bus at its maximum rate by enabling the three-state buffer for each byte and checking the status port between each read cycle.

If the UART fills the FIFO buffer before the computer can get around to dumping it, the almost-full flag generates an interrupt.

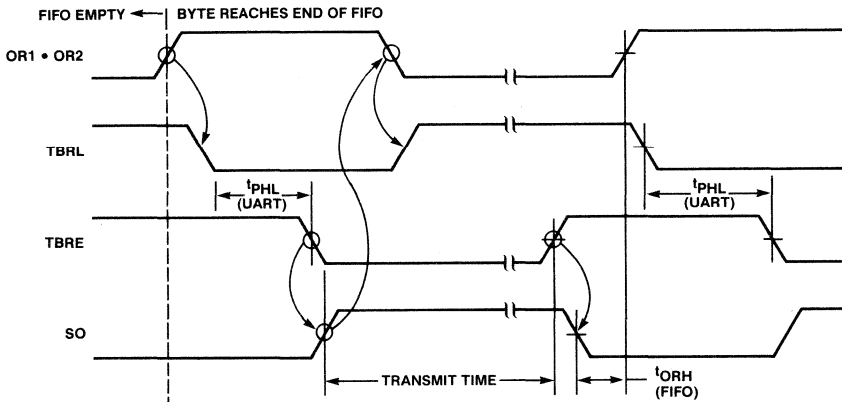


Figure 22. Timing Diagram, Transmit Buffer Operation

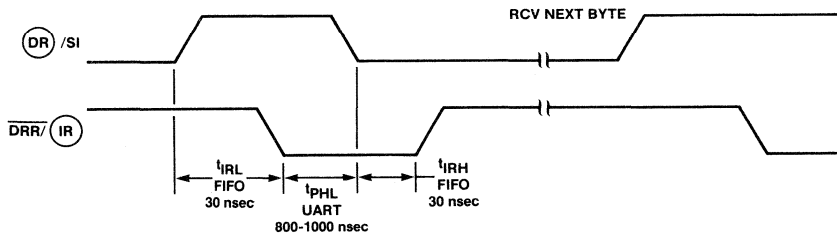


Figure 23. Timing Diagram, Receive Buffer Operation

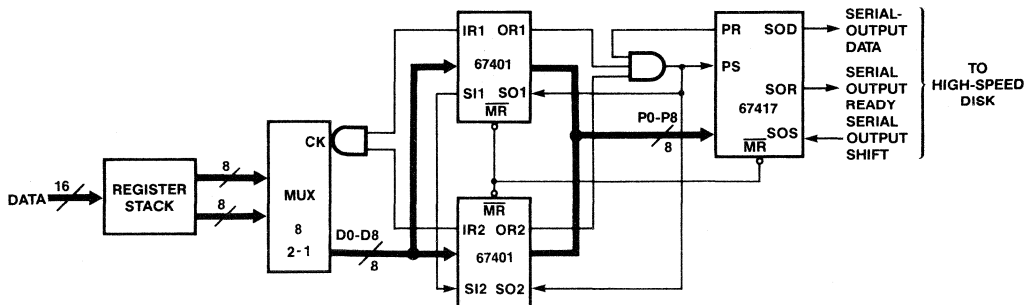


Figure 24. High-Speed Serial Interface

### High-Speed Disk Memory Buffer

A common computer interface requirement is a high-speed serial data interface to a disk memory or other high-speed device. Data is often formatted into records, tracks or other blocks that can be taken together and transmitted as a burst. In the case of a high-speed, high-density disk the data transfer must be made when the desired data passes by the read head. In order for the computer to use this data it must be converted to

parallel data words the size of the computer's basic data word and then resynchronized at a parallel word rate that is convenient for the computer. The reverse of this operation is required to write serial data from the computer to the disk. The logic block diagram (Figure 24) shows a method for accomplishing both serial-to-parallel read and parallel-to-serial write using 67417, 67401 and 67402 FIFOs to buffer 16-bit data words between a microcomputer and a high-speed disk. Serial data rates up to 10 MHz are possible with the components shown in the diagram.

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## Second Generation FIFOs Simplify System Design and Open New Application Areas

Zwie Amitai, Barry Hoberman and Nusra Lodhi

In many digital systems, different sections of the system operate at different rates and transmit or receive data in various formats. A simple example is a microprocessor connected to a slow peripheral such as a tape reader or a slow main memory. It is more efficient to have the microprocessor transmit and receive blocks of data at its full speed, but the peripheral must, due to its basic nature, transfer data one "piece" at a time, at a slow steady rate. A FIFO, used to buffer a block of data, can simplify the hardware design, and allow each subsection to handle the data transfer at its own characteristic pace.

First-In First-Out (FIFO) memories are devices used to buffer between subsystems which have different data rates. Recent innovations in FIFO architecture resulted in a still faster FIFO semiconductor device – AMD's 67413 – which operates in frequencies exceeding 35 MHz. New application areas induced the design and development of system-oriented FIFOs: the 54/74S417 Serializing FIFO which incorporates serial-to-parallel and parallel-to-serial conversion on the same chip, and the 4219 FIFO RAM Controller, which is used with an array of static RAMs to create very deep FIFOs (up to 64K deep) of indefinite width.

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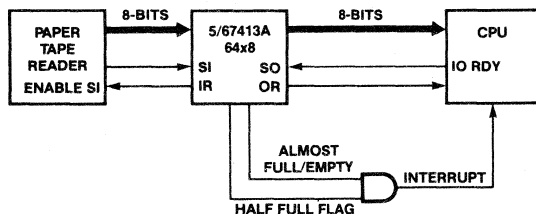
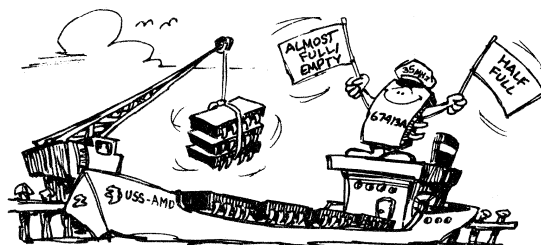


Figure 1. Slow Steady Rate to Fast 'Blocked Rate' FIFO Applications

## FIFO Architectures Exhibit Performance Trade-offs

A FIFO — First-In First-Out — is a dual port memory, from which data can be read only in the same order in which it was written. A FIFO has two independent ports: an input port and an output port. Each port has a READY output and a SHIFT input, which allow the system to access the FIFO. Newer FIFOs have additional "status" flags. The 67413 has a HALF-FULL flag and an ALMOST-FULL/EMPTY flag. The ALMOST flag indicates to the system that an action has to take place to maintain the data flow. The HALF-FULL flag is used to determine which action must take place: start filling or start emptying the FIFO to maintain continuous data flow (Figure 2).



"...THE STATUS FLAGS ON THE HIGH-SPEED 413A FIFO INDICATE WHEN THE FIFO IS CLOSE TO BEING FULL OR CLOSE TO BEING EMPTY, OR MORE OR LESS THAN HALF FULL..."

There are two approaches to FIFO internal architecture. One is the "Fall-Through" architecture based on shift-register technology such as in AMD's 57/67401/2. The other approach, the "RAM-based" approach, uses a random access memory (RAM) array and pointers (i.e., counters) that keep track of the order of the data read and written. An extreme case of the latter architecture is a FIFO constructed from an array of memory chips and an LSI FIFO RAM Controller that consists of the above mentioned counters/pointers and control logic. Each approach has its advantages and drawbacks. A successful compromise between these two architectural approaches led to the 67413's unique architecture allowing super-fast operation with a relatively low fall-through time.

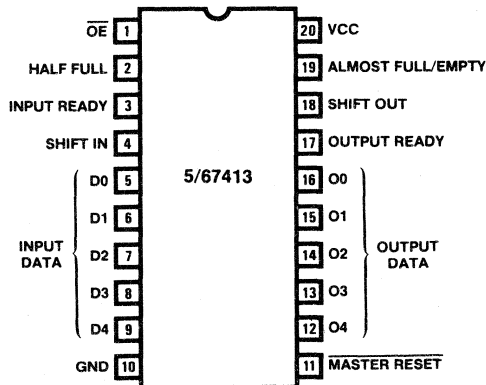


Figure 2. 67413 Pin Configuration

## Second Generation FIFOs Simplify System Design and Open New Application Areas

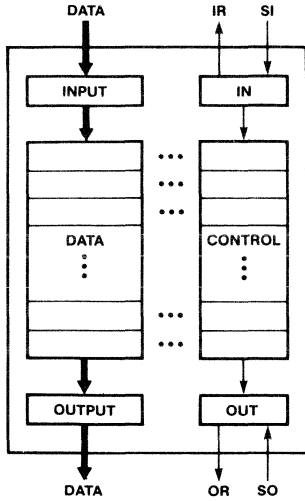


Figure 3. Fall-through, Single-stack, FIFO Architecture

A new approach to the design of FIFO significantly enhances their maximum operating frequency by blending these two architectures. This hybrid approach, used in the design of the 57/67413A at AMD, is a mix of mostly fall-through or "stack" architecture with a small amount of pointer operation i.e., RAM-based technique.

When a word of data is written into the "Fall-through" FIFO, it "trickles down" and stacks on top of the residing words. When a word is read out, an empty location is created at the bottom and all residing words drop down, making the empty location "bubble up."

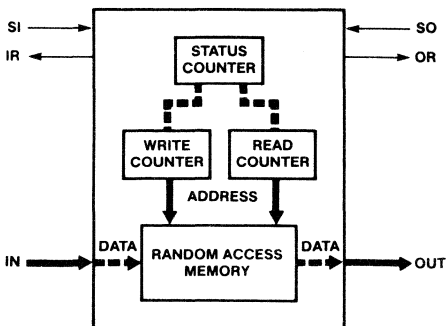


Figure 4. RAM-based FIFO Architecture

A RAM-based FIFO consists of a memory array, a write address counter, a read address counter, and a status counter/subtractor. When a word is entered into the FIFO, it is written into the location pointed by the write address counter. The counter is then incremented to point at a subsequent location. The read address counter is used to point at the location of a word which is read out of the FIFO. A subtractor can be used to keep track of the difference between these two counters and signal when the FIFO is full or empty. In order to achieve high speeds, "ring" address counters and a comparator are used instead of traditional binary counters and a subtractor.

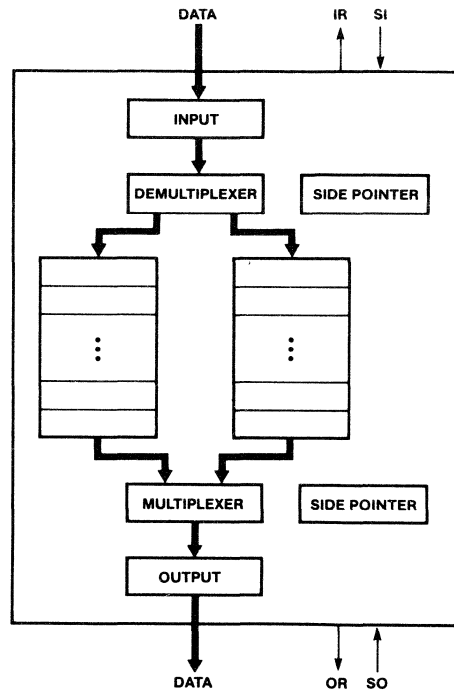
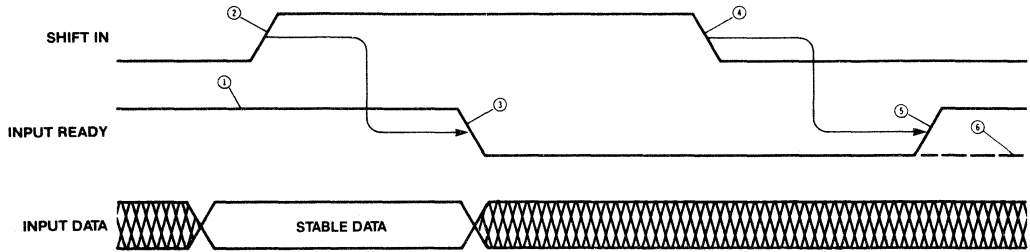


Figure 5. '413 Dual-stack, Hybrid Architecture

The internal architecture of AMD's 57/67413 FIFO incorporates a dual stack and a pointer to double the maximum frequency and halve the fall-through time. The 57/67413 has sixty-four words of five bits each, arranged in two separate thirty-two word "fall-through" stacks, an input port, an output port, and two side pointers. The input port and the output port each generates its own handshaking signals. The input side pointer controls the demultiplexing of incoming data into the two stacks, and the output side pointer controls the multiplexing of the outgoing data from the two stacks onto the output port. The multiplexer and demultiplexer are incorporated in the input and output ports.

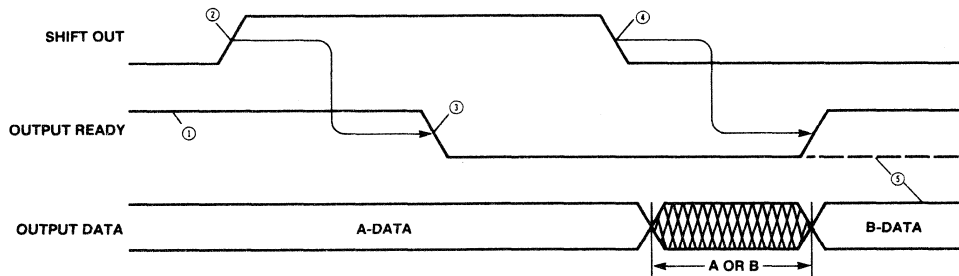
## Second Generation FIFOs Simplify System Design and Open New Application Areas



- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- ② Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
- ③ Input Ready goes LOW indicating the first word is full.
- ④ Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
- ⑤ If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

Figure 6A. The Mechanism of Shifting Data into the FIFO



- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
- ③ Output Ready goes LOW.
- ④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- ⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

Figure 6B. The Mechanism of Shifting Data Out of the FIFO

The above internal scheme is transparent to the user, who is required only to conform to the FIFO's simple, asynchronous handshake protocol. Two signals: Input Ready (IR) and Shift Out (SO) control the data flow into the FIFO (see Figure 6A). Two signals: Output Ready (OR) and Shift Out (SO) control the data

flow out of the FIFO (see Figure 6B). A Master Reset ( $\overline{MR}$ ) signal is provided to clear the FIFO. The master reset must be pulsed (LOW) after power-up to prepare the FIFO to accept data in the first location.



## Second Generation FIFOs Simplify System Design and Open New Application Areas

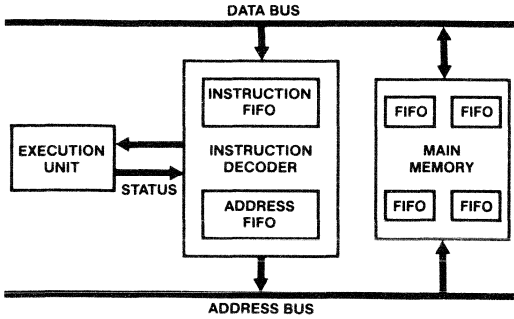


Figure 7. High-speed Processor Architecture

### FIFO Interface Allows Subsystems to Operate at Independent Rates

In pipelined architectures, as shown in Figure 7, a number of events take place concurrently. Instructions are fetched from the memory into a cache, instructions undergo processing in the Instruction Decoder, and the output of this unit initiates the sequence of executable microinstructions.

The concept of "free-running," independent subsystems that are interfaced via FIFOs can be further carried to the main memory section. Here, too, efficient choices of the data bus speed and address bus speed do not necessarily match the inherent speed of the main memory. Four FIFOs can simplify the interface of the main memory to the address and data buses, as shown in Figure 9.

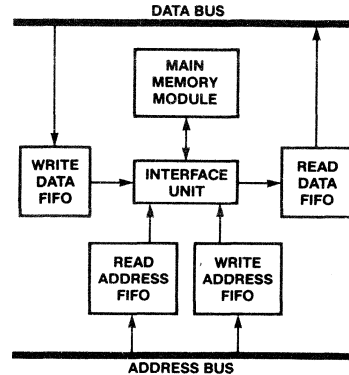


Figure 9. Four FIFOs Simplify Main Memory Interface

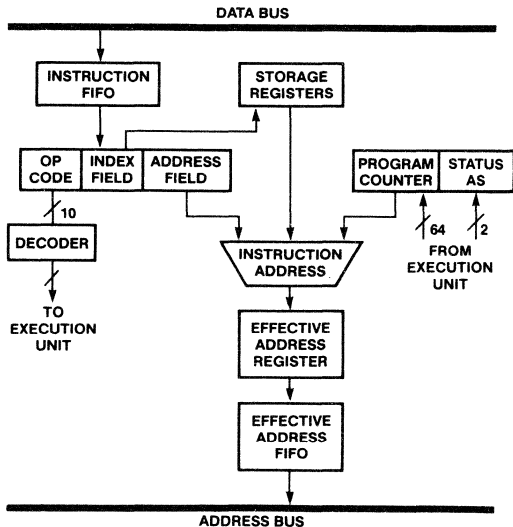


Figure 8. An Instruction FIFO and an Effective Address FIFO in a Basic Instruction Decoder

In order to achieve high throughput, the instructions are queued in an instruction FIFO, and the instruction lookahead can operate on the instructions independently of the data bus operations. A basic function of the instruction decoder is to compute and provide an effective address to the address bus (Figure 8). Once again, the rate of the address generation must fit the rate at which the addresses are needed. An effective address FIFO simplifies the design of the system sections, enabling each to operate independently, as long as their average throughputs are the same. The high speed of the 67413 (35 MHz), and its short fall-through time make it a natural candidate for this task. A three-state output stage with high drive can directly drive a bus and does away with the additional delay caused by buffers.

### Fast FIFOs Capture New Application Domains

The existence of very fast FIFOs brought about new application domains such as data acquisition of fast signals. The following systems exhibit typical high-speed data acquisition techniques using high-speed memory buffers to accommodate data rate differences between the signals and the data logging system. The system shown in Figure 10 detects and stores the pulse rate and frequency of radar signals using a Bragg cell. Both amplitude

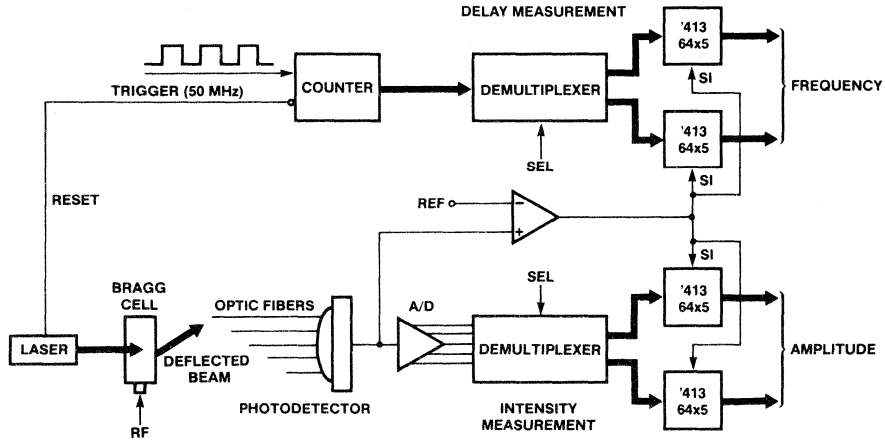


Figure 10. Radar Frequency and Amplitude Acquisition

and frequency data arrive at the rate of 50 MHz and are buffered by FIFOs. A Bragg cell translates the frequency of the radar signal into a deflection of a laser beam, and the amplitude of the radar signal into the intensity level of the laser beam. The deflected laser beam hits one or two fibers out of a collection of fibers of different lengths, that are connected to a photocell. The signal arrives at the photocell after a delay determined by the length of the fiber. Therefore, the delay relates directly to the radar frequency. A counter is used to measure the delay. The counter is reset when the laser beam is triggered, and once the beam is detected at the photodetector, its contents are written into a buffer. This technique is quite general and can be used also for pulse rate measurement. The laser beam intensity is sampled, converted to a digital format, and written into another

buffer. Two FIFOs and a multiplexer are needed for each buffer to allows data rates over the FIFO's 35-MHz maximum operating frequency up to 70 MHz.

Another data acquisition application is a Particle Flight Detector. Due to the nature of the observed phenomena, the data coming out of a Particle Flight Detector is generally in short bursts. The temporal frequency of the data exceeds 30 MHz while the average rate of the data stream is much lower, and can be handled by a standard bus such as the SYSBUS (32-bit, 10-MHz international standard bus for physics instrumentation). The block diagram shown in Figure 11 utilizes an array of 35-MHz FIFOs to handle the bursts of data and two arrays of static RAMs to ensure maximum bus throughput.

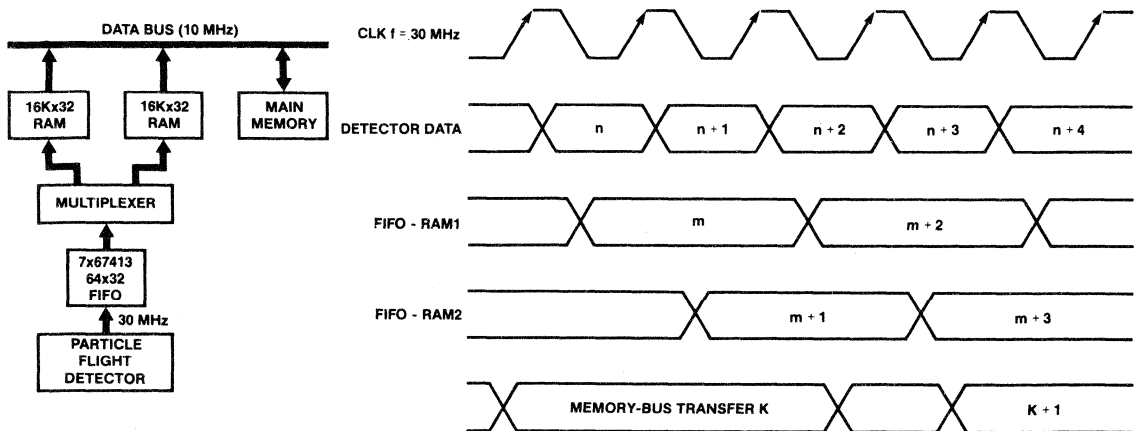


Figure 11. Particle Flight Detector Interface to a 10 MHz Bus (SYSBUS)

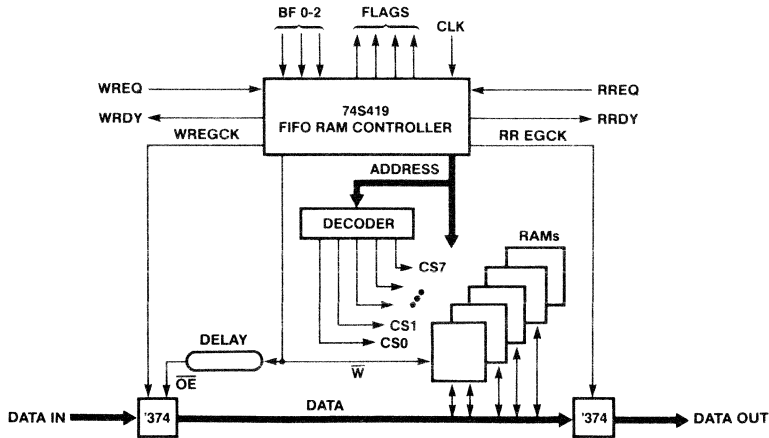


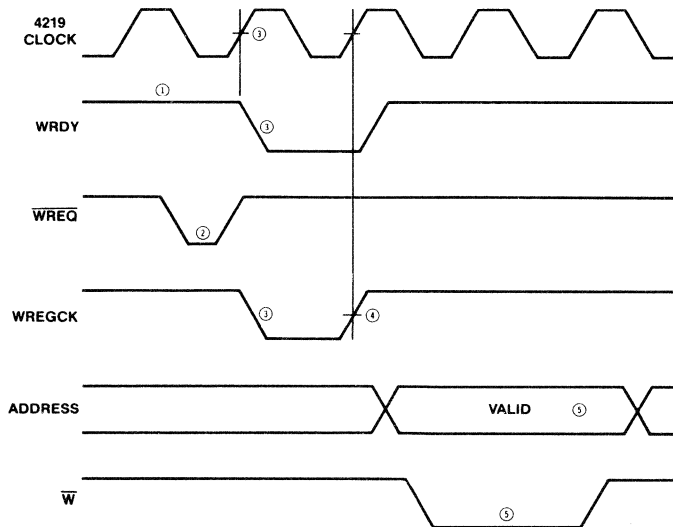
Figure 12. A FIFO RAM Controller and Static RAMs Make a Very Deep FIFO of Variable Width

### Very Deep FIFOs Implemented by an LSI Controller and a Static RAM Array

The search for system-oriented LSI solutions for very deep buffers, such as those needed for communication networks, resulted in the development of the FIFO RAM Controller which can make a static RAM array look like a FIFO (see Figure 12). The 54/74S4219 FIFO RAM Controller integrates all address generation and status detection needed to control the static RAMs, giving the system designer two simple "handshake"

signals for input (write) and output (read) operations. A read counter and a write counter provide the read and write addresses, while an up-down counter keeps track of the difference between these two counters. The status flags include the FULL, EMPTY, ALMOST-FULL/EMPTY, and the HALF-FULL flags, and are generated according to the buffer length selected. The buffer length can vary from 512 to 64K words, and the maximum data rate at each port exceeds 15 MHz. Arbitration between read and write requests is done in the controller according to priority rules pin-selected by the user.

2



- ① WRDY is HIGH; new Write requests may be made.
- ② A Write request is made (WREQ pulled LOW) asynchronously of the '4219 clock.
- ③ The request is synchronized, WRDY goes LOW to indicate that no Write request should be made. WREGCK goes LOW.
- ④ WREGCK goes HIGH clocking the data into the Write Data Register.
- ⑤ A Write cycle takes place over two '4219 clock cycles.

Figure 13. '4219 Write FIFO Operation

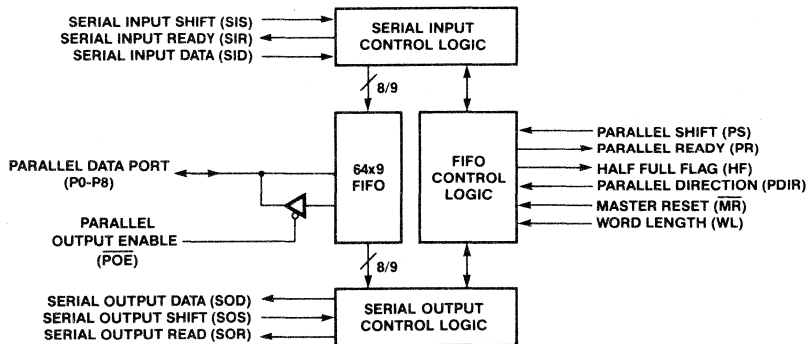


Figure 14. '67417 Serializing FIFO Architecture

The '4219 was designed to isolate the static RAM array from the rest of the system so that the handshake protocol will be similar to the protocol required by most FIFOs. The '4219 generates all the control signals for the static RAMs, and the subsystems on either side monitor two outputs of the '4219 (the Register clock and the Ready) and supply only one control signal (Request). The protocol of the write (input) FIFO transaction is shown in Figure 13. The data must be available at the write data register no later than one '4219 clock cycle after the write request has been asserted. The data may be terminated after WREGCK has gone HIGH clocking the data into the register. The read (output) FIFO transaction protocol is similar. The data is available at the read data register outputs once RREGCK is HIGH. The priority controls and the request enables give the system designer more flexibility in his system design, and allow one subsystem to take either complete control of the FIFO operation, or just priority in case of simultaneous write and read requests.

### System Oriented FIFOs Incorporate Serializing/Deserializing Functions

The 67417 is a serializing FIFO intended as a one-chip solution for data buffering and serializing/deserializing operations. It can be successfully used for interfacing parallel-format computing equipment to serial-format data communications and mass memory equipment. The device's architecture (see Figure 14) includes one parallel port for both input and output of parallel-format data, and two serial ports: one for input and one for output. Data flow can be parallel-to-serial, serial-to-parallel, and serial-to-serial. Each port has its own Request-Ready signal pair and is accessed using a simple handshake protocol similar to the one used for most FIFOs.

Most applications of the 67417 conform to the block diagram shown in Figure 15. The ability to change the FIFO's direction may be used to reduce chip count in systems that always empty the FIFO contents before changing the direction of the data transfer. Other applications may use two FIFOs back-to-back to create a FIFO transceiver with serializing/deserializing capability.

The word length of the parallel format can be eight or nine bits (selected by the WL pin), and can be changed when the FIFO is partially full. This feature allows the FIFO to be loaded with 8-bit words and unloaded as a 9-bit FIFO with zeros in the 9th bit locations.

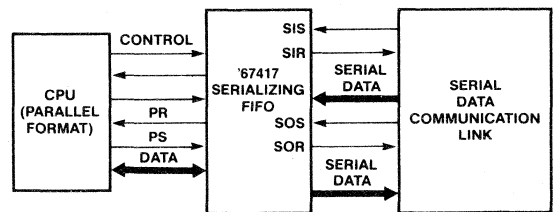


Figure 15. '67417 Serializing FIFO Interfacing a CPU and a Serial Data Communication Link

With the availability of high-speed FIFOs with "system-oriented" features, such as high drive and status flags, system designers can have a more compact and flexible system architecture. New application areas appear for the new FIFOs using their higher speeds and special features.



Advanced  
Micro  
Devices

AN-177

# Cascadability Issues in Advanced Micro Devices' Shallow FIFOs

John McGowan

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## Abstract

The First-In, First-Out Memory (FIFO) allows the system designer to buffer two streams of data which are running at different rates, even asynchronously. This application note pertains to *cascadable* FIFOs, which can operate as a single-component data buffer, or can be cascaded to form

deeper, multi-component, customized buffers. Ensuring that these devices can cascade over a large frequency range, and with asynchronous data streams, requires certain timing criteria to be satisfied. These criteria are the focus of this application note.

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# Cascadability Issues in Advanced Micro Devices' Shallow FIFOs

John McGowan

## Operation Overview

Small FIFOs are controlled by two signals, Shift In (SI) and Shift Out (SO). There are two status signals generated by the FIFO: Input Ready (IR) and Output Ready (OR). A typical small FIFO pinout is shown in Figure 1.

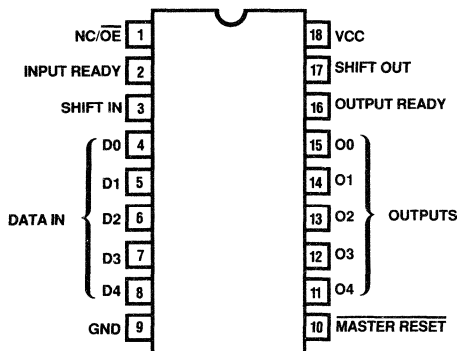


Figure 1. Typical Small-FIFO Pinout

Data is shifted into the FIFO as follows:

1. SI and IR both being HIGH initiates the shift in.
2. The FIFO internally detects a valid shift in by ANDing the SI and IR signals.
3. Data is latched by the FIFO when this valid shift is detected.
4. The FIFO acknowledges the valid shift by bringing IR LOW.
5. The SI line is brought LOW to complete the shift in operation, and to reset the valid shift detect.
6. IR returns HIGH if there is room for new data.

Data is shifted out of the FIFO as follows:

1. SO and OR both being HIGH initiates the shift out.
2. The FIFO internally detects a valid shift out by ANDing the SO and OR signals.

3. The FIFO acknowledges the valid shift out by bringing OR LOW.
4. The SO line is brought LOW to complete the shift out operation.
5. If the FIFO is not empty, OR will return HIGH following SO going LOW. Whenever OR is HIGH, a valid data word is present at the outputs.

The shift in operation is independent of the shift out operation, allowing data to be shifted in at a different rate than it is shifted out. The FIFO indicates that it is full by holding IR LOW after a shift in, and that it is empty by holding OR LOW after a shift out.

## Cascading

If a deeper buffer size is required, two or more FIFOs may be cascaded, as shown in Figure 2.

The operation of this buffer is identical to that of the single FIFO buffer. The user controls the shifting of data into the most *upstream* part, and the shifting of data out of the most *downstream* part. This composite buffer has the same handshake (SI, IR, SO, and OR) and data (D0..D4, O0..O4) lines as a single FIFO.

The user has control over the data as it enters and leaves the buffer. The passage of data through the "middle" of the buffer is beyond user control. This data must be capable of being correctly transferred between any of the "middle" devices at a rate greater than or equal to the overall buffer throughput rate.

The point of data transfer between two FIFOs is called the *cascade interface*. There are numerous timing criteria which must be satisfied by the FIFOs on each side of this interface in order to ensure a flawless transfer of data. This is true even for two-FIFO buffers, in which the "middle" of the buffer consists of a single cascade interface. Such criteria must be satisfied at all frequencies within the operating range, and for asynchronous data streams. The following cases illustrate the various timing conditions that may be encountered whenever two or more FIFOs are cascaded.

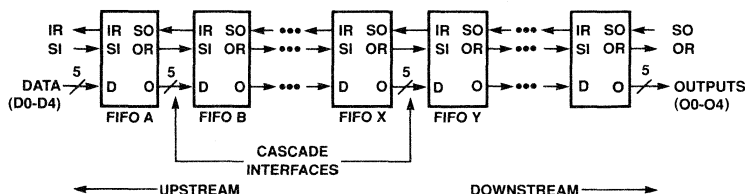


Figure 2. A Cascaded Buffer

**Case 1: Low-Frequency Fallthrough**

Monolithic Memories' shallow FIFOs are *fallthrough* devices, that is, the first word shifted into an empty part automatically "falls through" the buffer and it becomes visible at the outputs. Its presence is indicated by the rising edge of OR. The following sequence describes this fallthrough action as a word is shifted into FIFO A (see Figure 2):

1. IR of FIFO A is HIGH because the device is empty.
2. The user brings SI HIGH, latching the data word and commencing a shift in.
3. SI is then brought LOW to release the word for fallthrough.
4. OR of FIFO A will go HIGH within the "fallthrough time" (tPT). OR going HIGH signals a valid word at the outputs.
5. IR of FIFO B is HIGH because it, too, is empty.
6. Because OR of A is tied to SI of B, a valid shift in is begun into FIFO B on the rising edge of OR.
7. Because IR of B is tied to SO of A, a valid shift out is begun (SO\*OR = 1) out of A.
8. Data is simultaneously shifted out of A, and into device B. The transfer is thus begun.
9. Because a valid shift out is detected in A, OR goes LOW to acknowledge it. This becomes a falling edge on SI for B.
10. The transfer is now complete. The word falls through B, then through FIFO C, and so on, until it reaches the outputs of the bottom FIFO.

The timing diagram for low-frequency fallthrough is shown in Figure 3.

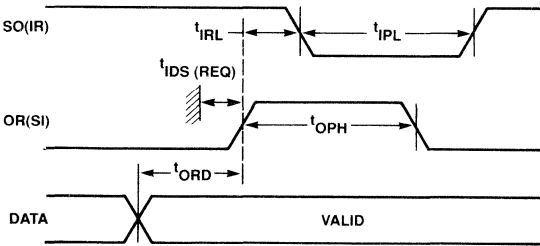


Figure 3. Low-Frequency Fallthrough

The term "low frequency" means that the time between arrival of words is long relative to the time required for a data transfer. There is a basic set of timing requirements that must be satisfied in all fallthrough cases, plus an additional one for high-frequency operation. The basic set will now be discussed.

Consider a cascade interface between FIFOs X and Y of Figure 2. The OR of X goes HIGH, then is quickly reset once a valid shift out is detected. The duration of this OR pulse, termed tOPH, must be long enough to be used by the SI of the downstream FIFO (Y). Specifically,

$$t_{OPH} > t_{SIH(Required)} [1].$$

This requirement is shown as a function of temperature in Figure 4.

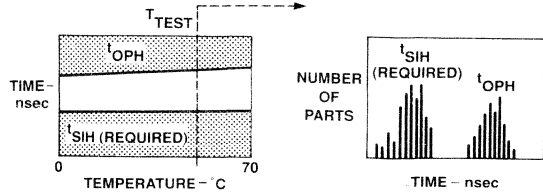


Figure 4. tOPH vs. tSIH at a Particular VCC

The tOPH requirement is derived from histograms generated during the characterization of a broad sample of cascadable parts. The parts are tested individually at a variety of voltage and temperature conditions. AMD specifies its cascadable FIFOs with a reliable margin between the tOPH and tSIH histograms under each condition.

A short logic 1 pulse on SI will produce a short logic 0 pulse (tIPL) on IR. tIPL must be long enough to be recognized as a legitimate SO low pulse by the upstream part X. Thus,

$$t_{IPL} > t_{SOL(req)} [2].$$

There is a direct relationship between tSIH and tIPL. The requirements on tIPL from [2] are used to dictate the requirement on tSIH. The parameter tIPL is used only for characterization and internal testing and does not appear in AMD sheets.

Next, there is the need for SO and OR to be simultaneously at a logic 1 long enough for the FIFO to detect a valid shift out. This time requirement, which is not found in the datasheets is termed tSOHR(req), "time for SO to remain high after OR goes high." If IR, which drives SO, goes LOW too soon after a valid shift in is detected in Y, the tSOHR requirement in X may be violated. If so, no shift out will take place. Therefore,

$$t_{IRL} > t_{SOHR(req)} [3].$$

The parameter tSOHR is characterized and tested. It is normally small relative to tSOH.

The last requirement for Case 1 pertains to data set-up. When in the fallthrough mode, input data is taken as valid on the rising edge of SI. The set-up time for this data (tIDS) must be met. Note, however, that meeting this set-up time is the responsibility of the upstream part (X). When X brings its OR pin HIGH, it indicates that new data is present. The time from OR HIGH to new data valid is termed tORD. Because this rising edge commences a shift in for the downstream part, the following relationship must hold:

$$-t_{ORD} > t_{IDS(req)} [4].$$

In all AMD cascadable FIFOs, tIDS max is specified at zero, while tORD max is never specified greater than zero. By this convention, [4] is always satisfied. The validity of inequality [4], and others documented in this application note, are ensured via the method of separation of parametric distributions, as illustrated in Figure 4.

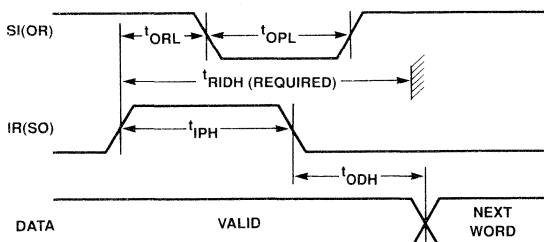
### Case 2: Low-Frequency Bubbleback

The term "bubbleback" is a hangover from the register-based FIFOs. Bubbleback occurs when one or more devices in the composite buffer are full, and a word is clocked out of the most downstream one. A vacancy is created in this bottom FIFO, and is soon filled by the first FIFO upstream from it. The vacancy then "bubbles back" all the way to the most upstream FIFO. In the process, a data transfer is required each time the vacancy crosses a cascade interface, as was the case for fallthrough.

The following sequence describes this bubbleback action:

1. The user shifts data out of the most downstream FIFO.
2. Since this FIFO is no longer full, its IR pin goes HIGH.
3. The first FIFO upstream from it held its OR HIGH, because it was not empty.
4. The IR of the end FIFO is tied to SO of the FIFO above it. The rising edge on IR commences a shift out of the upstream FIFO.
5. Simultaneous shift cycles occur in both FIFOs. IR of the end FIFO goes LOW to acknowledge the valid shift in.
6. IR going LOW in the end FIFO resets the valid shift out of the upstream device. Since this upstream part is not empty, its OR pin returns HIGH.
7. Because this upstream part now contains a vacancy, it commences a shift out of the next higher part. This process continues until the vacancy reaches the *most upstream* device.

The timing diagram for the cascade interface is shown below.



**Figure 5. Low-Frequency Bubbleback**

In bubbleback it is IR going HIGH which initiates the transfer of data. IR goes HIGH, then is quickly reset once a valid shift in is detected. This is analogous to the fallthrough case in which OR is pulsed HIGH. The first three bubbleback inequalities, then, are merely I/O duals of [1] through [3]:

$$t_{IPH} > t_{SOH}(\text{req}) \quad [5],$$

$$t_{OPL} > t_{SIL}(\text{req}) \quad [6],$$

$$t_{ORL} > t_{SIHR}(\text{req}) \quad [7].$$

There is no data set-up requirement for low-frequency bubbleback since the next data word is present and waiting long before a vacancy arrives for it. This data must, however, satisfy a hold time requirement, as measured from the start of the valid shift in.

As seen in Figure 5, SO is brought LOW in the middle of the data transfer. Bringing SO LOW clears the upstream FIFO, causing its read pointer to advance. A new data word then begins its way toward the outputs. The current word being transferred eventually becomes "old" data, to be replaced by the next word. The time that the "old" data is held after SO goes LOW is called tODH.

The bubbleback hold time requirement (see Figure 5) can be expressed as:

$$t_{IPH} + t_{ODH} > t_{RIDH}(\text{req}) \quad [8a].$$

The parameter tRIDH is the data hold time, relative to IR going HIGH. It is measured relative to IR because, in the bubbleback case, IR initiates the shifting-in of data.

Testing of [8a] is required to ensure cascadability in all outgoing parts. However, inequality [8a] mixes parameters from both the upstream (tODH) and the downstream (tIPH, tRIDH) parts. It is therefore necessary to rewrite [8a] so that it can be examined on individual parts:

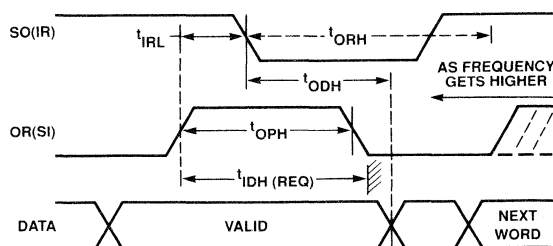
$$[t_{IPH} - t_{RIDH}(\text{req})] > -t_{ODH} \quad [8b].$$

The quantity on the left hand side of the equation becomes a new characterization parameter, called t1. If there is a sufficient margin between the test histograms of t1 and tODH (as was the case for tOPH versus tSIH), then criterion [8a] will certainly be satisfied.

### Case 3: Higher-Frequency Fallthrough

In Case 3, the frequency of operation becomes high enough such that the data transfer time is no longer negligible when compared to the time between arrivals of any two words. Still, the frequency is low enough such that the operation is clearly fallthrough, i.e., OR going HIGH initiates the transfer of data into a downstream part that is clearly waiting for new data.

The timing diagram for this case is shown in Figure 6.



**Figure 6. Higher-Frequency Fallthrough**

Inequalities [1] through [4] from Case 1 still hold. One more must be added to account for the second rising edge of OR, which now occurs soon after the data transfer.

The falling edge on IR, which occurs after a valid shift in is detected, is seen by the upstream part as a falling edge on SO. This implies a read pointer advance, which could bring new data to the outputs. In the low-frequency case there was no new data to bring, so the current word remained valid for quite some time. At higher frequency, there is a new word to bring to the outputs, which reduces the time that the current data is



## Cascadability Issues in Advanced Micro Devices' Shallow FIFOs

valid. There is the risk of a data hold time violation unless the following relationship is met:

$$t_{IRL} + t_{ODH} > t_{IDH}(req) \quad [9].$$

The parameter  $t_{IDH}$  is the data hold time relative to SI going HIGH.

As the frequency of operation gets continually higher, the second rising edge of OR falls closer to that of IR. The limiting cycle time for true fallthrough, as depicted here, is  $t_{IRL} + t_{ORH}$ , although this cycle time may not be obtainable due to limitations described in the section on natural frequency.

### Case 4: Higher-Frequency Bubbleback

In Case 4 the time between creations of vacancies approaches the time required for data transfer. However, the frequency is assumed low enough such that the operation is clearly bubbleback, i.e., the rising edge of IR initiates a shift out of an upstream part which is clearly waiting with valid data.

The timing diagram for this case is seen below.

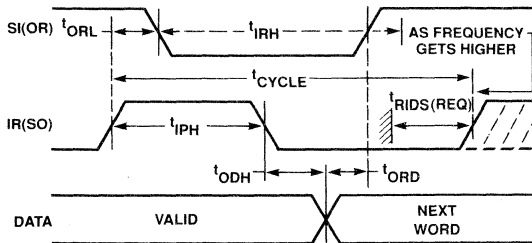


Figure 7. Higher-Frequency Bubbleback

Inequalities [5] through [8] from Case 2 are still pertinent. One more must be added to account for the rising edge of IR, which reappears soon after the data transfer.

As vacancies bubble back at ever increasing rates, there is the risk of violating the data set-up requirement as measured from the edge of IR. Specifically, the following relationship must hold:

$$t_{CYCLE} - t_{IPH} - t_{ODH} > t_{RIDS}(req) \quad [10].$$

The parameter  $t_{RIDS}$  is the set-up time relative to IR going HIGH, Inequality [10] tells us that if  $t_{CYCLE}$  gets too short, there may be a data set-up violation. As seen in Figure 7, so long as we remain in bubbleback mode, with IR coming high after SI, we will have  $t_{IPH} + t_{ODH} + |t_{ORD}| < t_{CYCLE}$ , implying  $t_{CYCLE} - t_{IPH} - t_{ODH} > |t_{ORD}|$ . However, AMD designs its cascaded devices such that  $t_{RIDS}(req) < 0$ , and  $t_{ORD} < 0$ , thereby ensuring that there is no set-up violation.

As the frequency of operation gets continually higher, the second rising edge of IR falls closer to that of OR. The limiting cycle time for true bubbleback, as defined here, is  $t_{ORL} + t_{IRH}$ , although this cycle time may not be obtainable, as discussed in the next section.

### Case 5: Natural Frequency

As mentioned previously, the user has no control over the handshake operations at the cascade interfaces. If the user shifts words into a relatively empty buffer at low frequency, the cascade interfaces will operate in the fallthrough mode (Case 1). If the user shifts words out of a relatively full buffer at low frequency, then the interfaces will be forced to operate in bubbleback mode (Case 2). For continuous operation at moderately high rates, the interface timing will begin to resemble one of the next two (3 and 4) cases.

As the frequency is increased further, the interface timing may no longer be clearly bubbleback or clearly fallthrough. This is what occurs as the throughput rate approaches the *natural frequency* of the cascade interface. This natural frequency is the maximum frequency at which the handshake signals can negotiate part-to-part data transfers. Consider Figure 8.

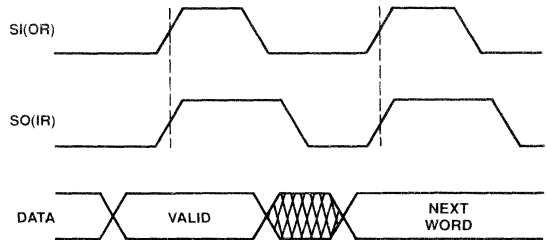


Figure 8. Zero-Phase Incidence

Figure 8 illustrates a perfectly legitimate handshake operation. There is clearly a shift in ( $SI^*IR=1$ ) and a shift out ( $SO^*OR=1$ ), implying a transfer of data. However, none of the previous cases directly apply since it is neither a fallthrough nor a bubbleback case.

In the fallthrough mode SO was clearly high before OR, while IR went high clearly before SI. Thus, SO had *positive phase* relative to OR, while SI had *negative phase*. Likewise, the bubbleback mode has negative phase for SO and positive phase for SI. The relative phases of the SI and SO signals have important implications for the cascading parameters at high frequencies. As explained later, the natural frequency of cascading must be guaranteed higher than the maximum throughput rate applied to the cascaded FIFO system. Predicting and measuring the natural frequency poses some difficulties, as explained below.

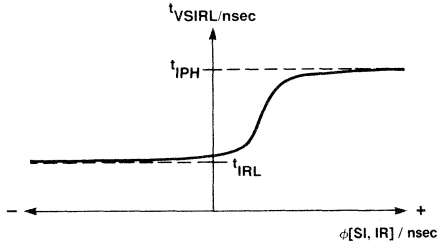
The fallthrough parameters  $t_{IRL}$ ,  $t_{OPH}$ ,  $t_{IDH}$ , etc., are all characterized at positive SO, negative SI phase, whereas the bubbleback parameters  $t_{ORL}$ ,  $t_{IPH}$ ,  $t_{RIDH}$ , etc., are all characterized at positive SI, negative SO phase. When the relative phases approach zero from either side (Figure 8), the meaning of these parameters becomes ambiguous. Take for example the parameter "time from valid shift in ( $SI^*IR=1$ ) to IR going low." For positive phases this quantity approaches the  $t_{IPH}$  asymptote, while for negative phases it approaches the  $t_{IRL}$  asymptote. When the phase is near zero, this quantity lies somewhere in between, as shown in Figure 9.

As indicated on the graph, a new name is required for this pseudo-parameter. It will be known here as  $t_{VSIRL}$ , or "time from valid shift in to IR low." Similar graphs can be generated for

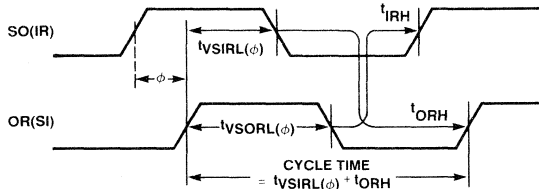
## Cascadability Issues in Advanced Micro Devices' Shallow FIFOs

the pseudo-parameter called  $t_{VSORL}$ , as well as for  $t_{(R)IDS}$  and  $t_{(R)IDH}$ . This sort of graphical information is useful when analyzing operating characteristics at or near the natural frequency. At this point there are two approaches one can take to predicting the natural frequency:

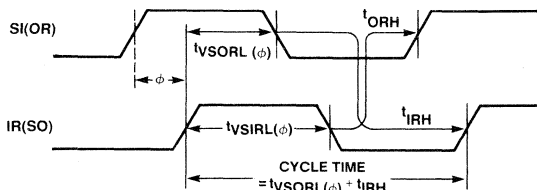
- 1) Take an iterative approach to determine the minimum working values of phase ( $\phi$ ),  $t_{VSIRL}(\phi)$ ,  $t_{VSORL}(\phi)$ ,  $t_{(R)IDS}(\phi)$ , etc., using two figures, 10 and 11.



**Figure 9.  $t_{VSIRL}$  as a Function of Phase**



**Figure 10. Positive SO/OR Phase at Natural Frequency**



**Figure 11. Positive SI/IR Phase at Natural Frequency**

One needs to determine which of the two cases (Figures 10, 11) has a lower maximum frequency. In equation form:

$$1/f_{MAX} = \max\{t_{VSIRL}(\phi) + t_{ORH}, t_{VSORL}(\phi) + t_{IRH}\} \quad [11]$$

- 2) Approach (1) provides the exact value of the natural frequency, but only after a considerable amount of iteration. There exists a simpler approach to the problem, based upon the results of Cases 3 and 4. This approach yields a conservative estimate of the natural frequency, such that if the composite buffer is operated at or below this frequency, cascadability can be guaranteed.

Figure 6 depicts fallthrough operation based on the assumption that  $t_{IRL} + t_{ORH}$  is clearly greater than  $t_{OPH} + t_{IRH}$ . If this is not the case, then the second rising edge of OR could possibly occur before the second rising edge of IR. Then, the parameter  $t_{OPH}$  is no longer valid, and should be replaced by the more applicable  $t_{ORL}$ . However,  $t_{ORL}$  pertains to cases where SO arrives substantially after OR. If the rising edges of IR and OR are close to one another, then the applicable value may lie somewhere inbetween  $t_{ORL}$  and  $t_{OPH}$ . To be safe, merely take the greater of these two values.

The same reasoning applies for the breakdown of the fundamental assumption of Case 4. The following is a simple worst-case expression for  $f_{MAX}$  at each operating condition:

$$1/f_{MAX}(wc) = \max\{t_{VSIRL}(\max) + t_{ORH}, t_{VSORL}(\max) + t_{IRH}\} \quad [12a],$$

where:

$$t_{VSIRL}(\max) = \max\{t_{IRL}, t_{IPH}\} \quad [12b],$$

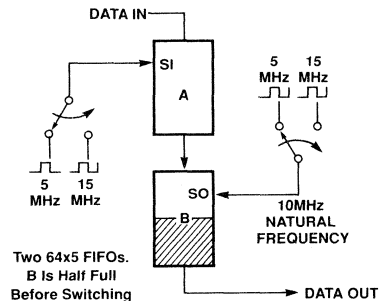
$$t_{VSORL}(\max) = \max\{t_{ORL}, t_{OPH}\} \quad [12c].$$

Note that using the results of Cases 3 and 4 produced equation [12] which bears great resemblance to the more accurate expression in [11]. One strategy for dealing with cascadability is to design a FIFO with "flat"  $t_{VSIRL}$ ,  $t_{VSORL}$ ,  $t_{(R)IDS}$ , etc., characteristics. This eliminates the dependence on signal phase, and  $f_{MAX}$  can be expressed exactly as:

$$1/f_{MAX} = \max\{t_{IRL} + t_{ORH}, t_{ORL} + t_{IRH}\} \quad [13].$$

Such a strategy provides a more reliable cascade interface, and is well worth the price of a lower  $f_{MAX}$ .

It should be noted that the natural frequency at each operating condition (VCC, temperature) is unique, and is the limiting frequency regardless of how it is approached, whether by fallthrough or by bubbleback. Consider the following figure.



**Figure 12. Approach of  $f_{MAX}$  from Fallthrough**

Let us say that the natural frequency of the cascade interface between A and B is 10 MHz. Data is shifted at low frequency into A, and falls through to B, until B is one-half full. The two-device buffer is then operated for a while with the input, output, and interface working at 5 MHz.

Then, the input and output frequencies are raised to, say, 15 MHz. Immediately thereafter, the composite buffer will continue to function, since the input and output circuitry of a FIFO

## Cascadability Issues in Advanced Micro Devices' Shallow FIFOs

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can usually operate at frequencies above the natural frequency. The cascade interface, however, will be limited to a rate of 10 MHz. Eventually, the bottom part will empty, and the top part will fill. A cascade limited bottleneck occurs, limiting the overall throughput rate to 10 MHz. Data words from the 15 MHz input stream will be intermittently read at a 10 MHz rate, causing a loss of data.

At some point in time between the frequency increase and the bottlenecking, there will be five or so words in the top part, and twenty-seven or so (half of 64, minus 5) words in the bottom part. The FIFOs will no longer be in fallthrough mode, since there is more than one word in the upstream part, and more than one vacancy in the downstream part. The natural frequency mode will have been entered, and the interface will carry data as fast as possible.

A similar example can be drawn for these FIFOs, with the composite buffer initially three-fourths filled. Eventually, the top part will fill and the bottom part will empty. At some point in between, the FIFOs will no longer be in bubbleback mode, but in the natural frequency mode, because there will exist more

than one vacancy in the downstream part and more than one word in the upstream part. The overall steady state throughput rate will again be limited to 10 MHz.

In each of the above cases, the composite buffer went from either fallthrough or bubbleback mode to the natural frequency mode (where both parts were neither full nor empty), then on to an interface limited natural frequency mode, subject to throughput-related errors.

Regardless from which direction the natural frequency was approached, this frequency must be unique since it represents the case where the upstream part contains more than one word and where the downstream part contains more than one vacancy. When this happens the interface has no dependence on what is happening at the system input and output ports and shifts data across it at the maximum possible rate.

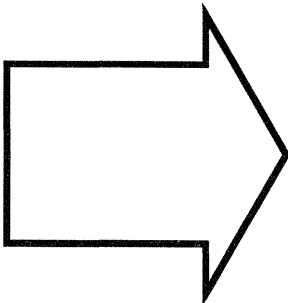
The maximum operating frequency of a cascaded FIFO must therefore be specified lower than the worst-case natural frequency in order to avoid asynchronously induced bottleneck errors.

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Advanced  
Micro  
Devices



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Advanced Micro Devices is preparing an ExpressROM™ Data Book containing preliminary specification on these important products. It is scheduled to be printed in June 1989. Then, you can secure a copy from your local sales office, authorized representative or favorite distributor.  
Ask for the Express ROM Data Book, number 12100A.



# Am27C64

8,192 x 8-Bit CMOS EPROM

## DISTINCTIVE CHARACTERISTICS

- Fast access time — 55 ns
- Low power consumption:
  - 100  $\mu$ A maximum standby current
- Programming voltage: 12.5 V
- Single +5-V power supply
- JEDEC-approved pinout
- $\pm 10\%$  power supply tolerance available
- One-Time Programmable (OTP) Flashrite™ programming
- Latch-up protected to 100 mA from  $-1$  V to  $V_{CC} + 1$  V

## GENERAL DESCRIPTION

The Am27C64 is a 64K-bit, ultraviolet erasable programmable read-only memory. It is organized as 8,192 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

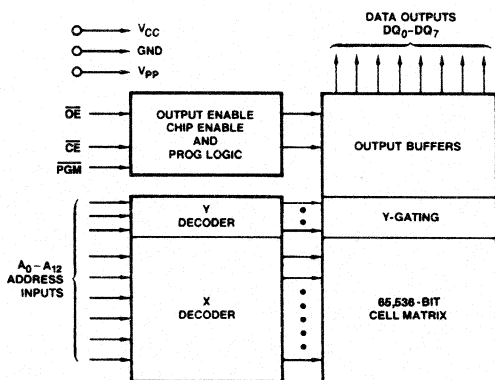
Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C64 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus

eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C64 supports AMD's interactive programming algorithm (1-ms pulses) resulting in typical programming times of less than two minutes.

## BLOCK DIAGRAM



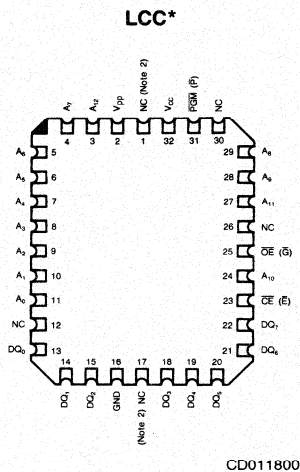
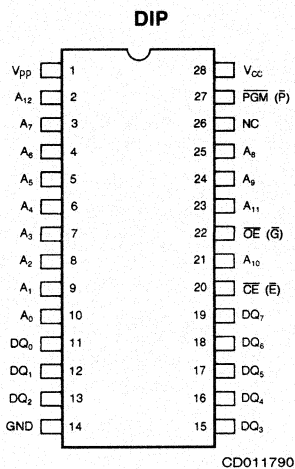
BD000219

## PRODUCT SELECTOR GUIDE

Family Part No.	Am27C64							
Ordering Part No:								
$\pm 5\%$ $V_{CC}$ Tolerance	-55	-75	-95	-125	-155	-205	-255	-305
$\pm 10\%$ $V_{CC}$ Tolerance	-	-70	-90	-120	-150	-200	-250	-300
Max. Access Time (ns)	55	70	90	120	150	200	250	300
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	55	70	90	120	150	200	250	300
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	35	40	40	50	65	75	100	120



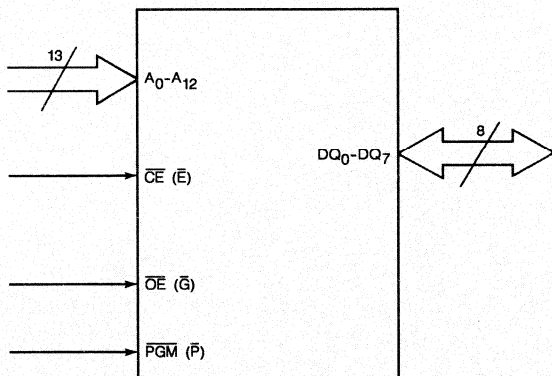
## CONNECTION DIAGRAMS Top View



Notes: 1. JEDEC nomenclature is in parentheses.  
2. Don't use (DU) for PLCC.

\* Also available in 32-pin rectangular plastic leaded chip carrier.

## LOGIC SYMBOL



LS003350

## PIN DESCRIPTION

$A_0 - A_{12}$	= Address Inputs
$\overline{CE} (\overline{E})$	= Chip Enable Input
$DQ_0 - DQ_7$	= Data Inputs/Outputs
$\overline{OE} (\overline{G})$	= Output Enable Input
$\overline{PGM} (\overline{F})$	= Program Enable Input
$V_{CC}$	= $V_{CC}$ Supply Voltage
$V_{PP}$	= Program Supply Voltage
GND	= Ground
NC	= No Internal Connection
DU	= No External Connection

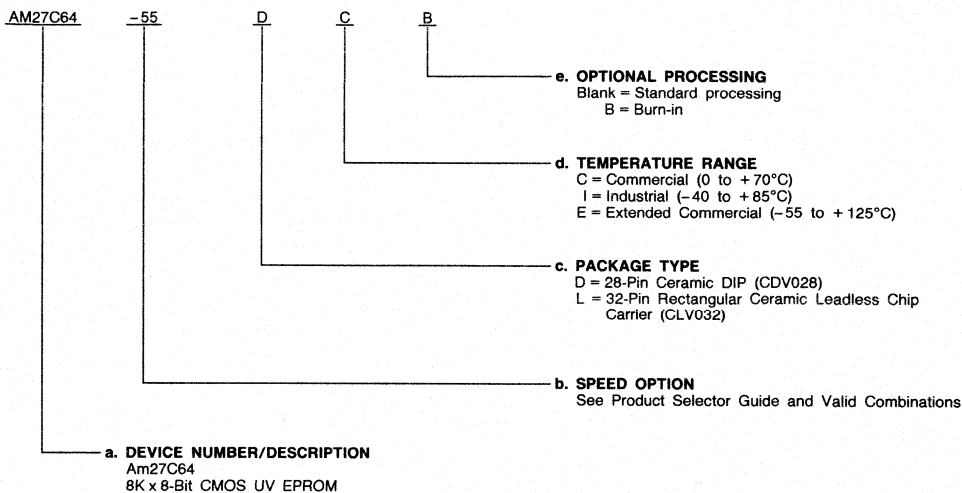


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27C64-55	DC, DCB, LC, LCB
AM27C64-70	
AM27C64-75	
AM27C64-95	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C64-125	
AM27C64-155	
AM27C64-205	
AM27C64-255	
AM27C64-305	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C64-90	
AM27C64-120	
AM27C64-150	
AM27C64-200	
AM27C64-250	
AM27C64-300	

### Valid Combinations

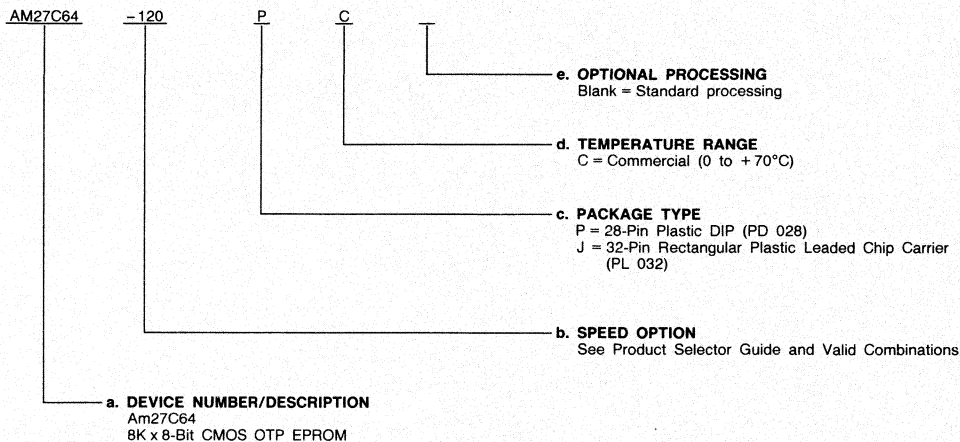
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION (Cont'd.)

### OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number**
- b. Speed Option**
- c. Package Type**
- d. Temperature Range**
- e. Optional Processing**



Valid Combinations	
AM27C64-120	JC, PC
AM27C64-125	
AM27C64-150	
AM27C64-155	
AM27C64-200	
AM27C64-205	
AM27C64-250	
AM27C64-255	
AM27C64-300	
AM27C64-305	

#### Valid Combinations

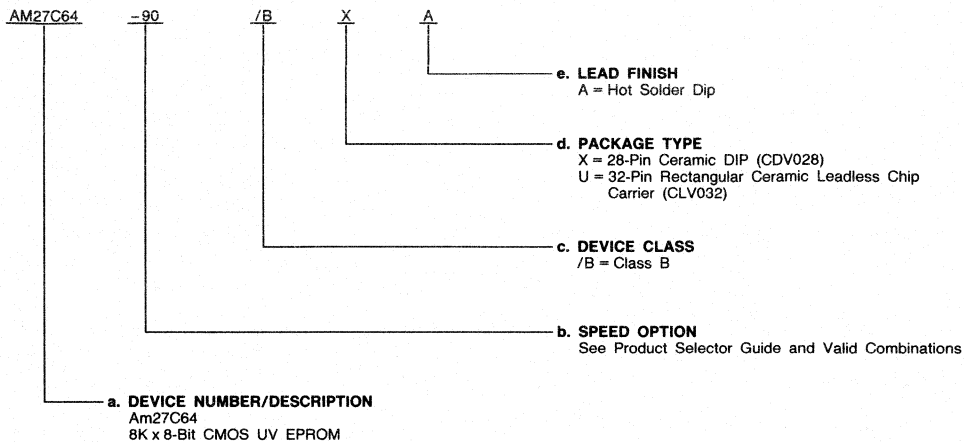
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option**
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27C64-90	/BXA, /BUA
AM27C64-120	
AM27C64-150	
AM27C64-200	
AM27C64-250	
AM27C64-300	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

**3**

## FUNCTIONAL DESCRIPTION

### Erasing the Am27C64

In order to clear all locations of your programmed contents, it is necessary to expose the Am27C64 to an ultraviolet light source. A dosage of 15 W seconds/cm<sup>2</sup> is required to completely erase an Am27C64. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm<sup>2</sup> for 15 to 20 minutes. The Am27C64 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C64, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C64 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

### Programming the Am27C64

Upon delivery, or after each erasure, the Am27C64 has all 65,336 bits in the "ONE", or HIGH state. "ZEROS" are loaded into the Am27C64 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the V<sub>pp</sub> pin,  $\overline{CE}$  is at V<sub>IL</sub>, and PGM is at V<sub>IL</sub>.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The flowchart in Figure 1 shows AMD's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C64. This part of the algorithm is done at V<sub>CC</sub> = 6.0 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at V<sub>CC</sub> = 5 V ± 5%.

### Flashrite

The OTP EPROM Flashrite programming algorithm (shown in Figure 2) reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the OTP EPROM.

The Flashrite programming algorithm programs and verifies at V<sub>CC</sub> = 6.25 V and V<sub>pp</sub> = 12.75 V. After the final address is completed, all bytes are compared to the original data with V<sub>CC</sub> = V<sub>pp</sub> = 5.25 V.

### Program Inhibit

Programming of multiple Am27C64s in parallel with different data is also easily accomplished. Except for  $\overline{CE}$ , all like inputs of the parallel Am27C64 may be common. A TTL low-level program pulse applied to an Am27C64 PGM input with V<sub>pp</sub> = 12.5 ± 0.5 V and  $\overline{CE}$  LOW will program that Am27C64. A high-level  $\overline{CE}$  input inhibits the other Am27C64s from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with  $\overline{OE}$  and  $\overline{CE}$  at V<sub>IL</sub>, PGM at V<sub>IH</sub>, and V<sub>pp</sub> between 12.0 V to 13.0 V.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C64.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A<sub>9</sub> of the Am27C64. Two identifier bytes may then be sequenced from the device outputs by toggling address line A<sub>0</sub> from V<sub>IL</sub> to V<sub>IH</sub>. All other address lines must be held at V<sub>IL</sub> during auto select mode.

Byte 0 (A<sub>0</sub> = V<sub>IL</sub>) represents the manufacturer code, and byte 1 (A<sub>0</sub> = V<sub>IH</sub>), the device identifier code. For the Am27C64, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ<sub>7</sub>) defined as the parity bit.

### Read Mode

The Am27C64 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t<sub>ACC</sub>) is equal to the delay from  $\overline{CE}$  to output (t<sub>CE</sub>). Data is available at the outputs t<sub>OE</sub> after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least t<sub>ACC</sub> - t<sub>OE</sub>.

### Standby Mode

The Am27C64 has a CMOS standby mode which reduces the maximum V<sub>CC</sub> current to 100 μA. It is placed in CMOS-standby when  $\overline{CE}$  is at V<sub>CC</sub> ± 0.3 V. The Am27C64 also has a TTL-standby mode which reduces the maximum V<sub>CC</sub> current to 1.0 mA. It is placed in TTL-standby when  $\overline{CE}$  is at V<sub>IH</sub>. When in standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V<sub>CC</sub> and GND to minimize transient effects. In

addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7- $\mu$ F bulk electrolytic capacitor should be used

between  $V_{CC}$  and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

**MODE SELECT TABLE**

Pins								
Mode		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	$A_0$	$A_9$	$V_{PP}$	Outputs
Read		$V_{IL}$	$V_{IL}$	X	X	X	$V_{CC}$	DOUT
Output Disable		$V_{IL}$	$V_{IH}$	X	X	X	$V_{CC}$	High Z
Standby (TTL)		$V_{IH}$	X	X	X	X	$V_{CC}$	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	$V_{CC}$	High Z
Program		$V_{IL}$	X	$V_{IL}$	X	X	$V_{PP}$	DIN
Program Verify		$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$	DOUT
Program Inhibit		$V_{IH}$	X	X	X	X	$V_{PP}$	High Z
Auto Select (Note 3)	Manufacturer Code	$V_{IL}$	$V_{IL}$	X	$V_{IL}$	$V_H$	$V_{CC}$	01H
	Device Code	$V_{IL}$	$V_{IL}$	X	$V_{IH}$	$V_H$	$V_{CC}$	15H

Notes:1. X can be either  $V_{IL}$  or  $V_{IH}$

2.  $V_H = 12.0$  V  $\pm$  0.5 V

3.  $A_1$ - $A_8 = A_{10} - A_{12} = V_{IL}$

4. See DC Programming Characteristics for  $V_{PP}$  voltage during programming.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	-65 to +125°C
All Other Products	-65 to +150°C
Ambient Temperature	
with Power Applied	-55 to +125°C
Voltage with Respect to Ground:	
All pins except $A_g$ , $V_{PP}$ , and $V_{CC}$	-0.6 to $V_{CC} + 0.5$ V
$A_g$ and $V_{PP}$	-0.6 to 13.5 V
$V_{CC}$	-0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

- Notes: 1. Minimum DC voltage on input or I/O is -0.5 V. During transitions, the inputs may undershoot GND to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O is  $V_{CC} + 0.5$  V which may overshoot to  $V_{CC} + 2.0$  V for periods up to 20 ns.
2. For  $A_g$  and  $V_{PP}$  the minimum DC input is -0.5 V. During transitions,  $A_g$  and  $V_{PP}$  may undershoot GND to -2.0 V for periods of up to 20 ns.  $A_g$  and  $V_{PP}$  must not exceed 13.5 V for any period of time.

## OPERATING RANGES

Commercial (C) Devices	
Case Temperature ( $T_C$ )	0 to +70°C
Industrial (I) Devices	
Case Temperature ( $T_C$ )	-40 to +85°C
Extended Commercial (E) Devices	
Case Temperature ( $T_C$ )	-55 to +125°C
Military (M) Devices	
Case Temperature ( $T_C$ )	-55 to +125°C
Supply Read Voltages:	
$V_{CC}/V_{PP}$ for Am27C64-XX5	+4.75 to +5.25 V
$V_{CC}/V_{PP}$ for Am27C64-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

### TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400$ $\mu$ A		2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1$ mA			0.45	V
$V_{IH}$	Input HIGH Voltage			2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage			-0.3	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0$ V to $V_{CC}$	C/I Devices		1.0	$\mu$ A
			E/M Devices		5.0	
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0$ V to $V_{CC}$	C/I Devices		10	$\mu$ A
			E/M Devices		10	
$I_{CC1}$	$V_{CC}$ Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$ , $f = 5$ MHz, $I_{OUT} = 0$ mA (Open Outputs)	C/I Devices		30	mA
			E/M Devices		50	
$I_{CC2}$	$V_{CC}$ Standby Current (Note 9)	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$	C/I Devices		1.0	mA
			E/M Devices		1.0	
$I_{PP1}$	$V_{PP}$ Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$ , $V_{PP} = V_{CC}$			100	$\mu$ A

### CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400$ $\mu$ A		2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1$ mA			0.45	V
$V_{IH}$	Input HIGH Voltage			$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage			-0.3	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0$ V to $V_{CC}$	C/I Devices		1.0	$\mu$ A
			E/M Devices		5.0	

## DC CHARACTERISTICS over operating range unless otherwise specified (Cont'd.)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>	C/I Devices		10	μA
			E/M Devices		10	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$ , f = 5 MHz, I <sub>OUT</sub> = 0 mA (Open Outputs)	C/I Devices		25	mA
			E/M Devices		25	
I <sub>CC2</sub>	V <sub>CC</sub> Standby Current (Note 9)	$\overline{CE} = V_{CC} \pm 0.3$ V	C/I Devices		100	μA
			E/M Devices		120	
I <sub>PP1</sub>	V <sub>PP</sub> Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$ , V <sub>PP</sub> = V <sub>CC</sub>			100	μA

## CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C <sub>IN1</sub>	Address Input Capacitance	V <sub>IN</sub> = 0 V	8	12	pF
C <sub>IN2</sub>	$\overline{OE}$ Input Capacitance	V <sub>IN</sub> = 0 V	12	20	pF
C <sub>IN3</sub>	$\overline{CE}$ Input Capacitance	V <sub>IN</sub> = 0 V	9	12	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0 V	8	12	pF

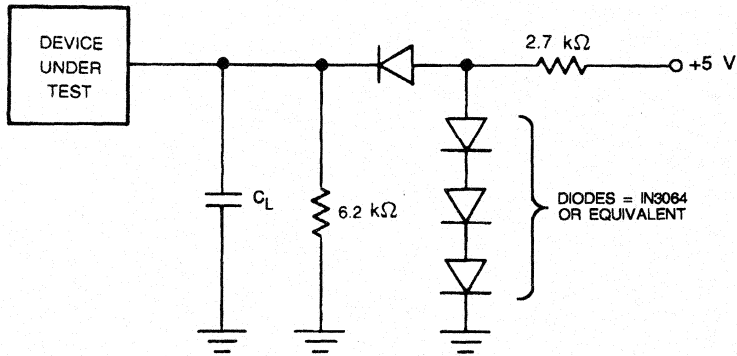
- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.  
 2. Typical values are for nominal supply voltages.  
 3. This parameter is only sampled and not 100% tested.  
 4. **Caution:** The Am27C64 must not be removed from, or inserted into, a socket or board when V<sub>PP</sub> or V<sub>CC</sub> is applied.  
 5. I<sub>CC1</sub> is tested with  $\overline{OE} = V_{IH}$  to simulate open outputs.  
 6. Maximum active power usage is the sum of I<sub>CC</sub> and I<sub>PP</sub>.  
 7. T<sub>A</sub> = 25°C, f = 1 MHz.  
 8. Minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> + 0.5 V which may overshoot to V<sub>CC</sub> + 2.0 V for periods less than 20 ns.  
 9. For Am27C64-305, I<sub>CC1</sub> = 50mA, I<sub>CC2</sub> (TTL) = 5mA, I<sub>CC2</sub> (CMOS) = 500 μA, and I<sub>PP1</sub> (Read) = 1mA maximum.

## SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions	Am27C64							Unit	
JEDEC	Standard			-55	-70, -75	-90, -95	-120, -125	-150, -155	-200, -205	-250, -255		-300, -305
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.								ns
				Max.	55	70	90	120	150	200	250	
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.								ns
				Max.	55	70	90	120	150	200	250	
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.								ns
				Max.	35	40	40	50	65	75	100	
t <sub>EHQZ</sub> , t <sub>GHQZ</sub>	t <sub>DF</sub>	Output Enable HIGH to Output Float (Note 2)		Min.								ns
				Max.	25	25	25	35	50	55	60	
t <sub>AXQX</sub>	t <sub>OH</sub>	Output Hold from Addresses, $\overline{CE}$ , or $\overline{OE}$ , whichever occurred first		Min.	0	0	0	0	0	0	0	ns
				Max.								

- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.  
 2. This parameter is only sampled and not 100% tested.  
 3. **Caution:** The Am27C64 must not be removed from, or inserted into, a socket or board when V<sub>PP</sub> or V<sub>CC</sub> is applied.  
 4. For the -55, -70, and -75:  
 Output Load: 1 TTL gate and C<sub>L</sub> = 30 pF,  
 Input Rise and Fall Times: 20 ns,  
 Input Pulse Levels: 0 to 3 V,  
 Timing Measurement Reference Level: 1.5 V for inputs and outputs.  
 For all other versions:  
 Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF,  
 Input Rise and Fall Times: 20 ns,  
 Input Pulse Levels: 0.45 to 2.4 V,  
 Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

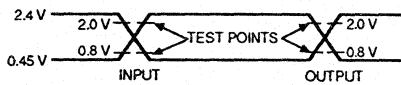
### SWITCHING TEST CIRCUIT



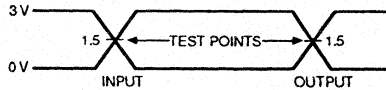
TC003193

$C_L = 100 \text{ pF}$  including jig capacitance (30 pF for -55, -70, and -75)

### SWITCHING TEST WAVEFORMS



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are  $\leq 20 \text{ ns}$ .



11419-001A






WF026840

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are  $\leq 20 \text{ ns}$  for -55, -70, and -75 devices.

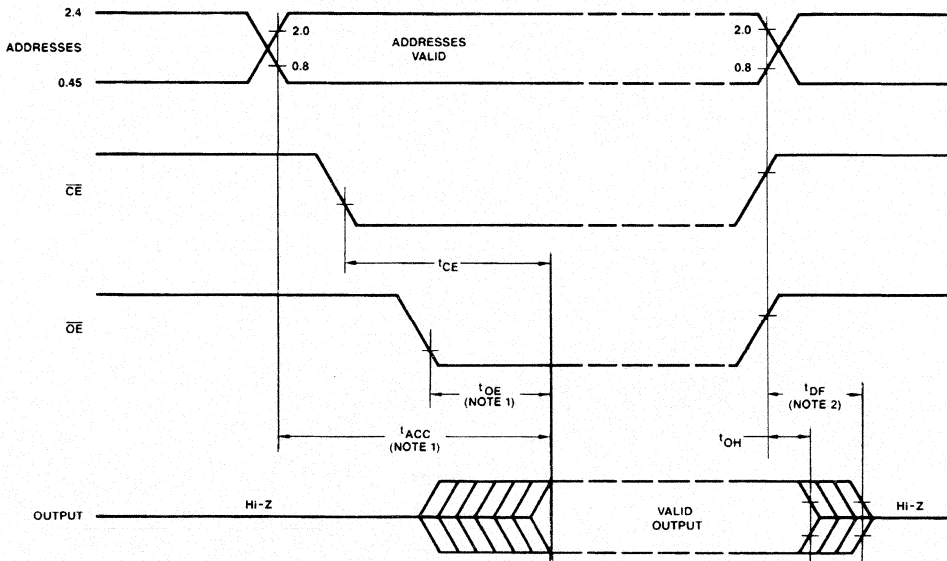


## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

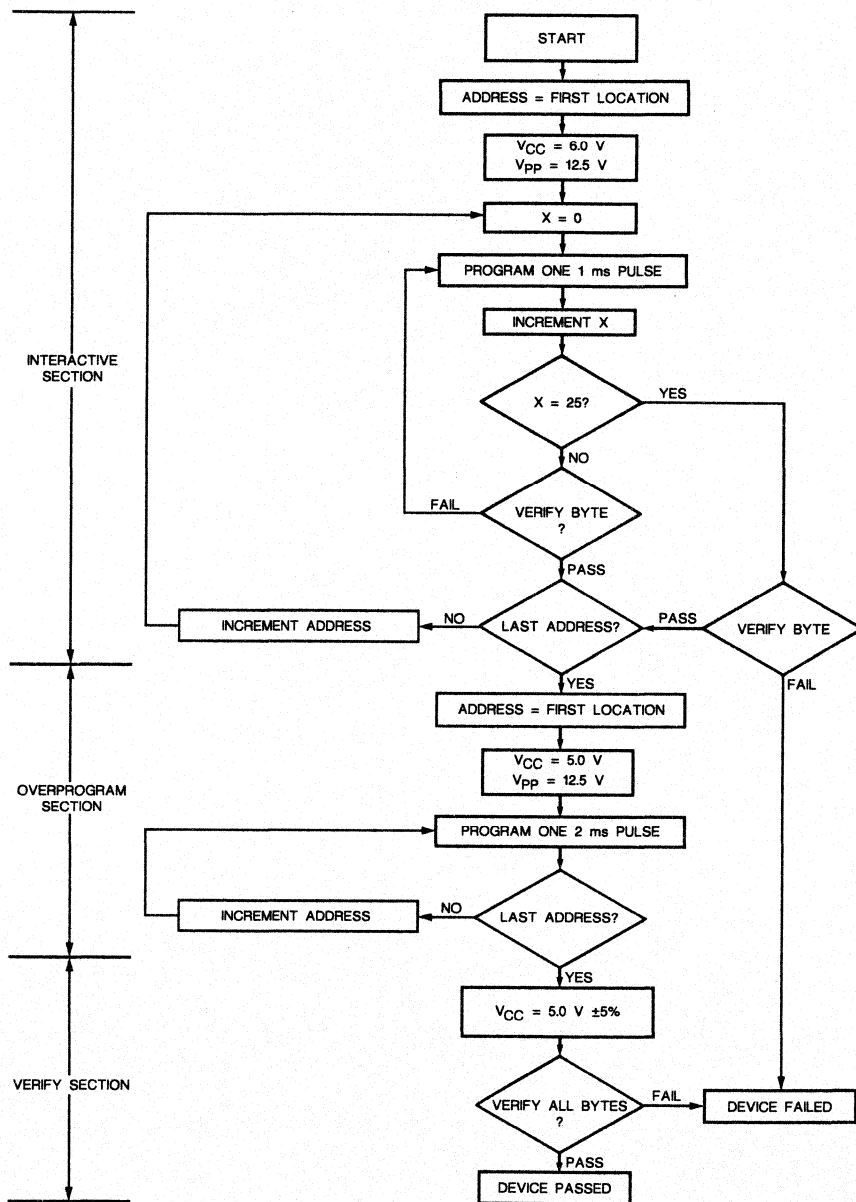


WF001323

- Notes: 1.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .  
 2.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.

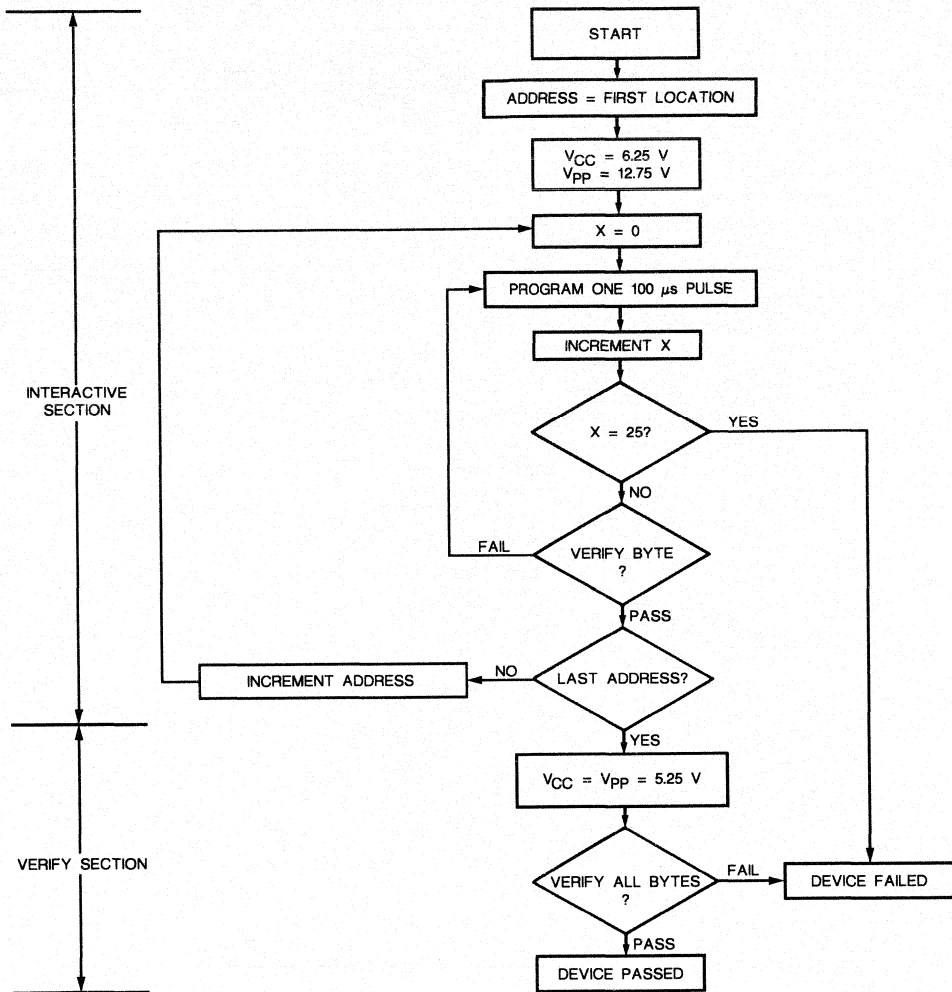
3

## PROGRAMMING FLOW CHARTS



PF002840

Figure 1. Interactive Programming Flow Chart



10205B-008A

PF002490

Figure 2. Flashrite Programming Flow Chart for OTP EPROM

## DC PROGRAMMING CHARACTERISTICS (T<sub>A</sub> = +25°C ±5°C) (Notes 1, 2, & 3).

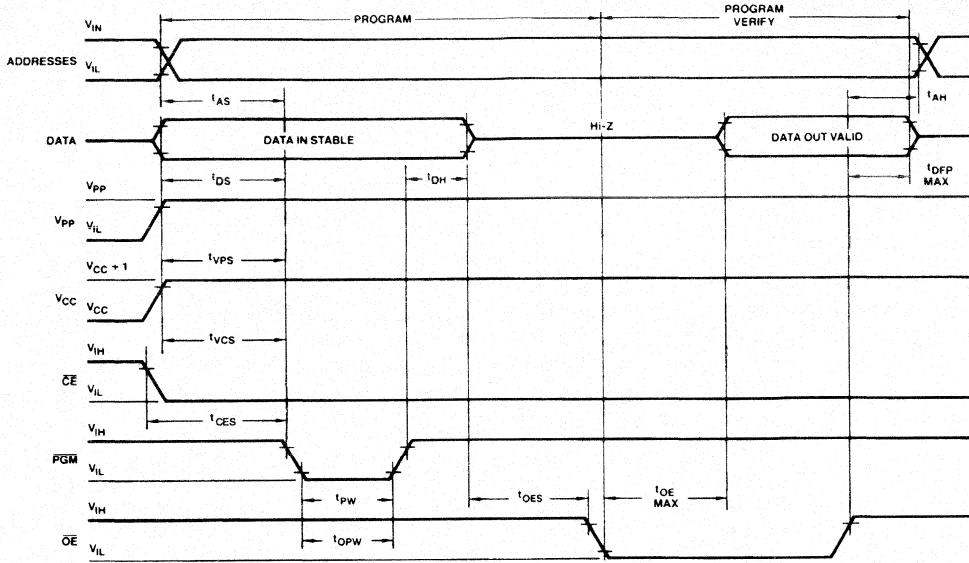
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I <sub>LI</sub>	Input Current (All Inputs)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>		10.0	μA
V <sub>IL</sub>	Input LOW Level (All Inputs)		-0.3	0.8	V
V <sub>IH</sub>	Input HIGH Level		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output LOW Voltage During Verify	I <sub>OL</sub> = 2.1 mA		0.45	V
V <sub>OH</sub>	Output HIGH Voltage During Verify	I <sub>OH</sub> = -400 μA	2.4		V
V <sub>H</sub>	A <sub>9</sub> Auto Select Voltage		11.5	12.5	V
I <sub>CC3</sub>	V <sub>CC</sub> Supply Current (Program & Verify)			50	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current (Program)	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$		30	mA
V <sub>CC1</sub>	Interactive Supply Voltage		5.75	6.25	V
V <sub>PP1</sub>	Interactive Programming Voltage		12.0	13.0	V
V <sub>CC2</sub>	Flashrite Supply Voltage		6.00	6.50	V
V <sub>PP2</sub>	Flashrite Programming Voltage		12.5	13.0	V

## SWITCHING PROGRAMMING CHARACTERISTICS (T<sub>A</sub> = +25°C ±5°C) (Notes 1, 2, & 3).

Parameter Symbols		Parameter Description	Min.	Max.	Unit	
JEDEC	Standard					
t <sub>AVEL</sub>	t <sub>AS</sub>	Address Setup Time	2		μs	
t <sub>DZGL</sub>	t <sub>OES</sub>	$\overline{OE}$ Setup Time	2		μs	
t <sub>ELPL</sub>	t <sub>CES</sub>	$\overline{CE}$ Setup Time	2		μs	
t <sub>DVEL</sub>	t <sub>DS</sub>	Data Setup Time	2		μs	
t <sub>GHAX</sub>	t <sub>AH</sub>	Address Hold Time	0		μs	
t <sub>EHDX</sub>	t <sub>DH</sub>	Data Hold Time	2		μs	
t <sub>GHQZ</sub>	t <sub>DFP</sub>	Output Enable to Output Float Delay	0	130	ns	
t <sub>VPS</sub>	t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	2		μs	
t <sub>ELEH1</sub>	t <sub>PW</sub>	$\overline{PGM}$ Program Pulse Width	Flashrite	95	105	μs
			Interactive	0.95	1.05	ms
t <sub>ELEH2</sub>	t <sub>OPW</sub>	$\overline{PGM}$ Overprogram Pulse Width (Interactive)	1.95	2.05	ms	
t <sub>VCS</sub>	t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	2		μs	
t <sub>GLQV</sub>	t <sub>OE</sub>	Data Valid from $\overline{OE}$		150	ns	

- Notes:**
1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.
  2. When programming the Am27C64, a 0.1-μF capacitor is required across V<sub>PP</sub> and ground to suppress spurious voltage transients which may damage the device.
  3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

**PROGRAMMING ALGORITHM WAVEFORMS (Notes 1 & 2)**



WF000555

- Notes: 1. The input timing reference level is 0.8 V for  $V_{IL}$  and 2 V for  $V_{IH}$ .  
 2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device, but must be accommodated by the programmer.

# Am27C128

16,384 x 8-Bit CMOS EPROM



## DISTINCTIVE CHARACTERISTICS

- Fast access time — 55 ns
- Low power consumption:
  - 100  $\mu$ A maximum standby current
- Programming voltage: 12.5 V
- Single +5-V power supply
- JEDEC-approved pinout
- $\pm 10\%$  power supply tolerance available
- One-Time Programmable (OTP) Flashrite™ programming
- Latch-up protected to 100 mA from  $-1$  V to  $V_{CC} + 1$  V

## GENERAL DESCRIPTION

The Am27C128 is a 128K-bit, ultraviolet erasable programmable read-only memory. It is organized as 16,384 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

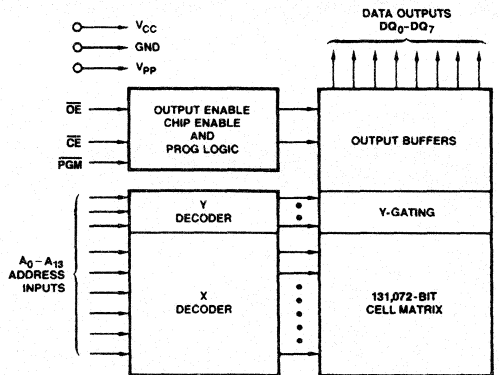
Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C128 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus

eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C128 supports AMD's interactive programming algorithm (1-ms pulses) resulting in typical programming times of less than two minutes.

## BLOCK DIAGRAM

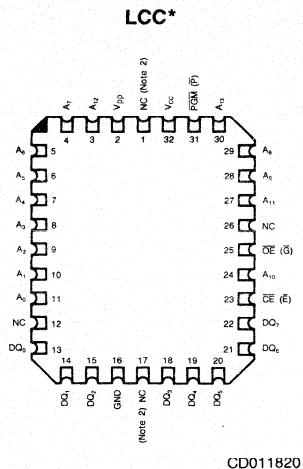
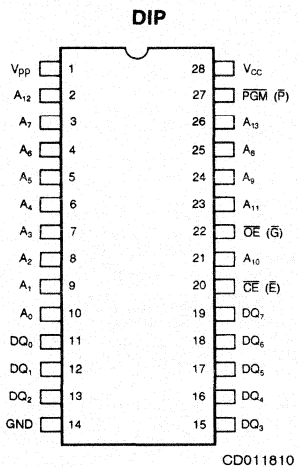


BD008360

## PRODUCT SELECTOR GUIDE

Family Part No.	Am27C128							
Ordering Part No:								
±5% $V_{CC}$ Tolerance	-55	-75	-95	-125	-155	-205	-255	-305
±10% $V_{CC}$ Tolerance	-	-70	-90	-120	-150	-200	-250	-300
Max. Access Time (ns)	55	70	90	120	150	200	250	300
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	55	70	90	120	150	200	250	300
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	35	40	40	50	65	75	100	120

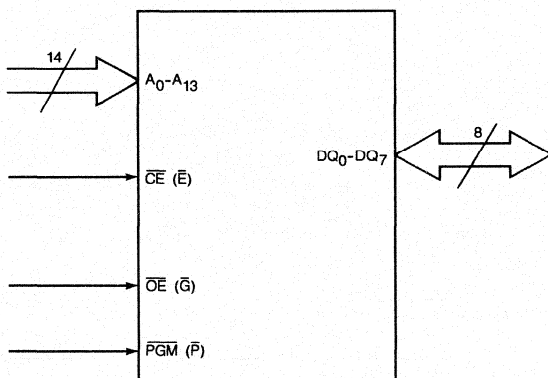
## CONNECTION DIAGRAMS Top View



Notes: 1. JEDEC nomenclature is in parentheses  
2. Don't use (DU) for PLCC.

\* Also available in 32-pin rectangular plastic leaded chip carrier.

## LOGIC SYMBOL



LS003360

## PIN DESCRIPTION

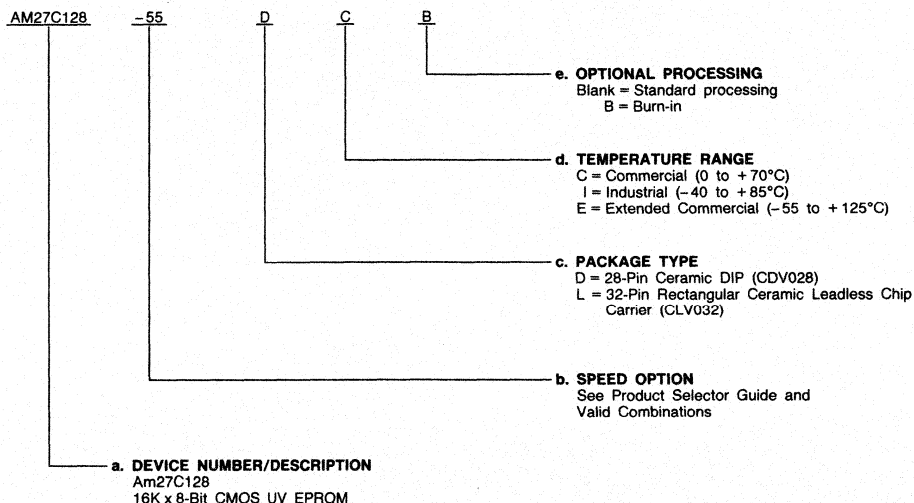
$A_0 - A_{13}$	=	Address Inputs
$\overline{CE} (\overline{E})$	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Inputs/Outputs
$\overline{OE} (\overline{G})$	=	Output Enable Input
$\overline{PGM} (\overline{F})$	=	Program Enable Input
$V_{CC}$	=	$V_{CC}$ Supply Voltage
$V_{PP}$	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27C128-55	DC, DCB, LC, LCB
AM27C128-70	
AM27C128-75	
AM27C128-95	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C128-125	
AM27C128-155	
AM27C128-205	
AM27C128-255	
AM27C128-305	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C128-90	
AM27C128-120	
AM27C128-150	
AM27C128-200	
AM27C128-250	
AM27C128-300	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

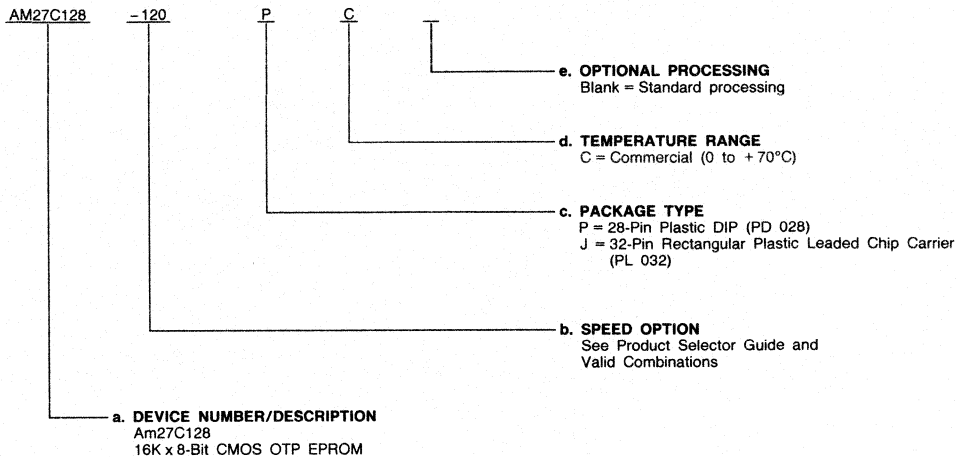


## ORDERING INFORMATION (Cont'd.)

### OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option**
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM27C128-120	JC, PC
AM27C128-125	
AM27C128-150	
AM27C128-155	
AM27C128-200	
AM27C128-205	
AM27C128-250	
AM27C128-255	
AM27C128-300	
AM27C128-305	

#### Valid Combinations

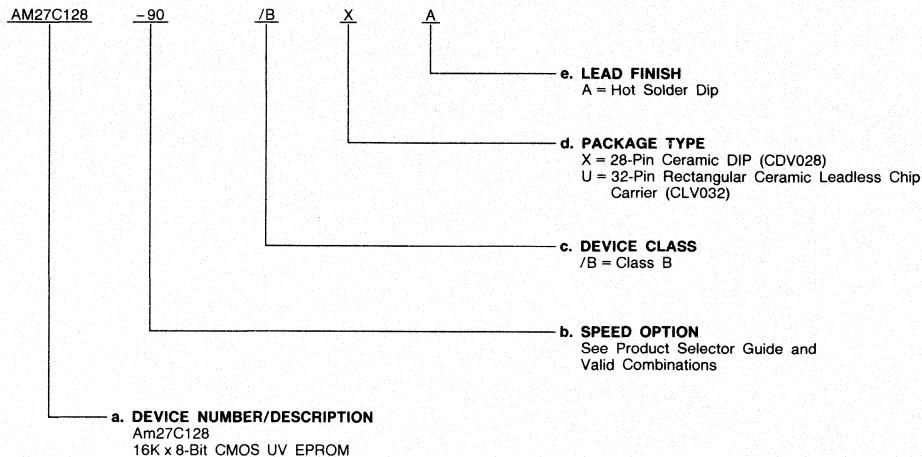
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option**
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27C128-90	/BXA, /BUA
AM27C128-120	
AM27C128-150	
AM27C128-200	
AM27C128-250	
AM27C128-300	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## FUNCTIONAL DESCRIPTION

### Erasing the Am27C128

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C128 to an ultraviolet light source. A dosage of 15 W seconds/cm<sup>2</sup> is required to completely erase an Am27C128. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm<sup>2</sup> for 15 to 20 minutes. The Am27C128 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C128, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C128 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

### Programming the Am27C128

Upon delivery, or after each erasure, the Am27C128 has all 131,072 bits in the "ONE", or HIGH state. "ZEROS" are loaded into the Am27C128 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the V<sub>PP</sub> pin,  $\overline{CE}$  is at V<sub>IL</sub>, and PGM is at V<sub>IL</sub>.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The flowchart in Figure 1 shows AMD's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C128. This part of the algorithm is done at V<sub>CC</sub> = 6.0 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at V<sub>CC</sub> = 5 V ± 5%.

### Flashrite

The OTP EPROM Flashrite programming algorithm (shown in Figure 2) reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the OTP EPROM.

The Flashrite programming algorithm programs and verifies at V<sub>CC</sub> = 6.25 V and V<sub>PP</sub> = 12.75 V. After the final address is completed, all bytes are compared to the original data with V<sub>CC</sub> = V<sub>PP</sub> = 5.25 V.

### Program Inhibit

Programming of multiple Am27C128s in parallel with different data is also easily accomplished. Except for  $\overline{CE}$ , all like inputs of the parallel Am27C128 may be common. A TTL low-level program pulse applied to an Am27C128 PGM input with V<sub>PP</sub> = 12.5 ± 0.5 V and  $\overline{CE}$  LOW will program that Am27C128.

A high-level  $\overline{CE}$  input inhibits the other Am27C128s from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with  $\overline{OE}$  and  $\overline{CE}$  at V<sub>IL</sub>, PGM at V<sub>IH</sub>, and V<sub>PP</sub> between 12.0 V to 13.0 V.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C128.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A<sub>9</sub> of the Am27C128. Two identifier bytes may then be sequenced from the device outputs by toggling address line A<sub>0</sub> from V<sub>IL</sub> to V<sub>IH</sub>. All other address lines must be held at V<sub>IL</sub> during auto select mode.

Byte 0 (A<sub>0</sub> = V<sub>IL</sub>) represents the manufacturer code, and byte 1 (A<sub>0</sub> = V<sub>IH</sub>), the device identifier code. For the Am27C128, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ<sub>7</sub>) defined as the parity bit.

### Read Mode

The Am27C128 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t<sub>ACC</sub>) is equal to the delay from  $\overline{CE}$  to output (t<sub>CE</sub>). Data is available at the outputs t<sub>OE</sub> after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least t<sub>ACC</sub> - t<sub>OE</sub>.

### Standby Mode

The Am27C128 has a CMOS standby mode which reduces the maximum V<sub>CC</sub> current to 100 μA. It is placed in CMOS-standby when  $\overline{CE}$  is at V<sub>CC</sub> ± 0.3 V. The Am27C128 also has a TTL-standby mode which reduces the maximum V<sub>CC</sub> current to 1.0 mA. It is placed in TTL-standby when  $\overline{CE}$  is at V<sub>IH</sub>. When in standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-μF ceramic capacitor (high

3

frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM

arrays, a 4.7- $\mu$ F bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

**MODE SELECT TABLE**

Pins								
		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	$A_0$	$A_9$	$V_{PP}$	Outputs
Read		$V_{IL}$	$V_{IL}$	X	X	X	$V_{CC}$	D <sub>OUT</sub>
Output Disable		$V_{IL}$	$V_{IH}$	X	X	X	$V_{CC}$	High Z
Standby (TTL)		$V_{IH}$	X	X	X	X	$V_{CC}$	High Z
Standby (CMOS)		$V_{CC} \pm 0.3 V$	X	X	X	X	$V_{CC}$	High Z
Program		$V_{IL}$	X	$V_{IL}$	X	X	$V_{PP}$	D <sub>IN</sub>
Program Verify		$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$	D <sub>OUT</sub>
Program Inhibit		$V_{IH}$	X	X	X	X	$V_{PP}$	High Z
Auto Select (Notes 3 & 4)	Manufacturer Code	$V_{IL}$	$V_{IL}$	X	$V_{IL}$	$V_H$	$V_{CC}$	01H
	Device Code	$V_{IL}$	$V_{IL}$	X	$V_{IH}$	$V_H$	$V_{CC}$	16H

Notes: 1. X can be either  $V_{IL}$  or  $V_{IH}$

2.  $V_H = 12.0 V \pm 0.5 V$

3.  $A_1 - A_8 = A_{10} - A_{12} = V_{IL}$

4.  $A_{13} = X$

5. See DC Programming characteristics for  $V_{PP}$  voltage during programming.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	-65 to +125°C
All Other Products	-65 to +150°C
Ambient Temperature	
with Power Applied	-55 to +125°C
Voltage with Respect to Ground:	
All pins except $A_9$ , $V_{PP}$ , and	
$V_{CC}$	-0.6 to $V_{CC} + 0.5$ V
$A_9$ and $V_{PP}$	-0.6 to 13.5 V
$V_{CC}$	-0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

- Notes: 1. Minimum DC voltage on input or I/O is -0.5 V. During transitions, the inputs may undershoot GND to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O is  $V_{CC} + 0.5$  V which may overshoot to  $V_{CC} + 2.0$  V for periods up to 20 ns.
2. For  $A_9$  and  $V_{PP}$  the minimum DC input is -0.5 V. During transitions,  $A_9$  and  $V_{PP}$  may undershoot GND to -2.0 V for periods of up to 20 ns.  $A_9$  and  $V_{PP}$  must not exceed 13.5 V for any period of time.

## OPERATING RANGES

Commercial (C) Devices	
Case Temperature ( $T_C$ )	0 to +70°C
Industrial (I) Devices	
Case Temperature ( $T_C$ )	-40 to +85°C
Extended Commercial (E) Devices	
Case Temperature ( $T_C$ )	-55 to +125°C
Military (M) Devices	
Case Temperature ( $T_C$ )	-55 to +125°C
Supply Read Voltage:	
$V_{CC}/V_{PP}$ for Am27C128-XX5	+4.75 to +5.25 V
$V_{CC}/V_{PP}$ for Am27C128-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

### TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400 \mu A$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage		-0.3	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0 \text{ V to } V_{CC}$		1.0	$\mu A$
				5.0	
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0 \text{ V to } V_{CC}$		10	$\mu A$
				10	
$I_{CC1}$	$V_{CC}$ Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$ , $f = 5 \text{ MHz}$ , $I_{OUT} = 0 \text{ mA}$ (Open Outputs)		30	mA
				50	
$I_{CC2}$	$V_{CC}$ Standby Current (Note 9)	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$		1.0	mA
				1.0	
$I_{PP1}$	$V_{PP}$ Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$ , $V_{PP} = V_{CC}$		100	$\mu A$

### CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400 \mu A$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{IH}$	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage		-0.3	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0 \text{ V to } V_{CC}$		1.0	$\mu A$
				5.0	

## DC CHARACTERISTICS over operating range unless otherwise specified (Cont'd.)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>	C/I Devices	10	μA
			E/M Devices	10	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$ , f = 5 MHz, I <sub>OUT</sub> = 0 mA (Open Outputs)	C/I Devices	25	mA
			E/M Devices	25	
I <sub>CC2</sub>	V <sub>CC</sub> Standby Current (Note 9)	$\overline{CE} = V_{CC} \pm 0.3$ V	C/I Devices	100	μA
			E/M Devices	120	
I <sub>PP1</sub>	V <sub>PP</sub> Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$ , V <sub>PP</sub> = V <sub>CC</sub>		100	μA

## CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C <sub>IN1</sub>	Address Input Capacitance	V <sub>IN</sub> = 0 V	8	12	pF
C <sub>IN2</sub>	$\overline{OE}$ Input Capacitance	V <sub>IN</sub> = 0 V	12	20	pF
C <sub>IN3</sub>	$\overline{CE}$ Input Capacitance	V <sub>IN</sub> = 0 V	9	12	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0 V	8	12	pF

- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.  
 2. Typical values are for nominal supply voltages.  
 3. This parameter is only sampled and not 100% tested.  
 4. **Caution:** The Am27C128 must not be removed from, or inserted into, a socket or board when V<sub>PP</sub> or V<sub>CC</sub> is applied.  
 5. I<sub>CC1</sub> is tested with  $\overline{OE} = V_{IH}$  to simulate open outputs.  
 6. Maximum active power usage is the sum of I<sub>CC</sub> and I<sub>PP</sub>.  
 7. T<sub>A</sub> = 25°C, f = 1 MHz.  
 8. Minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> + 0.5 V which may overshoot to V<sub>CC</sub> + 2.0 V for periods less than 20 ns.  
 9. For Am27C128-305, I<sub>CC1</sub> = 50mA, I<sub>CC2</sub> (TTL) = 5mA, I<sub>CC2</sub> (CMOS) = 500μA, and I<sub>PP1</sub> (Read) = 1mA maximum.

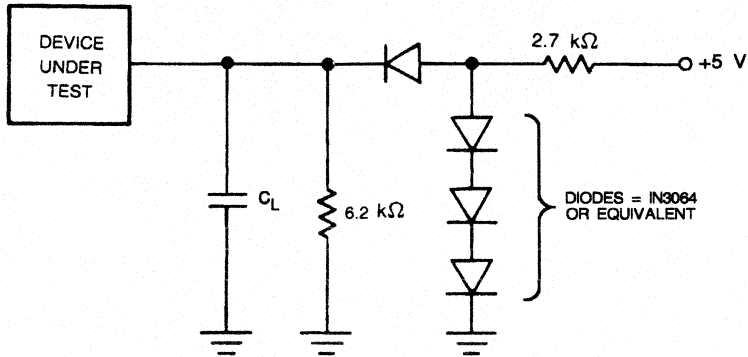
## SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions	Am27C128									Unit
JEDEC	Standard			-55	-70, -75	-90, -95	-120, -125	-150, -155	-200, -205	-250, -255	-300, -305		
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.									ns
				Max.	55	70	90	120	150	200	250	300	
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.									ns
				Max.	55	70	90	120	150	200	250	300	
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.									ns
				Max.	35	40	40	50	65	75	100	120	
t <sub>EHQZ</sub> , t <sub>GHQZ</sub>	t <sub>DF</sub>	Output Enable HIGH to Output Float (Note 2)		Min.									ns
				Max.	25	25	25	35	50	55	60	75	
t <sub>AXQX</sub>	t <sub>OH</sub>	Output Hold from Addresses, $\overline{CE}$ , or $\overline{OE}$ , whichever occurred first		Min.	0	0	0	0	0	0	0	0	ns
				Max.									

- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.  
 2. This parameter is only sampled and not 100% tested.  
 3. **Caution:** The Am27C128 must not be removed from, or inserted into, a socket or board when V<sub>PP</sub> or V<sub>CC</sub> is applied.  
 4. For the -55, -70, -75:  
 Output Load: 1 TTL gate and C<sub>L</sub> = 30 pF,  
 Input Rise and Fall Times: 20 ns,  
 Input Pulse Levels: 0 to 3 V,  
 Timing Measurement Reference Level -1.5 V inputs and outputs.

For all other Versions:  
 Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF,  
 Input Rise and Fall Times: 20 ns,  
 Input Pulse Levels: 0.45 to 2.4 V,  
 Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

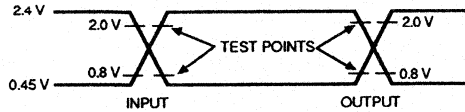
### SWITCHING TEST CIRCUIT



TC003193

$C_L = 100$  pF including jig capacitance (30 pF for -55, -70, and -75)

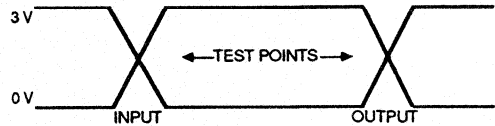
### SWITCHING TEST WAVEFORMS



11420-001A

WF026820

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are  $\leq 20$  ns.








11420-002A

WF026830

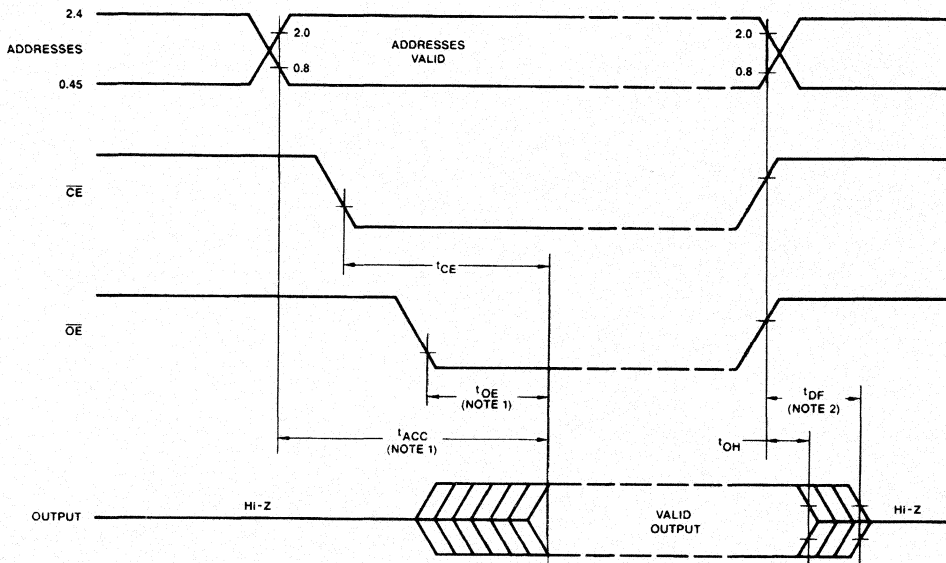
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are  $\leq 20$  ns for -55, -70, and -75 devices.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

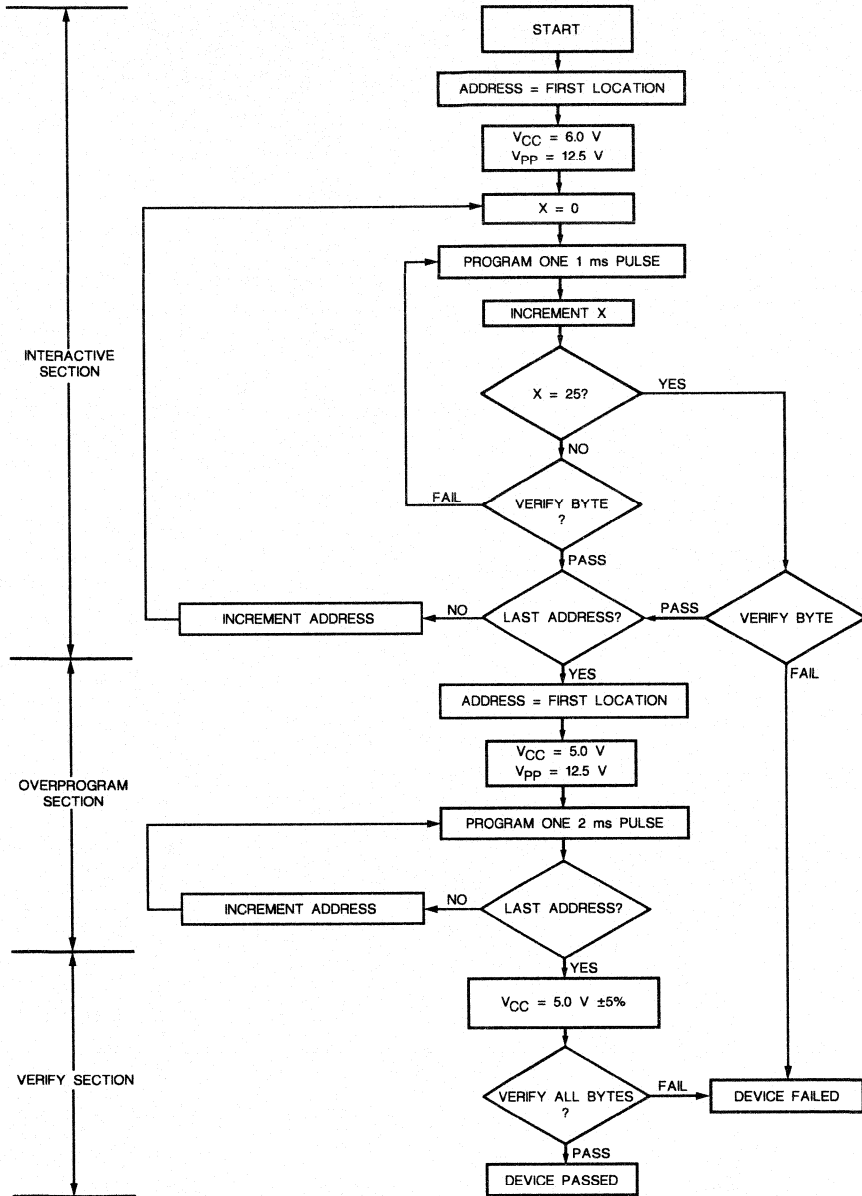


WF001324

- Notes: 1.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .  
 2.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.

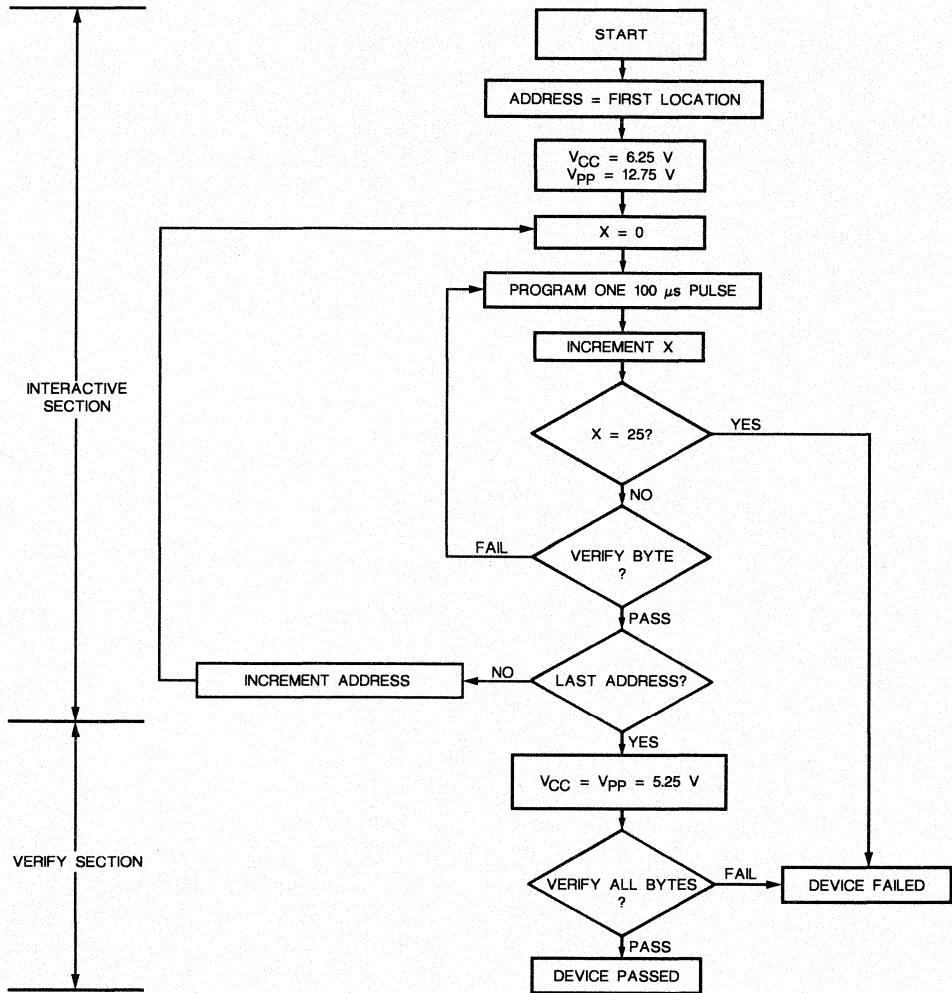


# PROGRAMMING FLOW CHARTS



PF002840

Figure 1. Interactive Programming Flow Chart



10205B-008A

PF002490

Figure 2. Flashrite Programming Flow Chart for OTP EPROM

## DC PROGRAMMING CHARACTERISTICS ( $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ ) (Notes 1, 2, & 3).

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$I_{LI}$	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or $V_{IH}$		10.0	$\mu\text{A}$
$V_{IL}$	Input LOW Level (All Inputs)		-0.3	0.8	V
$V_{IH}$	Input HIGH Level		2.0	$V_{CC} + 0.5$	V
$V_{OL}$	Output LOW Voltage During Verify	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{OH}$	Output HIGH Voltage During Verify	$I_{OH} = -400 \mu\text{A}$	2.4		V
$V_H$	$A_g$ Auto Select Voltage		11.5	12.5	V
$I_{CC3}$	$V_{CC}$ Supply Current (Program & Verify)			50	mA
$I_{PP2}$	$V_{PP}$ Supply Current (Program)	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$		30	mA
$V_{CC1}$	Interactive Supply Voltage		5.75	6.25	V
$V_{PP1}$	Interactive Programming Voltage		12.0	13.0	V
$V_{CC2}$	Flashrite Supply Voltage		6.00	6.50	V
$V_{PP2}$	Flashrite Programming Voltage		12.5	13.0	V

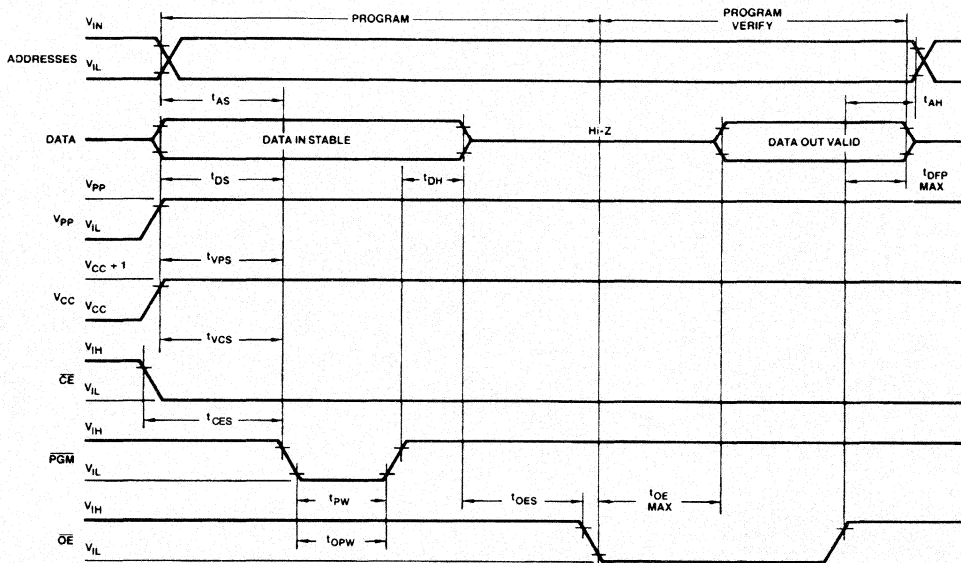
## SWITCHING PROGRAMMING CHARACTERISTICS ( $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ ) (Notes 1, 2, & 3).

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
$t_{AVEL}$	$t_{AS}$	Address Setup Time	2		$\mu\text{s}$
$t_{DZGL}$	$t_{OES}$	$\overline{OE}$ Setup Time	2		$\mu\text{s}$
$t_{ELPL}$	$t_{CES}$	$\overline{CE}$ Setup Time	2		$\mu\text{s}$
$t_{DVEL}$	$t_{DS}$	Data Setup Time	2		$\mu\text{s}$
$t_{GHAX}$	$t_{AH}$	Address Hold Time	0		$\mu\text{s}$
$t_{EHDX}$	$t_{DH}$	Data Hold Time	2		$\mu\text{s}$
$t_{GHQZ}$	$t_{DFP}$	Output Enable to Output Float Delay	0	130	ns
$t_{VPS}$	$t_{VPS}$	$V_{PP}$ Setup Time	2		$\mu\text{s}$
$t_{ELEH1}$	$t_{PW}$	Flashrite	95	105	$\mu\text{s}$
		Interactive	0.95	1.05	$\mu\text{s}$
$t_{ELEH2}$	$t_{OPW}$	PGM Overprogram Pulse Width (Interactive)	1.95	2.05	ms
$t_{VCS}$	$t_{VCS}$	$V_{CC}$ Setup Time	2		$\mu\text{s}$
$t_{GLQV}$	$t_{OE}$	Data Valid from $\overline{OE}$		150	ns

- Notes:**
- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$ , and removed simultaneously or after  $V_{PP}$ .
  - When programming the Am27C128, a 0.1- $\mu\text{F}$  capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients which may damage the device.
  - Programming characteristics are sampled but not 100% tested at worst-case conditions.

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## PROGRAMMING ALGORITHM WAVEFORMS (Notes 1 & 2)



WF000555

- Notes: 1. The input timing reference level is 0.8 V for V<sub>IL</sub> and 2 V for V<sub>IH</sub>.  
 2. t<sub>OE</sub> and t<sub>DFP</sub> are characteristics of the device, but must be accommodated by the programmer.

# Am27C256

32,768 x 8-Bit CMOS EPROM

## DISTINCTIVE CHARACTERISTICS

- Fast access time — 55 ns
- Low power consumption:
  - 100  $\mu$ A maximum standby current
- Programming voltage: 12.5 V
- Single +5-V power supply
- JEDEC-approved pinout
- $\pm 10\%$  power supply tolerance available
- One-Time Programmable (OTP) Flashrite™ programming
- Latch-up protected to 100 mA from  $-1$  V to  $V_{CC} + 1$  V

## GENERAL DESCRIPTION

The Am27C256 is a 256K-bit, ultraviolet erasable programmable read-only memory. It is organized as 32,768 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

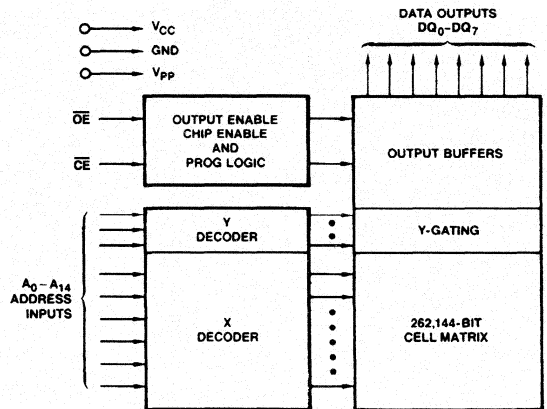
Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C256 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus

eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C256 supports AMD's interactive programming algorithm (1-ms pulses) resulting in typical programming times of less than two minutes.

## BLOCK DIAGRAM



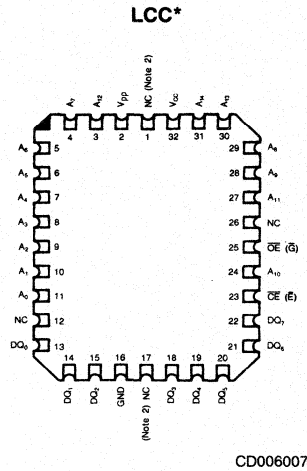
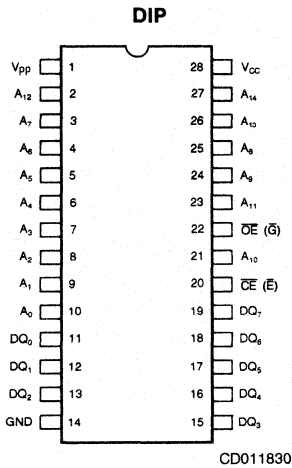
BD000214

3

## PRODUCT SELECTOR GUIDE

Family Part No.	Am27C256									
Ordering Part No:										
$\pm 5\% V_{CC}$ Tolerance	-55	-75	-95	-105	-125	-155	-175	-205	-255	-305
$\pm 10\% V_{CC}$ Tolerance	-	-70	-90	-100	-120	-150	-170	-200	-250	-300
Max. Access Time (ns)	55	70	90	100	120	150	170	200	250	300
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	55	70	90	100	120	150	170	200	250	300
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	35	40	40	40	50	65	70	75	100	120

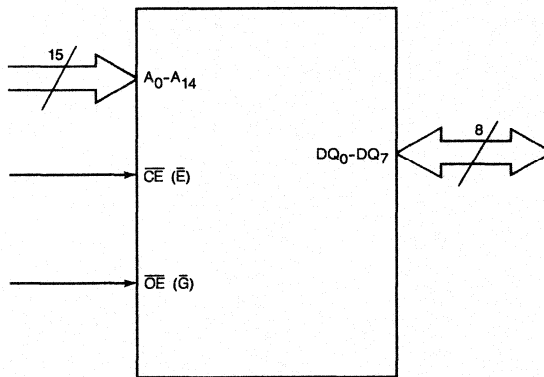
## CONNECTION DIAGRAMS Top View



Notes: 1. JEDEC nomenclature is in parentheses.  
2. Don't use (DU) for PLCC.

\* Also available in 32-pin rectangular plastic leaded chip carrier.

## LOGIC SYMBOL



LS002297

## PIN DESCRIPTION

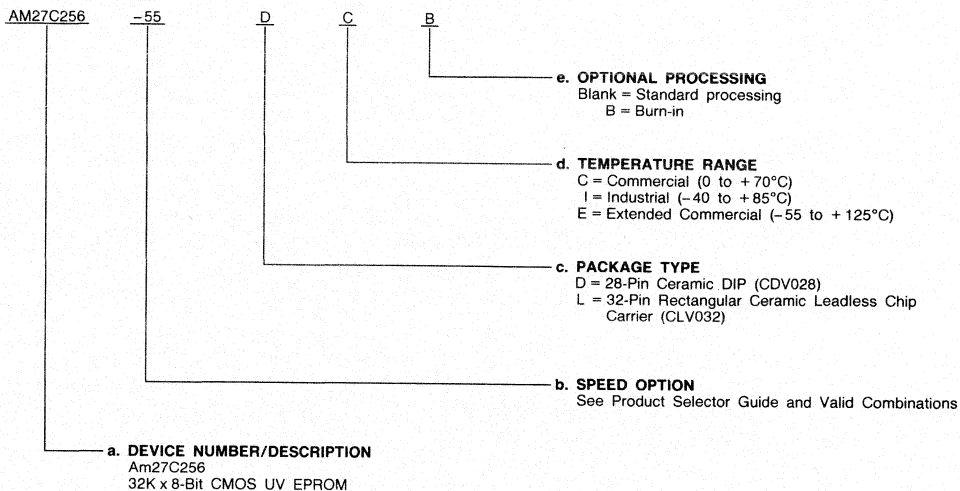
$A_0 - A_{14}$	= Address Inputs
$\overline{CE} (\overline{E})$	= Chip Enable Input
$DQ_0 - DQ_7$	= Data inputs/Outputs
$\overline{OE} (\overline{G})$	= Output Enable Input
$V_{CC}$	= $V_{CC}$ Supply Voltage
$V_{PP}$	= Program Supply Voltage
GND	= Ground
NC	= No Internal Connection
DU	= No External Connection

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27C256-55	DC, DCB, LC, LCB
AM27C256-70	
AM27C256-75	
AM27C256-95	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C256-105	
AM27C256-125	
AM27C256-155	
AM27C256-175	
AM27C256-205	
AM27C256-255	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C256-305	
AM27C256-90	
AM27C256-100	
AM27C256-120	
AM27C256-150	
AM27C256-170	
AM27C256-200	
AM27C256-250	
AM27C256-300	

### Valid Combinations

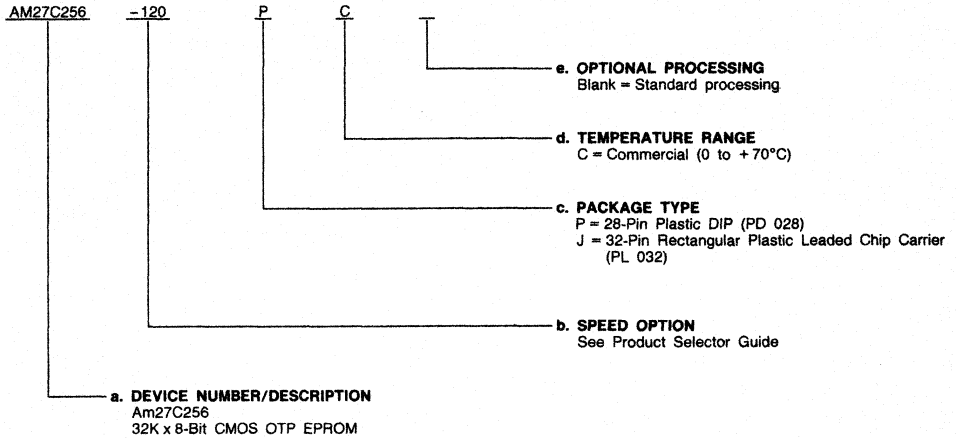
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION (Cont'd.)

### OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27C256-120	JC, PC
AM27C256-125	
AM27C256-150	
AM27C256-155	
AM27C256-170	
AM27C256-175	
AM27C256-200	
AM27C256-205	
AM27C256-250	
AM27C256-255	
AM27C256-300	
AM27C256-305	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

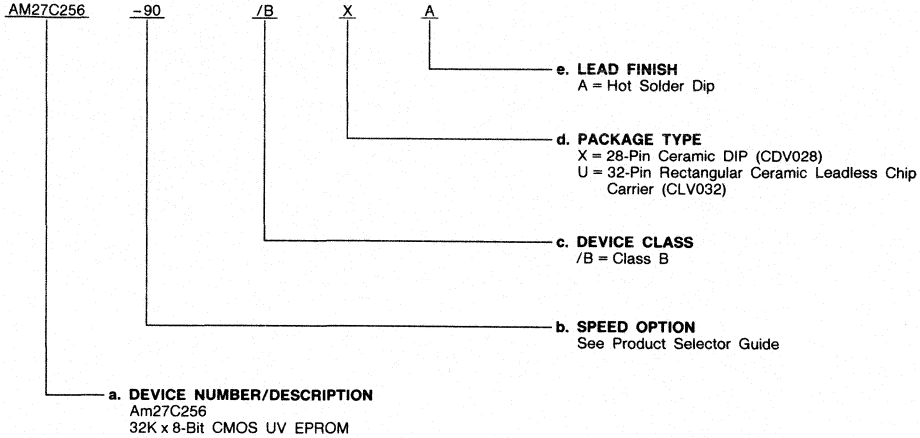


# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option**
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27C256-90	/BXA, /BUA
AM27C256-100	
AM27C256-120	
AM27C256-150	
AM27C256-170	
AM27C256-200	
AM27C256-250	
AM27C256-300	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## FUNCTIONAL DESCRIPTION

### Erasing the Am27C256

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C256 to an ultraviolet light source. A dosage of 15 W seconds/cm<sup>2</sup> is required to completely erase an Am27C256. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm<sup>2</sup> for 15 to 20 minutes. The Am27C256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C256, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

### Programming the Am27C256

Upon delivery, or after each erasure, the Am27C256 has all 262,144 bits in the "ONE", or HIGH state. "ZEROS" are loaded into the Am27C256 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the V<sub>PP</sub> pin,  $\overline{OE}$  is at V<sub>IH</sub>, and  $\overline{CE}$  is at V<sub>IL</sub>.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The flowchart in Figure 1 shows AMD's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C256. This part of the algorithm is done at V<sub>CC</sub> = 6.0 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at V<sub>CC</sub> = 5 V ± 5%.

### Flashrite

The OTP EPROM Flashrite programming algorithm (shown in Figure 2) reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the OTP EPROM.

The Flashrite programming algorithm programs and verifies at V<sub>CC</sub> = 6.25 V and V<sub>PP</sub> = 12.75 V. After the final address is completed, all bytes are compared to the original data with V<sub>CC</sub> = V<sub>PP</sub> = 5.25 V.

### Program Inhibit

Programming of multiple Am27C256s in parallel with different data is also easily accomplished. Except for  $\overline{CE}$ , all like inputs of the parallel Am27C256 may be common. A TTL low-level program pulse applied to an Am27C256  $\overline{CE}$  input with V<sub>PP</sub> = 12.5 ± 0.5 V and  $\overline{OE}$  HIGH will program that

Am27C256. A high-level  $\overline{CE}$  input inhibits the other Am27C256s from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with  $\overline{OE}$  at V<sub>IL</sub>,  $\overline{CE}$  at V<sub>IH</sub>, and V<sub>PP</sub> between 12.0 V to 13.0 V.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C256.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A<sub>G</sub> of the Am27C256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A<sub>0</sub> from V<sub>IL</sub> to V<sub>IH</sub>. All other address lines must be held at V<sub>IL</sub> during auto select mode.

Byte 0 (A<sub>0</sub> = V<sub>IL</sub>) represents the manufacturer code, and byte 1 (A<sub>0</sub> = V<sub>IH</sub>), the device identifier code. For the Am27C256, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ<sub>7</sub>) defined as the parity bit.

### Read Mode

The Am27C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t<sub>ACC</sub>) is equal to the delay from  $\overline{CE}$  to output (t<sub>CE</sub>). Data is available at the outputs t<sub>OE</sub> after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least t<sub>ACC</sub> - t<sub>OE</sub>.

### Standby Mode

The Am27C256 has a CMOS standby mode which reduces the maximum V<sub>CC</sub> current to 100 μA. It is placed in CMOS-standby when  $\overline{CE}$  is at V<sub>CC</sub> ± 0.3 V. The Am27C256 also has a TTL-standby mode which reduces the maximum V<sub>CC</sub> current to 1.0 mA. It is placed in TTL-standby when  $\overline{CE}$  is at V<sub>IH</sub>. When in standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-μF ceramic capacitor (high

frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM

arrays, a 4.7- $\mu$ F bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

**MODE SELECT TABLE**

Pins		Pins					Outputs
		$\overline{CE}$	$\overline{OE}$	$A_0$	$A_9$	$V_{PP}$	
Read		$V_{IL}$	$V_{IL}$	X	X	$V_{CC}$	$D_{OUT}$
Output Disable		$V_{IL}$	$V_{IH}$	X	X	$V_{CC}$	High Z
Standby (TTL)		$V_{IH}$	X	X	X	$V_{CC}$	High Z
Standby (CMOS)		$V_{CC} \pm 0.3 V$	X	X	X	$V_{CC}$	High Z
Program		$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$	$D_{IN}$
Program Verify		$V_{IH}$	$V_{IL}$	X	X	$V_{PP}$	$D_{OUT}$
Program Inhibit		$V_{IH}$	$V_{IH}$	X	X	$V_{PP}$	High Z
Auto Select (Notes 3 & 4)	Manufacturer Code	$V_{IL}$	$V_{IL}$	$V_{IL}$	$V_H$	$V_{CC}$	01 H
	Device Code	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_H$	$V_{CC}$	10 H

- Notes: 1. X can be either  $V_{IL}$  or  $V_{IH}$   
 2.  $V_H = 12.0 V \pm 0.5 V$   
 3.  $A_1 - A_8 = A_{10} - A_{12} = V_{IL}$   
 4.  $A_{13}$  and  $A_{14} = X$   
 5. See DC Programming characteristics for  $V_{PP}$  voltage during programming.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
OTP Products	-65 to +125°C
All Other Products	-65 to +150°C
Ambient Temperature	
with Power Applied	-55 to +125°C
Voltage with Respect to Ground:	
All pins except $A_g$ , $V_{pp}$ , and	
$V_{CC}$	-0.6 to $V_{CC} + 0.5$ V
$A_g$ and $V_{pp}$	-0.6 to 13.5 V
$V_{CC}$	-0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

- Notes: 1. Minimum DC voltage on input or I/O is -0.5 V. During transitions, the inputs may undershoot GND to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O is  $V_{CC} + 0.5$  V which may overshoot to  $V_{CC} + 2.0$  V for periods up to 20 ns.
2. For  $A_g$  and  $V_{pp}$  the minimum DC input is -0.5 V. During transitions,  $A_g$  and  $V_{pp}$  may undershoot GND to -2.0 V for periods of up to 20 ns.  $A_g$  and  $V_{pp}$  must not exceed 13.5 V for any period of time.

## OPERATING RANGES

Commercial (C) Devices	
Case Temperature ( $T_C$ )	0 to +70°C
Industrial (I) Devices	
Case Temperature ( $T_C$ )	-40 to +85°C
Extended Commercial (E) Devices	
Case Temperature ( $T_C$ )	-55 to +125°C
Military (M) Devices	
Case Temperature ( $T_C$ )	-55 to +125°C
Supply Read Voltage:	
$V_{CC}/V_{pp}$ for Am27C256-XX5	+4.75 to +5.25 V
$V_{CC}/V_{pp}$ for Am27C256-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

### TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400 \mu A$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage		-0.3	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0$ V to $V_{CC}$	C/I Devices	1.0	$\mu A$
			E/M Devices	5.0	
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0$ V to $V_{CC}$	C/I Devices	10	$\mu A$
			E/M Devices	10	
$I_{CC1}$	$V_{CC}$ Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$ , $f = 5$ MHz, $I_{OUT} = 0$ mA (Open Outputs)	C/I Devices	30	mA
			E/M Devices	50	
$I_{CC2}$	$V_{CC}$ Standby Current (Note 9)	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$	C/I Devices	1.0	mA
			E/M Devices	1.0	
$I_{PP1}$	$V_{pp}$ Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$ , $V_{pp} = V_{CC}$		100	$\mu A$

### CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400 \mu A$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
$V_{IH}$	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage		-0.3	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0$ V to $V_{CC}$	C/I Devices	1.0	$\mu A$
			E/M Devices	5.0	

## DC CHARACTERISTICS over operating range unless otherwise specified (Cont'd.)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>	C/I Devices	10	μA
			E/M Devices	10	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$ , f = 5 MHz, I <sub>OUT</sub> = 0 mA (Open Outputs)	C/I Devices	25	mA
			E/M Devices	25	
I <sub>CC2</sub>	V <sub>CC</sub> Standby Current (Note 9)	$\overline{CE} = V_{CC} \pm 0.3$ V	C/I Devices	100	μA
			E/M Devices	120	
I <sub>PP1</sub>	V <sub>PP</sub> Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$ , V <sub>PP</sub> = V <sub>CC</sub>		100	μA

## CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C <sub>IN1</sub>	Address Input Capacitance	V <sub>IN</sub> = 0 V	8	12	pF
C <sub>IN2</sub>	$\overline{OE}$ Input Capacitance	V <sub>IN</sub> = 0 V	12	20	pF
C <sub>IN3</sub>	$\overline{CE}$ Input Capacitance	V <sub>IN</sub> = 0 V	9	12	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0 V	8	12	pF

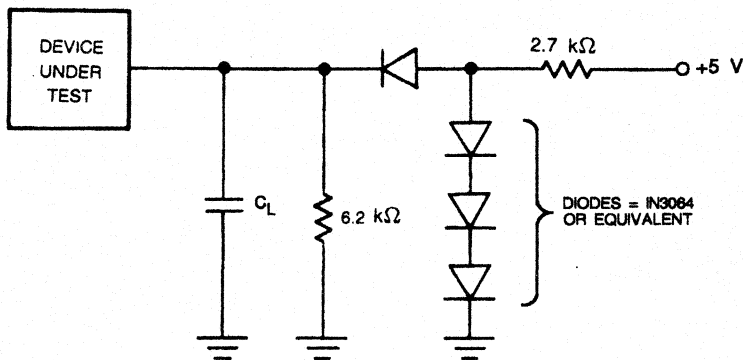
- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.  
2. Typical values are for nominal supply voltages.  
3. This parameter is only sampled and not 100% tested.  
4. **Caution:** The Am27C256 must not be removed from, or inserted into, a socket or board when V<sub>PP</sub> or V<sub>CC</sub> is applied.  
5. I<sub>CC1</sub> is tested with  $\overline{OE} = V_{IH}$  to simulate open outputs.  
6. Maximum active power usage is the sum of I<sub>CC</sub> and I<sub>PP</sub>.  
7. T<sub>A</sub> = 25°C, f = 1 MHz.  
8. Minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> + 0.5 V which may overshoot to V<sub>CC</sub> + 2.0 V for periods less than 20 ns.  
9. For Am27C256-305, I<sub>CC1</sub> = 50 mA, I<sub>CC2</sub>(TTL) = 5 mA, I<sub>CC2</sub>(CMOS) = 500 μA and I<sub>PP1</sub>(Read) = 1 mA maximum.

## SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbols		Parameter Description	Test Conditions	Am27C256										Unit								
JEDEC	Standard			-55	-70	-75	-90	-95	-100	-105	-120	-125	-150		-155	-170	-175	-200	-205	-250	-255	-300
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.																		ns
				Max.	55	70	90	100	120	150	170	200	250	300								
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.																		ns
				Max.	55	70	90	100	120	150	170	200	250	300								
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.																		ns
				Max.	35	40	40	40	50	65	70	75	100	120								
t <sub>EHQZ</sub> , t <sub>GHQZ</sub>	t <sub>DF</sub>	Output Enable HIGH to Output Float (Note 2)		Min.																		ns
				Max.	25	25	25	30	35	50	50	55	60	75								
t <sub>AXQX</sub>	t <sub>OH</sub>	Output Hold from Addresses, $\overline{CE}$ , or $\overline{OE}$ , whichever occurred first		Min.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ns
				Max.																		

- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.  
2. This parameter is only sampled and not 100% tested.  
3. **Caution:** The Am27C256 must not be removed from, or inserted into, a socket or board when V<sub>PP</sub> or V<sub>CC</sub> is applied.  
4. For the -55, -70, and -75:  
Output Load: 1 TTL gate and C<sub>L</sub> = 30 pF,  
Input Rise and Fall Times: 20 ns,  
Input Pulse Levels: 0 to 3 V,  
Timing Measurement Reference Level: 1.5 V for inputs and outputs.  
For all other versions:  
Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF,  
Input Rise and Fall Times: 20 ns  
Input Pulse Levels: 0.45 to 2.4 V,  
Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

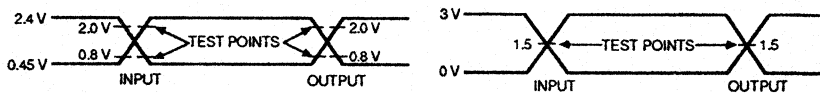
### SWITCHING TEST CIRCUIT



TC003193

$C_L = 100 \text{ pF}$  including jig capacitance (30 pF for -55, -70, & -75)

### SWITCHING TEST WAVEFORMS



11419-001A







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AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are  $\leq 20 \text{ ns}$ .

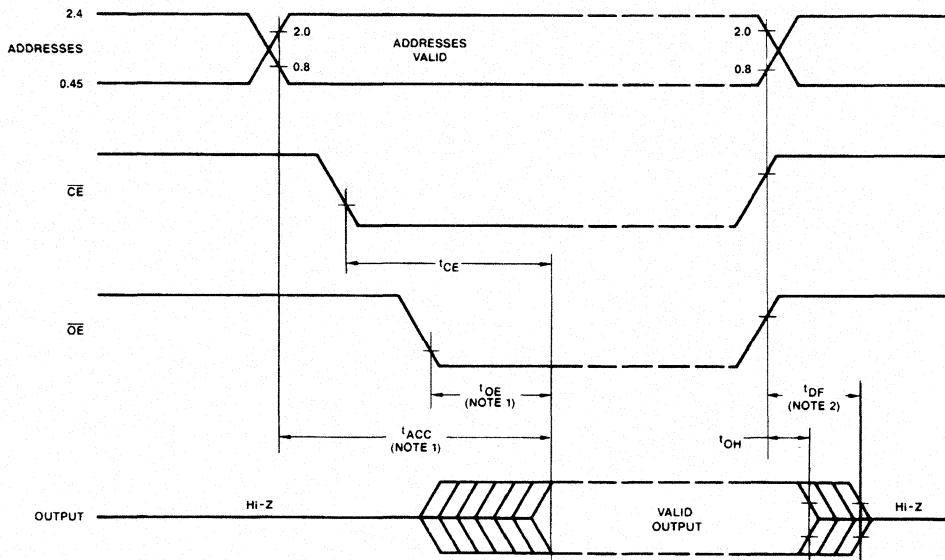
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are  $\leq 20 \text{ ns}$  for -55, -70, & -75 devices.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
 	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

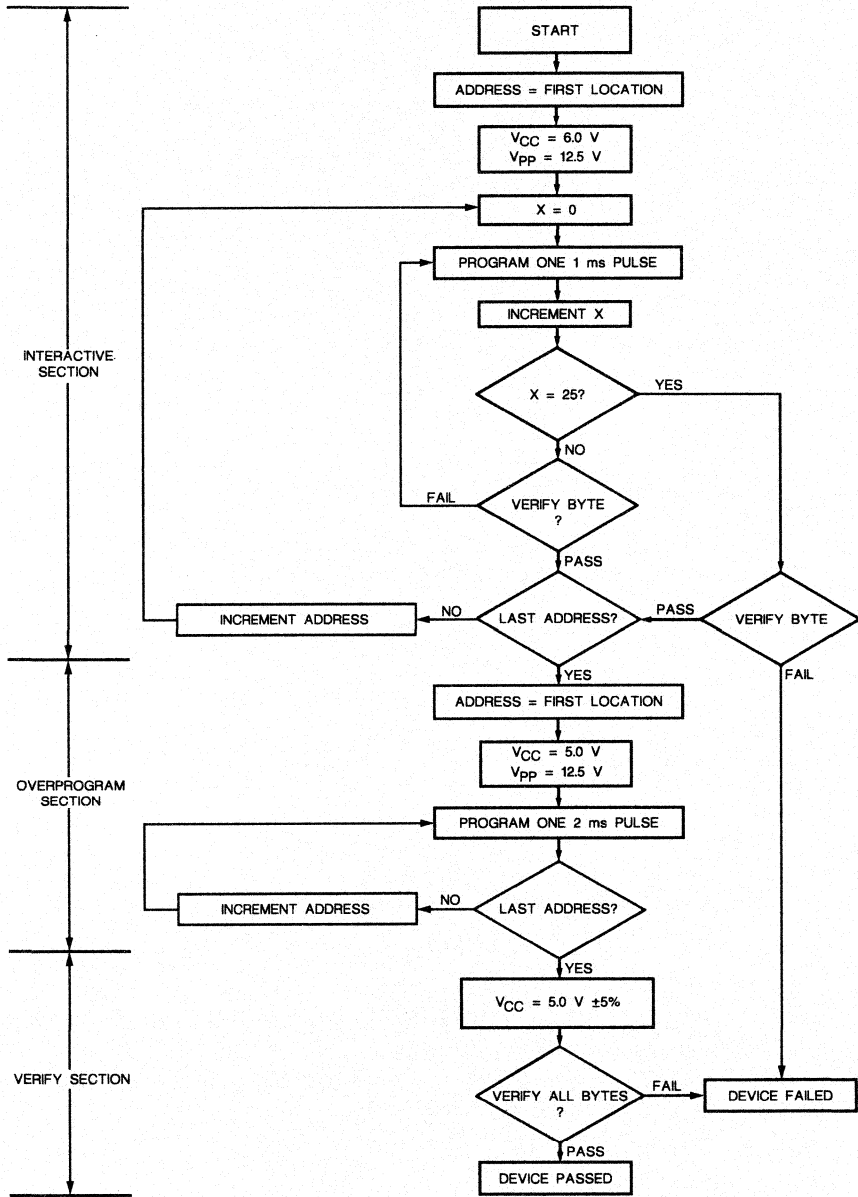
KS000010



WF001323

- Notes: 1.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .  
 2.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.

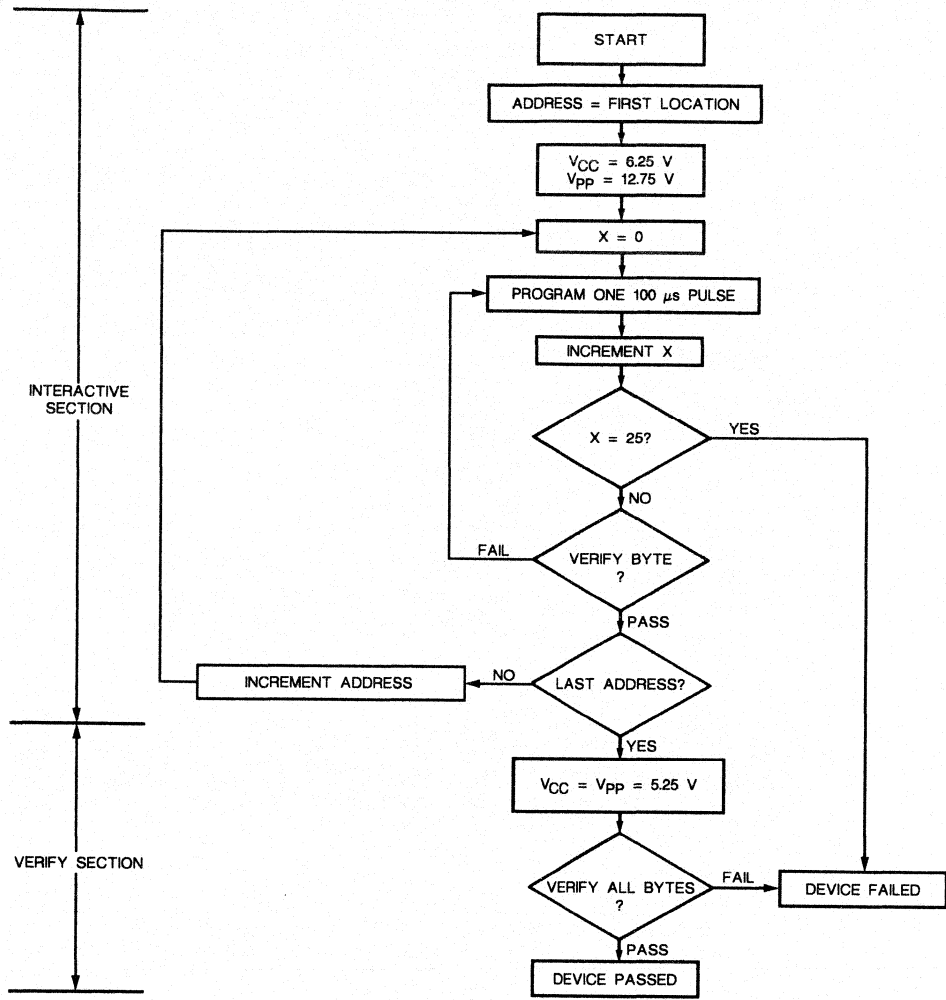
# PROGRAMMING FLOW CHARTS



PF002840

Figure 1. Interactive Programming Flow Chart





**3**

Figure 2. Flashrite Programming Flow Chart for OTP EPROM

10205B-008A  
PF002490

### DC PROGRAMMING CHARACTERISTICS ( $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ ) (Notes 1, 2, & 3).

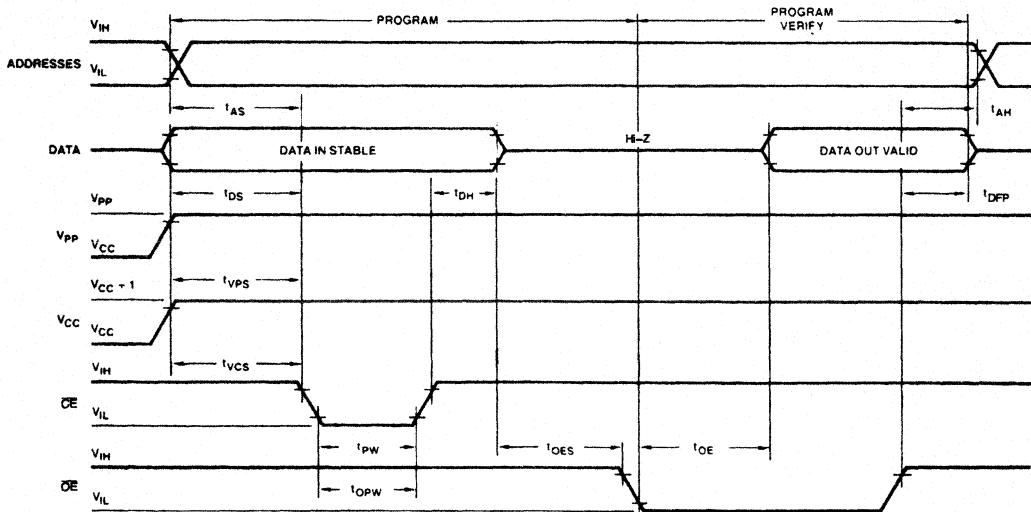
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$I_{LI}$	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or $V_{IH}$		10.0	$\mu\text{A}$
$V_{IL}$	Input LOW Level (All Inputs)		-0.3	0.8	V
$V_{IH}$	Input HIGH Level		2.0	$V_{CC} + 0.5$	V
$V_{OL}$	Output LOW Voltage During Verify	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{OH}$	Output HIGH Voltage During Verify	$I_{OH} = -400 \mu\text{A}$	2.4		V
$V_H$	$A_9$ Auto Select Voltage		11.5	12.5	V
$I_{CC3}$	$V_{CC}$ Supply Current (Program & Verify)			50	mA
$I_{PP2}$	$V_{PP}$ Supply Current (Program)	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$		30	mA
$V_{CC1}$	Interactive Supply Voltage		5.75	6.25	V
$V_{PP1}$	Interactive Programming Voltage		12.0	13.0	V
$V_{CC2}$	Flashrite Supply Voltage		6.00	6.50	V
$V_{PP2}$	Flashrite Programming Voltage		12.5	13.0	V

### SWITCHING PROGRAMMING CHARACTERISTICS ( $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ ) (Notes 1, 2, & 3).

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
$t_{AVEL}$	$t_{AS}$	Address Setup Time	2		$\mu\text{s}$
$t_{DZGL}$	$t_{OES}$	$\overline{OE}$ Setup Time	2		$\mu\text{s}$
$t_{DVEL}$	$t_{DS}$	Data Setup Time	2		$\mu\text{s}$
$t_{GHAX}$	$t_{AH}$	Address Hold Time	0		$\mu\text{s}$
$t_{EHDX}$	$t_{DH}$	Data Hold Time	2		$\mu\text{s}$
$t_{GHQZ}$	$t_{DFP}$	Output Enable to Output Float Delay	0	130	ns
$t_{VPS}$	$t_{VPS}$	$V_{PP}$ Setup Time	2		$\mu\text{s}$
$t_{ELEH1}$	$t_{PW}$	$\overline{CE}$ Program Pulse Width			
		Flashrite	95	105	$\mu\text{s}$
		Interactive	0.95	1.05	ms
$t_{ELEH2}$	$t_{OPW}$	$\overline{CE}$ Overprogram Pulse Width (Interactive)	1.95	2.05	ms
$t_{VCS}$	$t_{VCS}$	$V_{CC}$ Setup Time	2		$\mu\text{s}$
$t_{GLQV}$	$t_{OE}$	Data Valid from $\overline{OE}$		150	ns

- Notes:**
- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$ , and removed simultaneously or after  $V_{PP}$ .
  - When programming the Am27C256, a 0.1- $\mu\text{F}$  capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients which may damage the device.
  - Programming characteristics are sampled but not 100% tested at worst-case conditions.

## PROGRAMMING ALGORITHM WAVEFORMS (Notes 1 & 2)



WF026710

- Notes: 1. The input timing reference level is 0.8 V for  $V_{IL}$  and 2 V for  $V_{IH}$ .  
 2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device, but must be accommodated by the programmer.

# Am27C512

## 65,536 x 8-Bit CMOS EPROM



### DISTINCTIVE CHARACTERISTICS

- Fast access time — 90 ns
- Low power consumption:
  - 100  $\mu$ A maximum standby current
- Programming voltage: 12.5 V
- Single +5-V power supply
- JEDEC-approved pinout
- $\pm 10\%$  power supply tolerance available
- Latch-up protected to 100 mA from  $-1$  V to  $V_{CC} + 1$  V

### GENERAL DESCRIPTION

The Am27C512 is a 512K-bit, ultraviolet erasable programmable read-only memory. It is organized as 65,536 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Devices are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) packages.

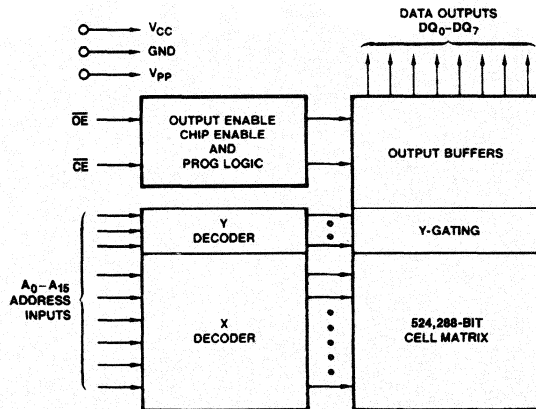
Typically, any byte can be accessed in less than 90 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C512 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus

eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C512 supports AMD's interactive programming algorithm (1-ms pulses) resulting in typical programming times of less than four minutes.

### BLOCK DIAGRAM



BD000213

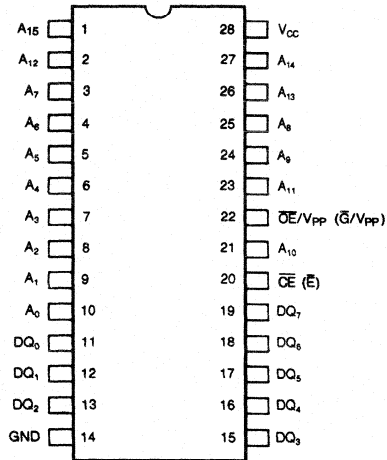
### PRODUCT SELECTOR GUIDE

Family Part No.	Am27C512						
Ordering Part No:							
$\pm 5\%$ $V_{CC}$ Tolerance	-95	-125	-155	-175	-205	-255	-305
$\pm 10\%$ $V_{CC}$ Tolerance	-90	-120	-150	-170	-200	-250	-300
Max. Access Time (ns)	90	120	150	170	200	250	300
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	90	120	150	170	200	250	300
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	40	50	50	50	75	100	100

Publication # 08140 Rev. D  
 Issue Date: February 1989

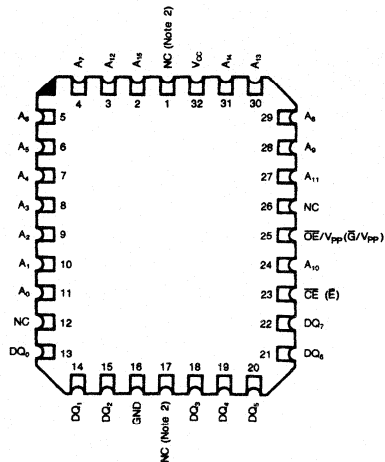
## CONNECTION DIAGRAMS Top View

### DIP



CD011731

### LCC\*



CD00600A

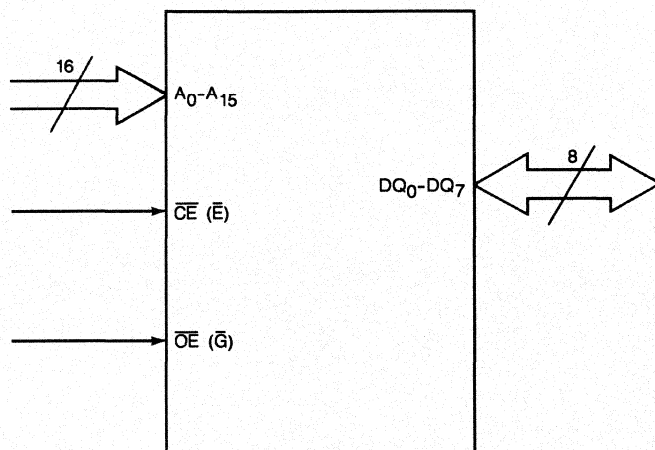
\*Also available in 32-pin rectangular plastic leaded chip carrier.

Notes: 1. JEDEC nomenclature is in parentheses.

2. Don't use (DU) for PLCC.

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## LOGIC SYMBOL



LS003312

## PIN DESCRIPTION

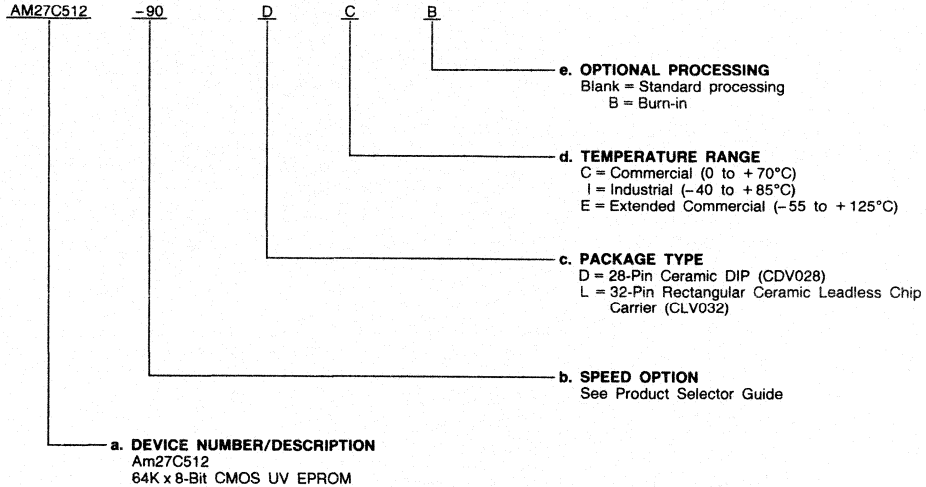
$A_0 - A_{15}$	= Address Inputs
$\overline{CE} (\overline{E})$	= Chip Enable Input
$DQ_0 - DQ_7$	= Data Inputs/Outputs
$\overline{OE} (\overline{G})$	= Output Enable Input
$V_{CC}$	= $V_{CC}$ Supply Voltage
$V_{PP}$	= Program Supply Voltage
GND	= Ground
NC	= No Internal Connection
DU	= No External Connection

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option**
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM27C512-90	DC, DCB, LC, LCB
AM27C512-95	
AM27C512-125	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C512-155	
AM27C512-175	
AM27C512-205	
AM27C512-255	
AM27C512-305	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C512-120	
AM27C512-150	
AM27C512-170	
AM27C512-200	
AM27C512-250	
AM27C512-300	

#### Valid Combinations

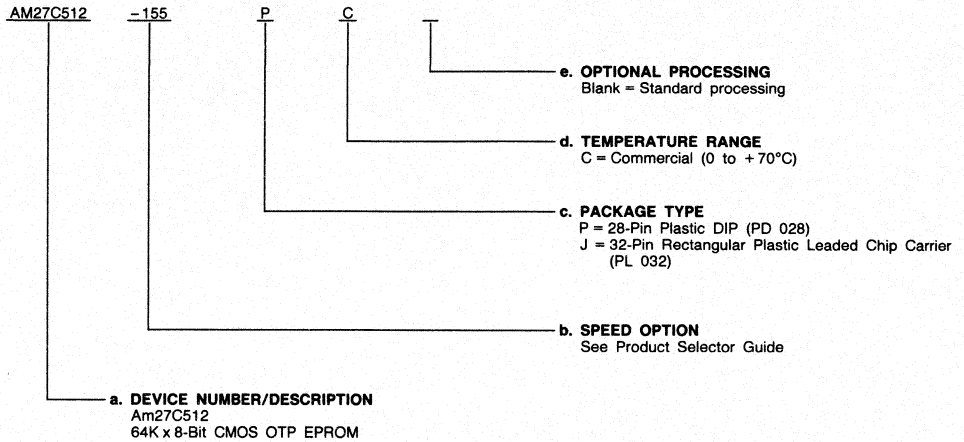
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION (Cont'd.)

### OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number**
- b. Speed Option**
- c. Package Type**
- d. Temperature Range**
- e. Optional Processing**



Valid Combinations	
AM27C512-155	JC, PC
AM27C512-170	
AM27C512-175	
AM27C512-200	
AM27C512-205	
AM27C512-250	
AM27C512-255	
AM27C512-300	
AM27C512-305	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

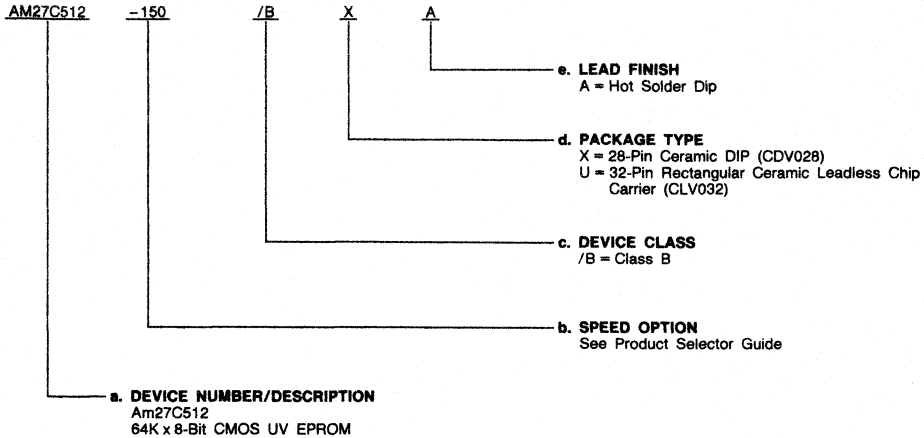


## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM27C512-150	/BXA, /BUA
AM27C512-170	
AM27C512-200	
AM27C512-250	
AM27C512-300	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

## FUNCTIONAL DESCRIPTION

### Erasing the Am27C512

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C512 to an ultraviolet light source. A dosage of 15 W seconds/cm<sup>2</sup> is required to completely erase an Am27C512. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 μW/cm<sup>2</sup> for 15 to 20 minutes. The Am27C512 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C512, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C512 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

### Programming the Am27C512

Upon delivery, or after each erasure, the Am27C512 has all 524,288 bits in the "ONE", or HIGH state. "ZEROS" are loaded into the Am27C512 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the  $\overline{OE}/V_{PP}$  pin, and  $\overline{CE}$  is at  $V_{IL}$ .

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The flowchart in Figure 1 shows AMD's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C512. This part of the algorithm is done at  $V_{CC} = 6.0$  V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at  $V_{CC} = 5$  V ± 5%.

### Program Inhibit

Programming of multiple Am27C512s in parallel with different data is also easily accomplished. Except for  $\overline{CE}$ , all like inputs of the parallel Am27C512 including  $\overline{OE}/V_{PP}$  may be common. A TTL low-level program pulse applied to an Am27C512  $\overline{CE}$  input with  $\overline{OE}/V_{PP} = 12.5 \pm 0.5$  V will program that Am27C512. A high-level  $\overline{CE}$  input inhibits the other Am27C512s from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with  $\overline{OE}/V_{PP}$  and  $\overline{CE}$  at  $V_{IL}$ . Data should be verified  $t_{DV}$  after the falling edge of  $\overline{CE}$ .

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type.

This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C512.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line  $A_9$  of the Am27C512. Two identifier bytes may then be sequenced from the device outputs by toggling address line  $A_0$  from  $V_{IL}$  to  $V_{IH}$ . All other address lines must be held at  $V_{IL}$  during auto select mode.

Byte 0 ( $A_0 = V_{IL}$ ) represents the manufacturer code, and byte 1 ( $A_0 = V_{IH}$ ), the device identifier code. For the Am27C512, these two identifier bytes are given in the Mode Selector table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ<sub>7</sub>) defined as the parity bit.

### Read Mode

The Am27C512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the outputs  $t_{OE}$  after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least  $t_{ACC} - t_{OE}$ .

### Standby Mode

The Am27C512 has a CMOS standby mode which reduces the maximum  $V_{CC}$  current to 100 μA. It is placed in CMOS-standby when  $\overline{CE}$  is at  $V_{CC} \pm 0.3$  V. The Am27C512 also has a TTL-standby mode which reduces the maximum  $V_{CC}$  current to 1.0 mA. It is placed in TTL-standby when  $\overline{CE}$  is at  $V_{IH}$ . When in standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}/V_{PP}$  be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

**MODE SELECT TABLE**

Mode \ Pins						
		$\overline{CE}$	$\overline{OE}/V_{PP}$	$A_0$	$A_9$	Outputs
Read		$V_{IL}$	$V_{IL}$	X	X	DOUT
Output Disable		$V_{IL}$	$V_{IH}$	X	X	High Z
Standby (TTL)		$V_{IH}$	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3 V$	X	X	X	High Z
Program		$V_{IL}$	$V_{PP}$	X	X	DIN
Program Verify		$V_{IL}$	$V_{IL}$	X	X	DOUT
Program Inhibit		$V_{IH}$	$V_{PP}$	X	X	High Z
Auto Select (Note 3)	Manufacturer Code	$V_{IL}$	$V_{IL}$	$V_{IL}$	$V_{H}$	01 H
	Device Code	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{H}$	91 H

- Notes: 1. X can be either  $V_{IL}$  or  $V_{IH}$   
 2.  $V_{H} = 12.0 V \pm 0.5 V$   
 3.  $A_1 - A_8 = A_{10} - A_{15} = V_{IL}$   
 4. See DC Programming characteristics for  $V_{PP}$  voltage during programming.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature:  
 OTP devices ..... -65 to 125°C  
 All other devices ..... -65 to 150°C

Ambient Temperature  
 with Power Applied ..... -55 to +125°C

Voltage with Respect to Ground:  
 All pins except Ag, Vpp, and  
 VCC ..... -0.6 to VCC + 0.5 V  
 Ag and Vpp ..... -0.6 to 13.5 V  
 VCC ..... -0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

- Notes: 1. Minimum DC voltage on input or I/O is -0.5 V. During transitions, the inputs may undershoot GND to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O is VCC + 0.5 V which may overshoot to VCC + 2.0 V for periods up to 20 ns.
2. For Ag and Vpp the minimum DC input is -0.5 V. During transitions, Ag and Vpp may undershoot GND to -2.0 V for periods of up to 20 ns. Ag and Vpp must not exceed 13.5 V for any period of time.

## OPERATING RANGES

Commercial (C) Devices  
 Case Temperature (TC) ..... 0 to +70°C

Industrial (I) Devices  
 Case Temperature (TC) ..... -40 to +85°C

Extended Commercial (E) Devices  
 Case Temperature (TC) ..... -55 to +125°C

Military (M) Devices  
 Case Temperature (TC) ..... -55 to +125°C

Supply Read Voltages:  
 VCC for Am27C512-XX5 ..... +4.75 to +5.25 V  
 VCC for Am27C512-XX0 ..... +4.50 to +5.50 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 7)

### TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
VOH	Output HIGH Voltage	IOH = -400 µA		2.4		V
VOL	Output LOW Voltage	IOL = 2.1 mA			0.45	V
VIH	Input HIGH Voltage			2.0	VCC + 0.5	V
VIL	Input LOW Voltage			-0.3	+0.8	V
ILI	Input Load Current	VIN = 0 V to VCC	C/I Devices		1.0	µA
			E/M Devices		5.0	
ILO	Output Leakage Current	VOUT = 0 V to VCC	C/I Devices		10	µA
			E/M Devices		10	
ICC1	VCC Active Current (Note 5 & 8)	CE = VIL, f = 10 MHz, IOUT = 0 mA (Open Outputs)	C/I Devices		40	mA
			E/M Devices		50	
ICC2	VCC Standby Current (Note 8)	CE = VIH, OE = VIL	C/I Devices		1	mA
			E/M Devices		1	

### CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
VOH	Output HIGH Voltage	IOH = -400 µA		2.4		V
VOL	Output LOW Voltage	IOL = 2.1 mA			0.45	V
VIH	Input HIGH Voltage			VCC - 0.3	VCC + 0.3	V
VIL	Input LOW Voltage			-0.3	+0.8	V
ILI	Input Load Current	VIN = 0 V to VCC	C/I Devices		1.0	µA
			E/M Devices		5.0	

## DC CHARACTERISTICS over operating range unless otherwise specified (Cont'd.)

### CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>	C/I Devices	10	μA
			E/M Devices	10	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current (Note 5 & 8)	$\overline{CE} = V_{IL}$ , f = 10 MHz, I <sub>OUT</sub> = 0 mA (Open Outputs)	C/I Devices	40	mA
			E/M Devices	50	
I <sub>CC2</sub>	V <sub>CC</sub> Standby Current (Note 8)	$\overline{CE} = V_{CC} \pm 0.3$ V	C/I Devices	100	μA
			E/M Devices	100	

### CAPACITANCE (Notes 2, 3, & 6)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C <sub>IN1</sub>	Input Capacitance	V <sub>IN</sub> = 0 V	8	12	pF
C <sub>IN2</sub>	$\overline{OE}/V_{PP}$ Input Capacitance	V <sub>IN</sub> = 0 V	12	20	pF
C <sub>IN3</sub>	$\overline{CE}$ Input Capacitance	V <sub>IN</sub> = 0 V	9	12	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0 V	8	12	pF

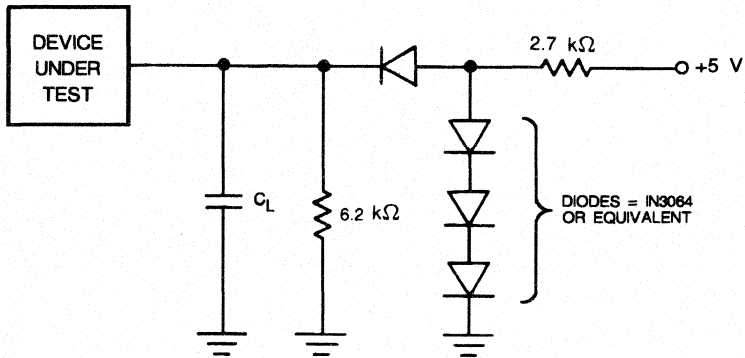
- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>pp</sub>, and removed simultaneously or after V<sub>pp</sub>.  
 2. Typical values are for nominal supply voltages.  
 3. This parameter is only sampled and not 100% tested.  
 4. **Caution:** The Am27C512 must not be removed from, or inserted into, a socket or board when V<sub>pp</sub> or V<sub>CC</sub> is applied.  
 5. I<sub>CC1</sub> is tested with  $\overline{OE} = V_{IH}$  to simulate open outputs.  
 6. T<sub>A</sub> = 25°C, f = 1 MHz.  
 7. Minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> + 0.5 V which may overshoot to V<sub>CC</sub> + 2.0 V for periods less than 20 ns.  
 8. For Am27C512-305DC I<sub>CC1</sub> = 50 mA, I<sub>CC2</sub> (TTL) = 5 mA, I<sub>CC2</sub> (CMOS) = 500 μA maximum.

## SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions	Am27C512							Unit
JEDEC	Standard			-90, -95	-120, -125	-150, -155	-170, -175	-200, -205	-250, -255	-300, -305	
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	Min.							ns
				Max.	90	120	150	170	200	250	
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$	Min.							ns
				Max.	90	120	150	170	200	250	
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.							ns
				Max.	40	50	50	50	75	100	
t <sub>EHQZ</sub> , t <sub>GHQZ</sub>	t <sub>DF</sub>	Output Enable HIGH to Output Float (Note 2)		Min.							ns
				Max.	30	30	30	30	60	60	
t <sub>AXQX</sub>	t <sub>OH</sub>	Output Hold from Addresses, $\overline{CE}$ , or $\overline{OE}$ , whichever occurred first		Min.	0	0	0	0	0	0	ns
				Max.							

- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>pp</sub>, and removed simultaneously or after V<sub>pp</sub>.  
 2. This parameter is only sampled and not 100% tested.  
 3. **Caution:** The Am27C512 must not be removed from, or inserted into, a socket or board when V<sub>pp</sub> or V<sub>CC</sub> is applied.  
 4. Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF, Input Rise and Fall Times: 20 ns, Input Pulse Levels: 0.45 to 2.4 V, Timing Measurement Reference Level – Inputs: 0.8 V and 2 V  
 Outputs: 0.8 V and 2 V

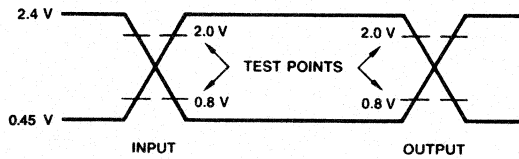
### SWITCHING TEST CIRCUIT



$C_L = 100 \text{ pF}$  including jig capacitance

TC003193

### SWITCHING TEST WAVEFORM








WF009502

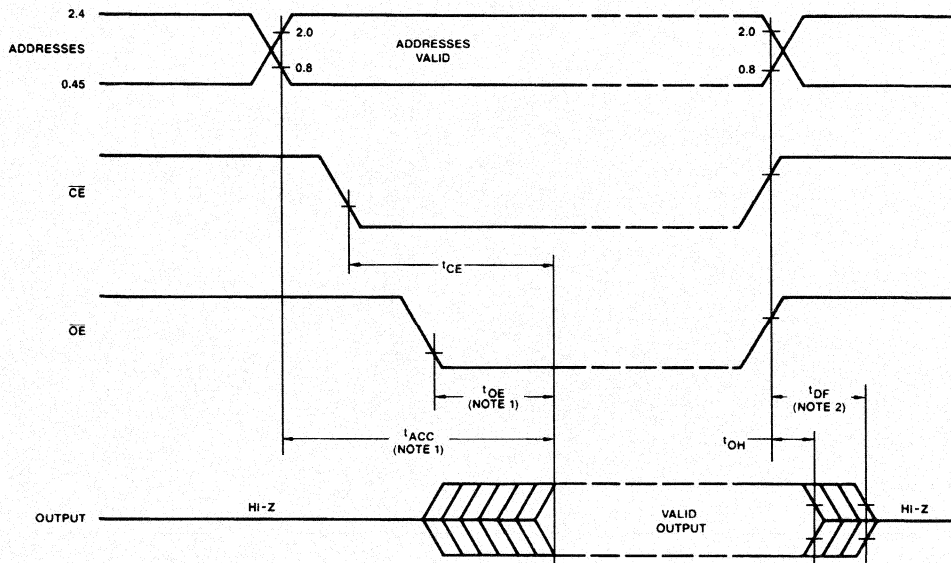
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are  $\leq 20 \text{ ns}$ .

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

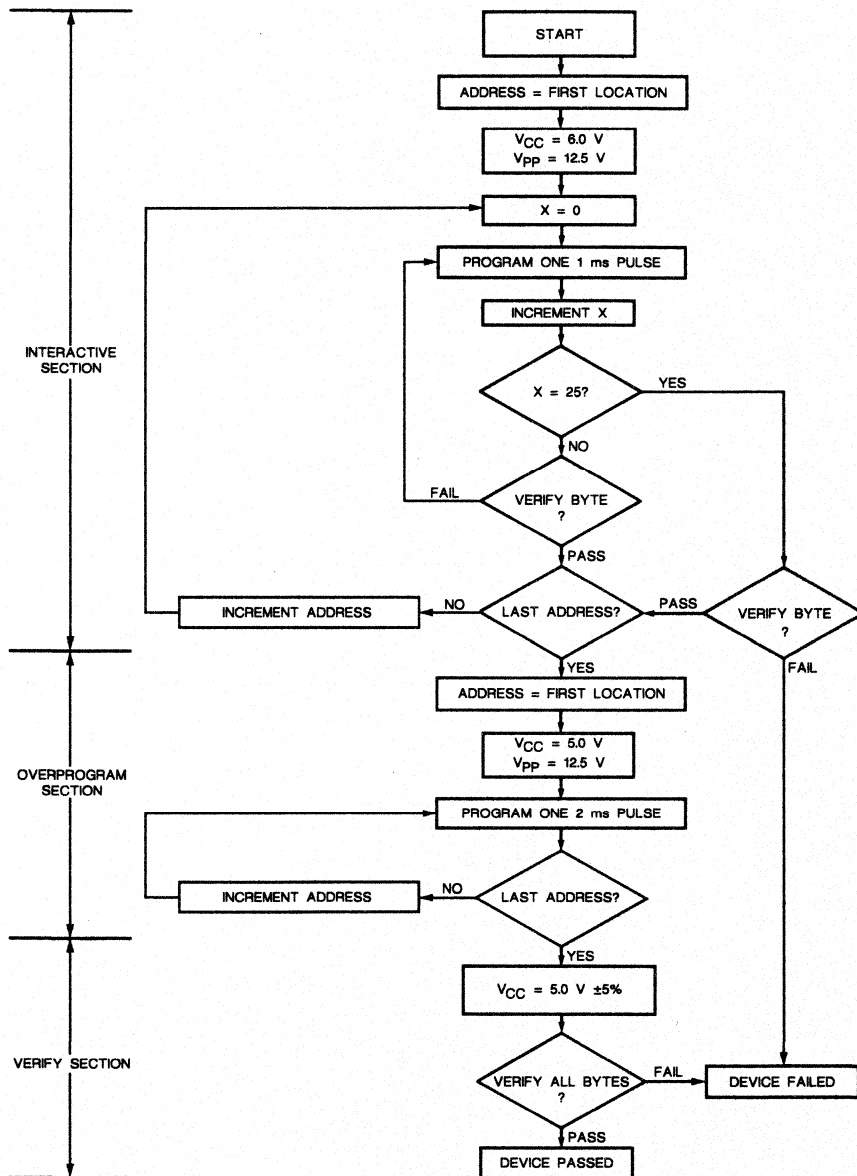
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KSO00010



WF001323

- Notes: 1.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .  
 2.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.



PF002841

Figure 1. Interactive Programming Flow Chart



## INTERACTIVE ALGORITHM

### DC PROGRAMMING CHARACTERISTICS ( $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ ) (Notes 1, 2, & 3).

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$I_{LI}$	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or $V_{IH}$		10.0	$\mu\text{A}$
$V_{IL}$	Input LOW Level (All Inputs)		-0.3	0.8	V
$V_{IH}$	Input HIGH Level		2.0	$V_{CC} + 0.5$	V
$V_{OL}$	Output LOW Voltage During Verify	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{OH}$	Output HIGH Voltage During Verify	$I_{OH} = -400 \mu\text{A}$	2.4		V
$V_H$	$A_9$ Auto Select Voltage		11.5	12.5	V
$I_{CC3}$	$V_{CC}$ Supply Current (Program & Verify)			50	mA
$I_{PP}$	$V_{PP}$ Supply Current (Program)	$\overline{CE} = V_{IL}, \overline{OE}/V_{PP} = V_{PP}$		30	mA
$V_{CC}$	Interactive Supply Voltage		5.75	6.25	V
$V_{PP}$	Interactive Programming Voltage		12.0	13.0	V

### SWITCHING PROGRAMMING CHARACTERISTICS ( $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ ) (Notes 1, 2, & 3).

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
$t_{AVEL}$	$t_{AS}$	Address Setup Time	2		$\mu\text{s}$
$t_{DVEL}$	$t_{DS}$	Data Setup Time	2		$\mu\text{s}$
$t_{GHAX}$	$t_{AH}$	Address Hold Time	0		$\mu\text{s}$
$t_{EHDX}$	$t_{DH}$	Data Hold Time	2		$\mu\text{s}$
$t_{EHQZ}$	$t_{DFP}$	Chip Enable to Output Float Delay	0	60	ns
$t_{VPS}$	$t_{VPS}$	$V_{PP}$ Setup Time	2		$\mu\text{s}$
$t_{ELEH1}$	$t_{PW}$	$\overline{CE}$ Initial Program Pulse Width	0.95	1.05	ms
$t_{ELEH2}$	$t_{OPW}$	$\overline{CE}$ Overprogram Pulse Width	1.95	2.05	ms
$t_{VCS}$	$t_{VCS}$	$V_{CC}$ Setup Time	2		$\mu\text{s}$
$t_{ELQV}$	$t_{DV}$	Data Valid from $\overline{CE}$		250	ns
$t_{EHGL}$	$t_{OEH}$	$\overline{OE}/V_{PP}$ Hold Time	2		$\mu\text{s}$
$t_{GLEL}$	$t_{VR}$	$\overline{OE}/V_{PP}$ Recovery Time	2		$\mu\text{s}$

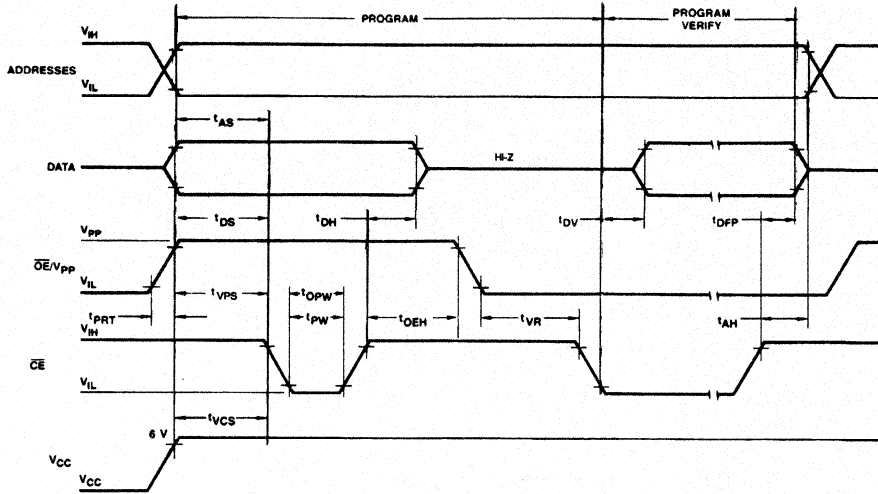
**Notes:** 1.  $V_{CC}$  must be applied simultaneously or before  $V_{pp}$ , and removed simultaneously or after  $V_{pp}$ .

2. When programming the Am27C512, a 0.1- $\mu\text{F}$  capacitor is required across  $V_{pp}$  and ground to suppress spurious voltage transients which may damage the device.

3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

3

INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS (Notes 1 & 2)



WF021992

- Notes: 1. The input timing reference level is 0.8 V for V<sub>IL</sub> and 2 V for V<sub>IH</sub>.  
 2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device, but must be accommodated by the programmer.



# Am27C010

1 Megabit (131,072 x 8-Bit) CMOS EPROM

## DISTINCTIVE CHARACTERISTICS

- Easy upgrade from 28-pin JEDEC EPROMs
- Fast access time
  - 100 ns
- Low power consumption
  - 100  $\mu$ A maximum standby current
- Programming voltage: 12.5 V
- Single + 5-V power supply
- Compact 32-pin DIP package requires no hardware change for upgrades to 8 megabits
- JEDEC-approved pinout
- $\pm 10\%$  power supply tolerance available
- One-Time Programmable (OTP) Flashrite™ programming
- Latch-up protected to 100 mA from  $-1$  V to  $V_{cc} + 1$  V

## GENERAL DESCRIPTION

The Am27C010 is a 1 megabit ultraviolet erasable programmable read-only memory. It is organized as 128K words by 8 bits per word, operates from a single + 5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) packages.

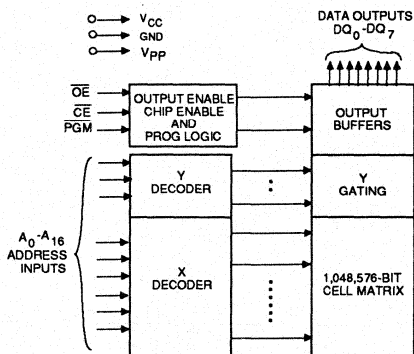
Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C010 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus

microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C010 supports AMD's interactive programming algorithm (0.5 ms pulses) resulting in typical programming times of less than two minutes.

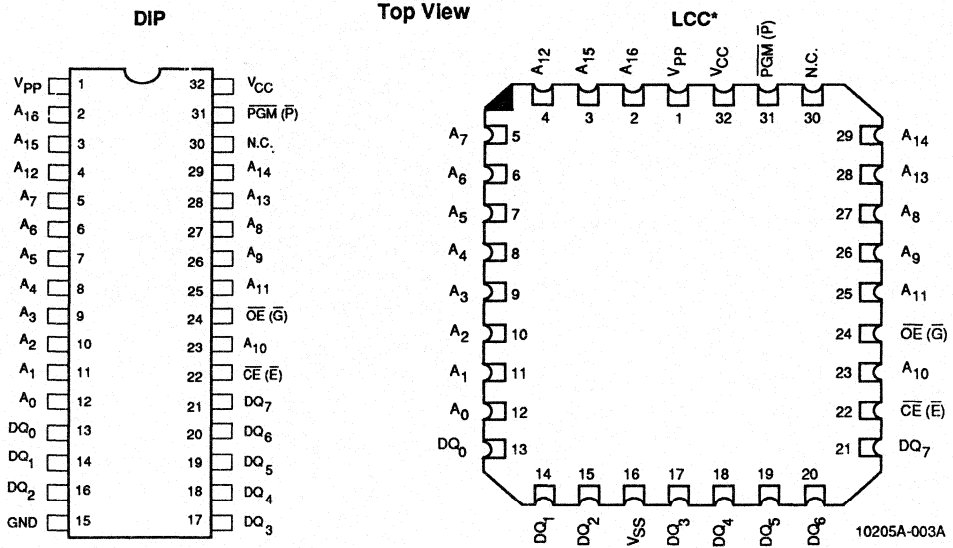
## BLOCK DIAGRAM



## PRODUCT SELECTOR GUIDE

Family Part No.	Am27C010						
<b>Ordering Part No:</b>							
$V_{cc} \pm 5\%$	-105	-125	-155	-175	-205	-255	-305
$V_{cc} \pm 10\%$	-100	-120	-150	-170	-200	-250	-300
Max. Access Time (ns)	100	120	150	170	200	250	300
$\overline{CE}$ (E) Access Time (ns)	100	120	150	170	200	250	300
$\overline{OE}$ (G) Access Time (ns)	50	50	65	65	75	100	120

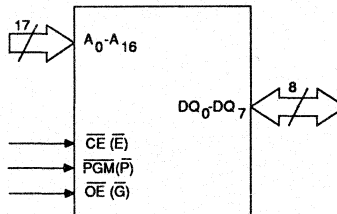
## CONNECTION DIAGRAMS



- Notes: 1. JEDEC nomenclature is in parentheses.  
 2. The 32-Pin DIP to 32-Pin LCC configuration varies from the JEDEC 28-Pin DIP to 32-Pin LCC configuration.

\* Also available in 32-pin rectangular plastic leaded chip carrier

### LOGIC SYMBOL



10205A-002A

### Pin Description

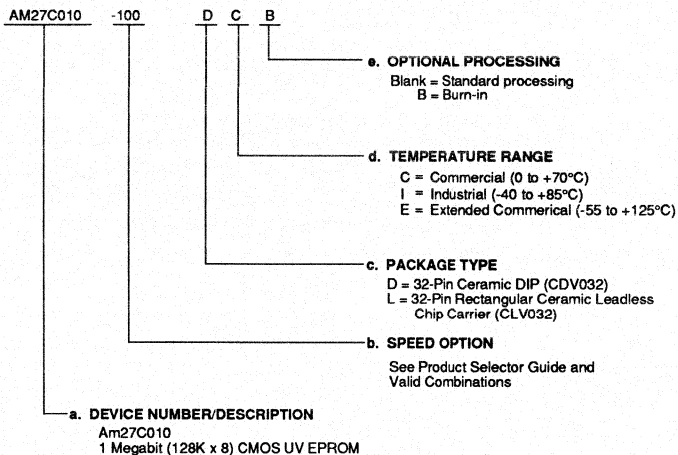
- $A_0-A_{16}$  = Address Inputs
- $\overline{CE} (\overline{E})$  = Chip Enable Input
- $DQ_0-DQ_7$  = Data Input/Outputs
- $\overline{OE} (\overline{G})$  = Output Enable Input
- $\overline{PGM} (\overline{P})$  = Program Enable Input
- $V_{CC}$  =  $V_{CC}$  Supply Voltage
- $V_{PP}$  = Program Supply Voltage
- GND = Ground
- NC = No Internal Connect

# ORDERING INFORMATION

## Standard Information

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27C010-100	DC, DCB
AM27C010-105	
AM27C010-120	
AM27C010-125	
AM27C010-155	DC, DCB, DI, DIB, LC, LI
AM27C010-175	
AM27C010-205	
AM27C010-255	
AM27C010-305	
AM27C010-170	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C010-200	
AM27C010-250	
AM27C010-300	

### Valid Combinations

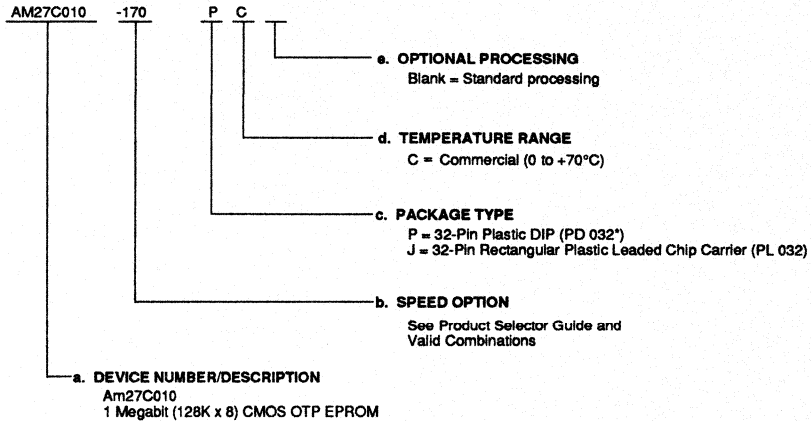
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION (Cont'd.)

### OTP Products (Preliminary)

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27C010-170	PC, JC
AM27C010-175	
AM27C010-200	
AM27C010-205	
AM27C010-250	
AM27C010-255	
AM27C010-300	
AM27C010-305	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

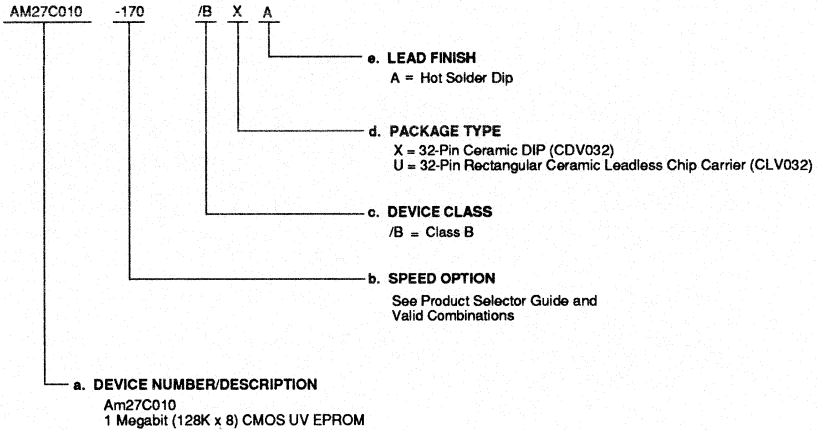
\*Package in Development; consult NVD Product Marketing for information.

## ORDERING INFORMATION (Cont'd.)

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM27C010-170	/BXA, /BUA
AM27C010-200	
AM27C010-250	
AM27C010-300	

For other Surface Mount Package options, contact NVD Military Marketing.

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## FUNCTIONAL DESCRIPTION

### Erasing the Am27C010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C010 to an ultraviolet light source. A dosage of 15 W seconds/cm<sup>2</sup> is required to completely erase an Am27C010. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 μW/cm<sup>2</sup> for 15 to 20 minutes. The Am27C010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C010, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

### Programming the Am27C010

Upon delivery, or after each erasure, the Am27C010 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROS" are loaded into the Am27C010 through the procedure of programming.

The programming mode is entered when  $12.5 \pm 0.5$  V is applied to the  $V_{PP}$  pin,  $\overline{CE}$  and  $\overline{PGM}$  is at  $V_{IL}$ , and  $\overline{OE}$  is at  $V_{IH}$ .

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The flowchart Figure 1 shows AMD's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C010. This part of the algorithm is done at  $V_{CC} = 6.0$  V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at  $V_{CC} = 5$  V  $\pm$  5%.

### Flashrite

The OTP EPROM Flashrite programming algorithm (shown in Figure 2) reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the OTP EPROM.

The Flashrite programming algorithm programs and verifies at  $V_{CC} = 6.25$  V and  $V_{PP} = 12.75$  V. After the final address is completed, all bytes are compared to the original data with  $V_{CC} = V_{PP} = 5.25$  V.

### Program Inhibit

Programming of multiple Am27C010 in parallel with different data is also easily accomplished. Except for  $\overline{CE}$ , all like inputs of the parallel Am27C010 may be common. A TTL low-level program pulse applied to an Am27C010  $\overline{CE}$  input with  $V_{PP} = 12.5 \pm 0.5$  V,  $\overline{PGM}$  is LOW, and  $\overline{OE}$  HIGH will program that Am27C010. A high-level  $\overline{CE}$  input inhibits the other Am27C010 from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with  $\overline{OE}$  and  $\overline{CE}$  at  $V_{IL}$ ,  $\overline{PGM}$  at  $V_{IH}$ , and  $V_{PP}$  between 12.0 V to 13.0 V.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C  $\pm$  5°C ambient temperature range that is required when programming the Am27C010.

To activate this mode, the programming equipment must force  $12.0 \pm 0.5$  V on address line  $A_0$  of the Am27C010. Two identifier bytes may then be sequenced from the device outputs by toggling address line  $A_0$  from  $V_{IL}$  to  $V_{IH}$ . All other address lines must be held at  $V_{IL}$  during auto select mode.

Byte 0 ( $A_0 = V_{IL}$ ) represents the manufacturer code, and byte 1 ( $A_0 = V_{IH}$ ), the device identifier code. For the Am27C010, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ<sub>7</sub>) defined as the parity bit.

### Read Mode

The Am27C010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the outputs  $t_{OE}$  after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least  $t_{ACC} - t_{OE}$ .

### Standby Mode

The Am27C010 has a CMOS standby mode which reduces the maximum  $V_{CC}$  current to 100 μA. It is placed in CMOS-standby when  $\overline{CE}$  is at  $V_{CC} \pm 0.3$  V. The Am27C010 also has a TTL-standby mode which reduces the maximum  $V_{CC}$  current to 1.0 mA. It is placed in TTL-standby when  $\overline{CE}$  is at  $V_{IH}$ . When in standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.



It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling

edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1- $\mu$ F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7- $\mu$ F bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode	Pins	$\overline{CE}$	$\overline{OE}$	PGM	$A_0$	$A_9$	$V_{PP}$	Outputs
Read		$V_{IL}$	$V_{IL}$	X	X	X	X	$D_{OUT}$
Output Disable		$V_{IL}$	$V_{IH}$	X	X	X	X	Hi-Z
Standby (TTL)		$V_{IH}$	X	X	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3 V$	X	X	X	X	X	Hi-Z
Program		$V_{IL}$	$V_{IH}$	$V_{IL}$	X	X	$V_{PP}$	$D_{IN}$
Program Verify		$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$	$D_{OUT}$
Program Inhibit		$V_{IH}$	X	X	X	X	$V_{PP}$	Hi-Z
Auto Select	Manufacturer Code	$V_{IL}$	$V_{IL}$	X	$V_{IL}$	$V_H$	X	O1H
(Note 3)	Device Code	$V_{IL}$	$V_{IL}$	X	$V_{IH}$	$V_H$	X	OEH

- Notes: 1.  $V_H = 12.0 V \pm 0.5 V$   
 2. X = Either  $V_{IH}$  or  $V_{IL}$   
 3.  $A_1 - A_9 = A_{10} - A_{16} = V_{IL}$   
 4. See DC Programming Characteristics for  $V_{PP}$  voltage during programming.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
OTP products .....	-65 to 125°C
All other products .....	-65 to 150°C
Ambient Temperature	
with Power Applied .....	-55 to +125°C
Voltage with Respect to Ground:	
All pins except $A_9$ , $V_{PP}$ , and	
$V_{CC}$ .....	-0.6 to $V_{CC} + 0.5$ V
$A_9$ and $V_{CC}$ .....	-0.6 to 13.5
$V_{CC}$ .....	-0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

- Notes: 1. Minimum DC voltage on input or I/O is -0.5 V. During transitions, the inputs may undershoot GND to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O is  $V_{CC} + 0.5$  V which may overshoot to  $V_{CC} + 2.0$  V for periods up to 20 ns.
2. For  $A_9$  and  $V_{PP}$  the minimum DC input is -0.5 V. During transitions,  $A_9$  and  $V_{PP}$  may undershoot GND to -2.0 V for periods of up to 20 ns.  $A_9$  and  $V_{PP}$  must not exceed 13.5 V for any period of time.

## OPERATING RANGES

Commercial (C) Devices	
Case Temperature ( $T_C$ ) .....	0 to +70°C
Industrial (I) Devices	
Case Temperature ( $T_C$ ) .....	-40 to +85°C
Extended Commercial (E) Devices	
Case Temperature ( $T_C$ ) .....	-55 to +125°C
Military (M) Devices	
Case Temperature ( $T_C$ ) .....	-55 to +125°C
Supply Read Voltages:	
$V_{CC}$ for Am27C010-XX5 .....	+4.75 to + 5.25 V
$V_{CC}$ for Am27C010-XX0 .....	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 4, 5, & 8) (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

### TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400 \mu A$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage		-0.3	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0 \text{ V to } +V_{CC}$	C/I Devices	1.0	$\mu A$
			E/M Devices	1.0	
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0 \text{ V to } +V_{CC}$	C/I Devices	10	$\mu A$
			E/M Devices	10	
$I_{CC1}$	$V_{CC}$ Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$ , $f = 5 \text{ MHz}$ $I_{OUT} = 0 \text{ mA}$ (Open Outputs)	C/I Devices	30	mA
			E/M Devices	60	
$I_{CC2}$	$V_{CC}$ Standby Current (Note 9)	$\overline{CE} = V_{IH}$	C/I Devices	1.0	mA
			E/M Devices	1.0	
$I_{PP1}$	$V_{PP}$ Current During Read (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$ , $V_{PP} = V_{CC}$		100	$\mu A$

## DC CHARACTERISTICS (Cont.)

### CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400 \mu A$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{IH}$	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage		-0.3	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0 \text{ V to } +V_{CC}$	C/I Devices	1.0	$\mu A$
			E/M Devices	1.0	
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0 \text{ V to } +V_{CC}$	C/I Devices	10	$\mu A$
			E/M Devices	10	
$I_{CC1}$	$V_{CC}$ Active Current (Notes 5 & 9)	$\overline{OE} = V_{IL}, f = 5 \text{ MHz}$ $I_{OUT} = 0 \text{ mA}$ (Open Outputs)	C/I Devices	30	mA
			E/M Devices	60	
$I_{CC2}$	$V_{CC}$ Standby Current (Note 9)	$\overline{CE} = V_{CC} \pm 0.3 \text{ V}$	C/I Devices	100	$\mu A$
			E/M Devices	100	
$I_{PP1}$	$V_{PP}$ Current During Read (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}, V_{PP} = V_{CC}$		100	$\mu A$

### Capacitance (Notes 2, 3, and 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		Unit
			Typ.	Max.	Typ.	Max.	
$C_{IN1}$	Address Input Capacitance	$V_{IN} = 0 \text{ V}$	8	12	6	9	pF
$C_{IN2}$	$\overline{OE}$ Input Capacitance	$V_{IN} = 0 \text{ V}$	12	20	9	15	pF
$C_{IN3}$	$\overline{CE}$ Input Capacitance	$V_{IN} = 0 \text{ V}$	9	12	7	9	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0 \text{ V}$	8	12	6	9	pF

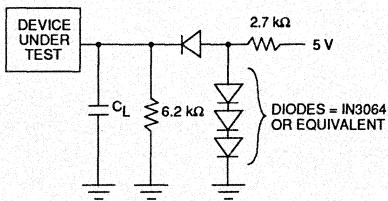
- Notes:
- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$ , and removed simultaneously or after  $V_{PP}$ .
  - Typical values are for nominal supply voltages.
  - This parameter is only sampled, not 100% tested.
  - Caution:** the Am27C010 must not be removed from (or inserted into) a socket when  $V_{CC}$  or  $V_{PP}$  is applied.
  - $I_{CC1}$  is tested with  $\overline{OE} = V_{IH}$  to simulate open outputs.
  - Maximum active power usage is the sum of  $I_{CC}$  and  $I_{PP}$ .
  - $T_A = +25^\circ C, f = 1 \text{ MHz}$ .
  - Minimum DC Input Voltage is  $-0.5 \text{ V}$ . During transitions, the inputs undershoot to  $-2.0 \text{ V}$  for periods less than 20 ns. Maximum DC Voltage on output pins is  $V_{CC} + 0.5 \text{ V}$  which may overshoot to  $V_{CC} + 2.0 \text{ V}$  for periods less than 20 ns.
  - For Am27C010-305  $I_{CC1} = 50 \text{ mA}$ ,  $I_{CC2}$  (TTL) = 5 mA,  $I_{CC2}$  (CMOS) = 1 mA, and  $I_{PP1} = 1 \text{ mA}$ .

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (Notes 1, 3, & 4)  
 (for APL Products, Group A, Subgroups 9, 10, and 11 are specified unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions	Am27C010							Unit	
				-100, -105	-120, -125	-150, -155	-170, -175	-200, -205	-250, -255	-300, -305		
$t_{AVO\bar{V}}$	$t_{ACC}$	Address to Output Delay	$\bar{C}\bar{E} = \bar{O}\bar{E} = V_{IL}$	Min.	-	-	-	-	-	-	-	ns
				Max.	100	120	150	170	200	250	300	
$t_{ELO\bar{V}}$	$t_{CE}$	Chip Enable to Output Delay	$\bar{O}\bar{E} = V_{IL}$	Min.	-	-	-	-	-	-	-	ns
				Max.	100	120	150	170	200	250	300	
$t_{GLO\bar{V}}$	$t_{OE}$	Output Enable to Output Delay	$\bar{C}\bar{E} = V_{IL}$	Min.	-	-	-	-	-	-	-	ns
				Max.	50	50	65	65	75	100	100	
$t_{EHQZ}$ $t_{GHQZ}$	$t_{DF}$ (Note 2)	Chip Enable HIGH or Output Enable HIGH, Whichever Comes First, to Output Float		Min.	0	0	0	0	0	0	0	ns
				Max.	50	50	50	50	60	60	60	
$t_{AXO\bar{X}}$	$t_{OH}$	Output Hold from Addresses, $\bar{C}\bar{E}$ , or $\bar{O}\bar{E}$ , Whichever Occured First		Min.	0	0	0	0	0	0	0	ns
				Max.	-	-	-	-	-	-	-	

- Notes:
1.  $V_{CC}$  must be applied simultaneously or before  $V_{pp}$ , and removed simultaneously or after  $V_{pp}$ .
  2. This parameter is only sampled, not 100% tested.
  3. **Caution:** The Am27C010 must not be removed from (or inserted into) a socket or board when  $V_{pp}$  or  $V_{cc}$  is applied.
  4. Output Load: 1 TTL gate and  $C_L = 100$  pF  
 Input Rise and Fall Times: 20 ns  
 Input Pulse Levels: 0.45 to 2.4 V  
 Timing Measurement Reference Level — Inputs: 0.8 to 2.0 V  
 Outputs: 0.8 to 2.0V

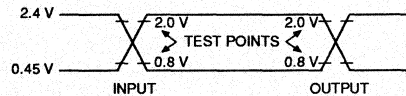
**SWITCHING TEST CIRCUIT**



$C_L = 100$  pF including jig capacitance.

10205A-004A

**SWITCHING TEST WAVEFORM**



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".  
 Input pulse rise and fall times are  $\leq 20$  ns.

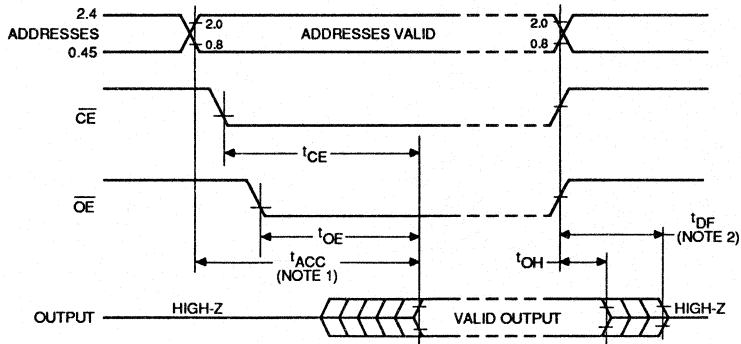
10205B-009A

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN

KS000010

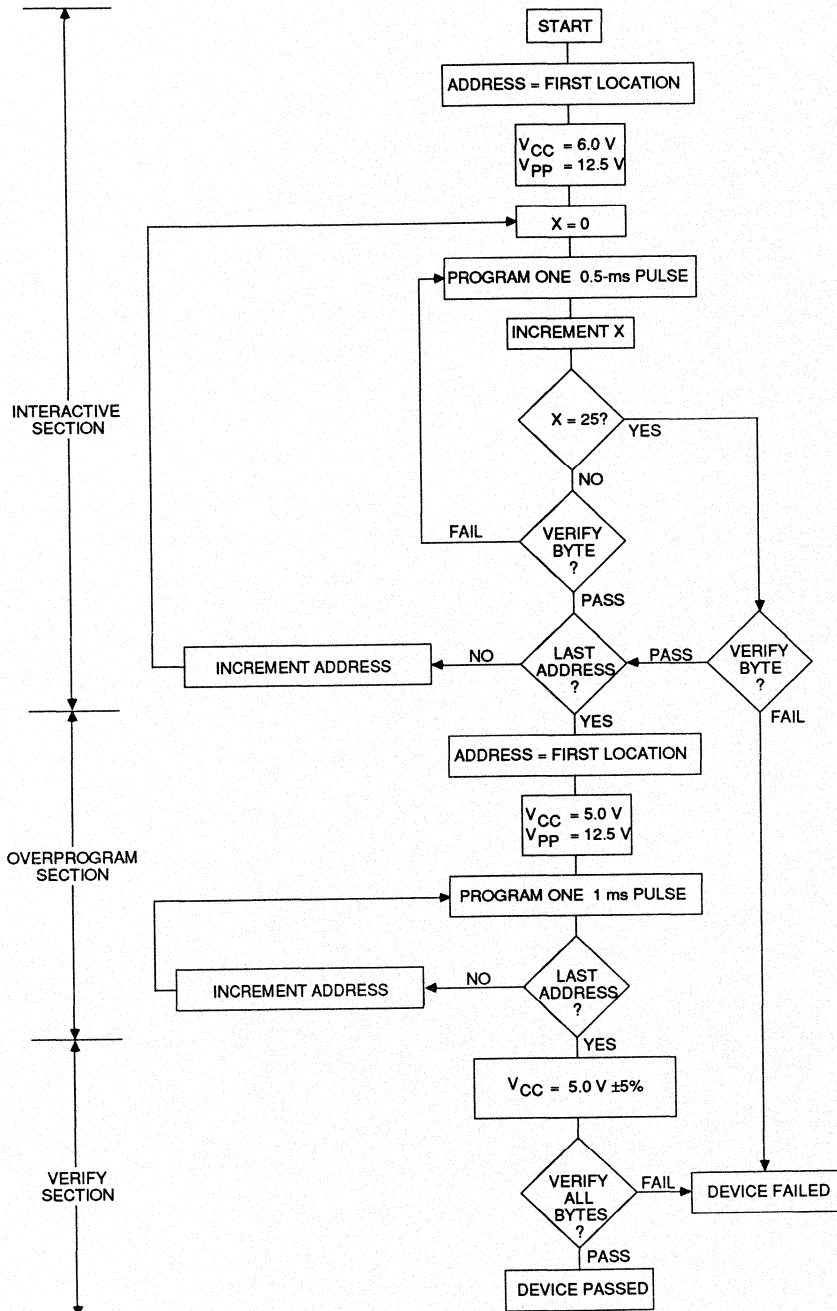


- Notes: 1.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .  
 2.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.

10205A-005A

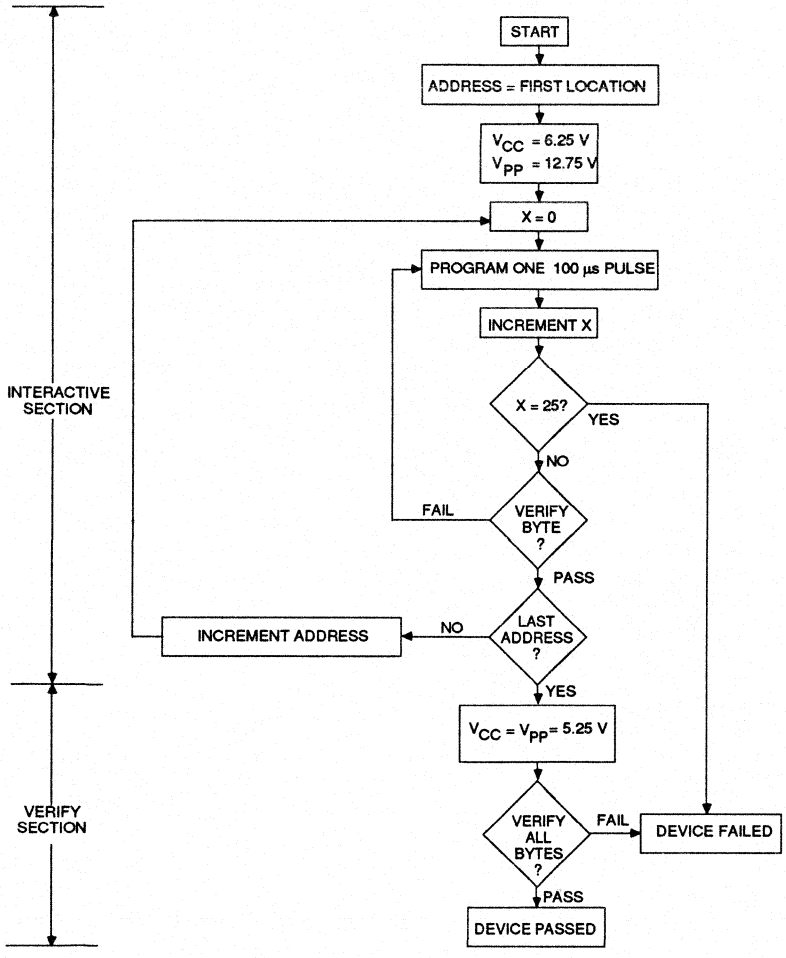
3

# PROGRAMMING FLOW CHARTS



10205B-007A

Figure 1. Interactive Programming Flow Chart



10205B-008A

Figure 2. Flashrite Programming Flow Chart for OTP EPROM

**DC PROGRAMMING CHARACTERISTICS** ( $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ ) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$I_{LI}$	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or $V_{IH}$		10.0	$\mu\text{A}$
$V_{IL}$	Input LOW Level (All Inputs)		-0.3	0.8	V
$V_{IH}$	Input HIGH Level		2.0	$V_{CC} + 0.5$	V
$V_{OL}$	Output LOW Voltage During Verify	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{OH}$	Output HIGH Voltage During Verify	$I_{OH} = -400 \mu\text{A}$	2.4		V
$V_H$	$A_9$ Auto Select Voltage		11.5	12.5	V
$I_{CC3}$	$V_{CC}$ Supply Current (Program & Verify)			50	mA
$I_{PP2}$	$V_{PP}$ Supply Current (Program)	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$		30	mA
$V_{CC1}$	Interactive Supply Voltage		5.75	6.25	V
$V_{PP1}$	Interactive Programming Voltage		12.0	13.0	V
$V_{CC2}$	Flashrite Supply Voltage		6.00	6.50	V
$V_{PP2}$	Flashrite Programming Voltage		12.5	13.0	V

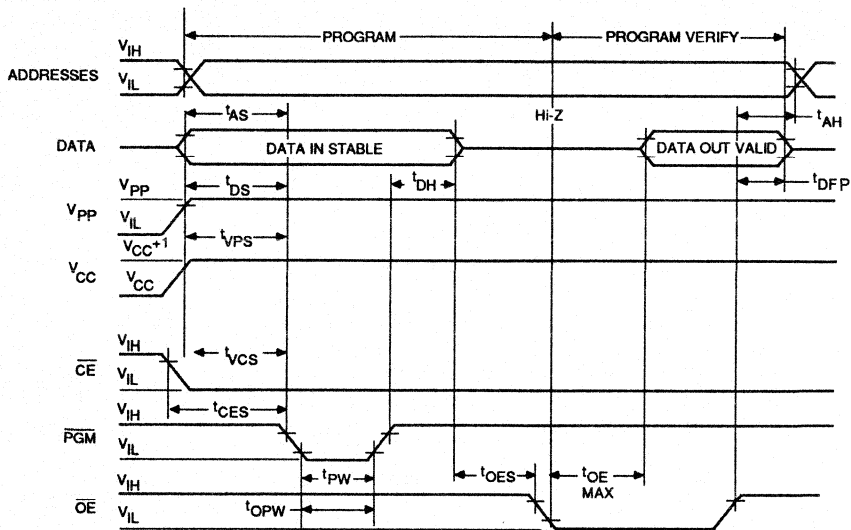
**SWITCHING PROGRAMMING CHARACTERISTICS** ( $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ ) (Notes 1, 2, and 3)

Parameter Symbols		Parameter Description	Min.	Max.	Unit	
JEDEC	Standard					
$t_{AVEL}$	$t_{AS}$	Address Setup Time	2		$\mu\text{s}$	
$t_{DZGL}$	$t_{OES}$	$\overline{OE}$ Setup Time	2		$\mu\text{s}$	
$t_{DVEL}$	$t_{DS}$	Data Setup Time	2		$\mu\text{s}$	
$t_{GHAX}$	$t_{AH}$	Address Hold Time	0		$\mu\text{s}$	
$t_{EHDX}$	$t_{DH}$	Data Hold Time	2		$\mu\text{s}$	
$t_{GHOZ}$	$t_{DFP}$	Output Enable to Output Float Delay	0	130	ns	
$t_{VPS}$	$t_{VPS}$	$V_{PP}$ Setup Time	2		$\mu\text{s}$	
$t_{ELEH1}$	$t_{PW}$	PGM Initial Program Pulse Width	Flashrite	95	105	$\mu\text{s}$
			Interactive	0.45	0.55	ms
$t_{ELEH2}$	$t_{OPW}$	PGM Overprogram Pulse Width (Interactive)	0.95	1.05	ms	
$t_{VCS}$	$t_{VCS}$	$V_{CC}$ Setup Time	2		$\mu\text{s}$	
$t_{ELPL}$	$t_{CES}$	$\overline{CE}$ Setup Time	2		$\mu\text{s}$	
$t_{GLOV}$	$t_{OE}$	Data Valid from $\overline{OE}$		150	ns	

- Notes:
- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$ , and removed simultaneously or after  $V_{PP}$ .
  - When programming the Am27C010, a 0.1- $\mu\text{F}$  capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients which may damage the device.
  - Programming characteristics are sampled but not 100% tested at worst-case conditions.



**INTERACTIVE and FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 and 2)**



- Notes: 1. The input timing reference level is 0.8 V for a V<sub>IL</sub> and 2 V for a V<sub>IH</sub> .  
 2. t<sub>OE</sub> and t<sub>DFP</sub> are characteristics of the device but must be accommodated by the programmer. 10205A-006A

# Am27C1024

1 Megabit (65,536 x 16-Bit) CMOS EPROM



## DISTINCTIVE CHARACTERISTICS

- First EPROM offering 16 inputs and outputs
- Fast access time — 100 ns
- Low power consumption:
  - 200  $\mu$ A maximum standby current
- Programming voltage: 12.5 V
- Single +5-V power supply
- JEDEC-approved 40-pin DIP and 44-pad LCC pinouts
- $\pm 10\%$  power supply tolerance available
- One-Time Programmable (OTP) Flashrite™ programming
- Latch-up protected to 100 mA from  $-1$  V to  $V_{CC} + 1$  V

## GENERAL DESCRIPTION

The Am27C1024 is a 1 megabit, ultraviolet erasable programmable read-only memory. It is organized as 64K words by 16 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. The x16 organization makes the Am27C1024 ideal for use in 16-bit microprocessor systems. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

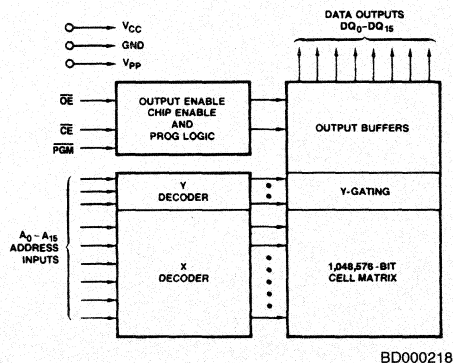
Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors with reduced WAIT states. The Am27C1024 offers sepa-

rate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 350  $\mu$ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C1024 supports AMD's interactive programming algorithm (0.5 ms pulses) resulting in typical programming times of less than two minutes.

## BLOCK DIAGRAM



BD000218

## PRODUCT SELECTOR GUIDE

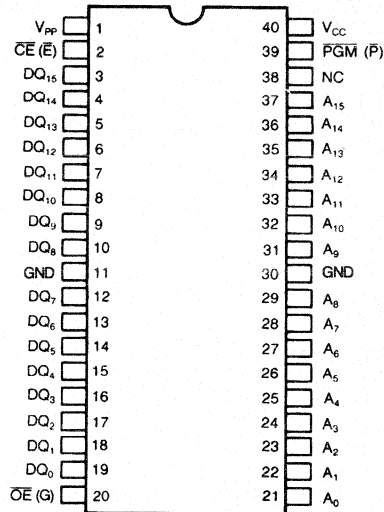
Family Part No.	Am27C1024							
Ordering Part No:								
$\pm 5\%$ $V_{CC}$ Tolerance	-105	-125	-155	-175	-205	-255	-305	-
$\pm 10\%$ $V_{CC}$ Tolerance	-100	-120	-150	-170	-200	-250	-300	-350
Max. Access Time (ns)	120	120	150	170	200	250	300	350
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	120	120	150	170	200	250	300	350
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	50	50	65	65	75	100	120	120

Flashrite is a trademark of Advanced Micro Devices Inc.

Publication #	Rev.	Amendment
06780	D	/0
Issue Date: January 1989		

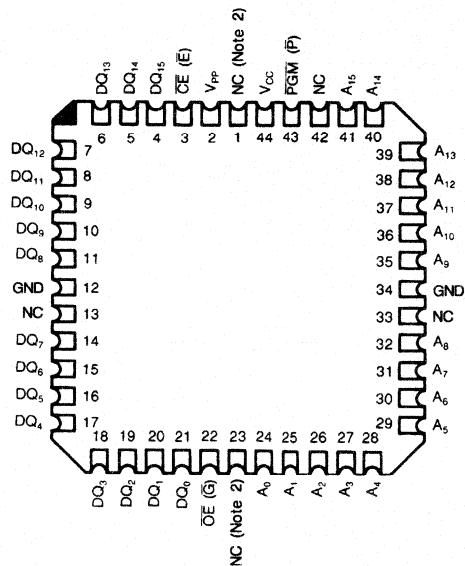
## CONNECTION DIAGRAMS Top View

### DIPs



CD009304

### LCC\*



CD009317

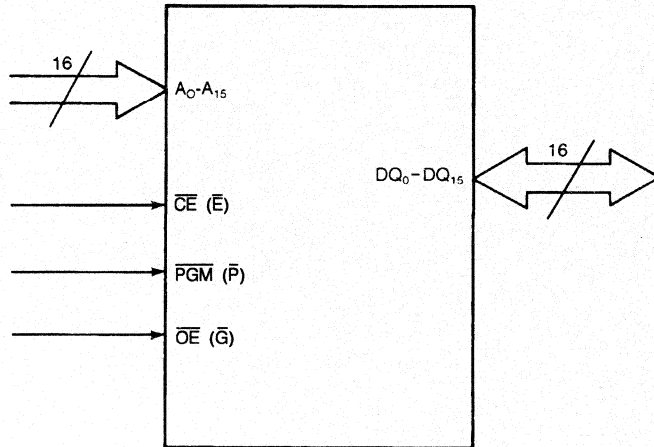
\*Also available in a 44-Pin plastic leaded chip carrier.

Notes: 1. JEDEC nomenclature is in parentheses

2. Don't use (DU) for PLCC

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## LOGIC SYMBOL



LS003320

### Pin Description

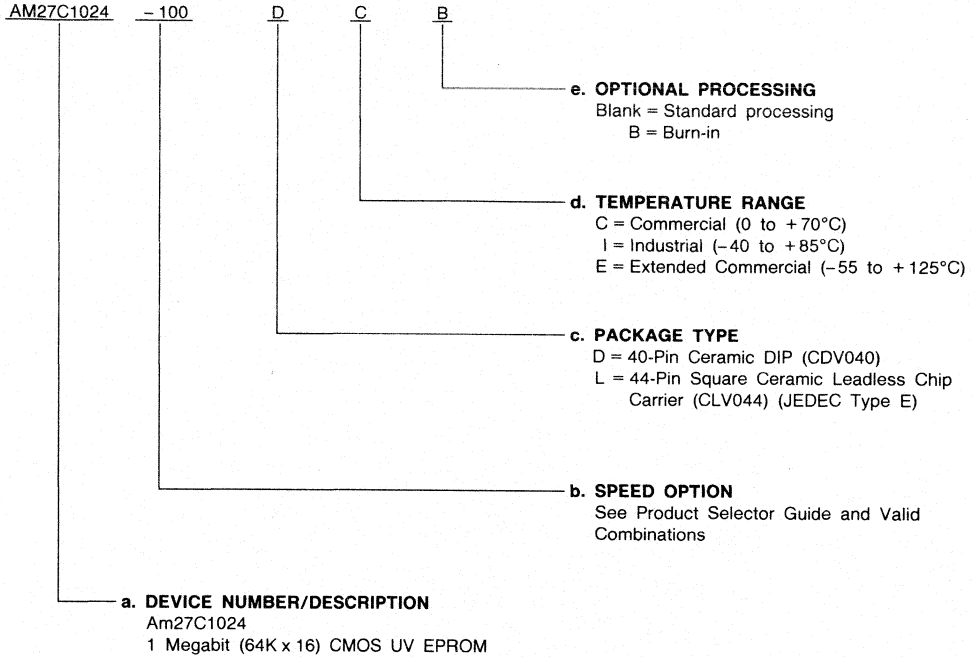
$A_0-A_{15}$	= Address Inputs
$\overline{CE}(\overline{E})$	= Chip Enable Input
$DQ_0-DQ_{15}$	= Data Input/Outputs
$\overline{OE}(\overline{G})$	= Output Enable Input
$\overline{PGM}(\overline{P})$	= Program Enable Input
$V_{CC}$	= $V_{CC}$ Supply Voltage
$V_{PP}$	= Program Supply Voltage
GND	= Ground
NC	= No Internal Connect
DU	= No External Connect

# ORDERING INFORMATION

## Standard Information

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Optional Processing



3

Valid Combinations	
AM27C1024-100	DC, DCB
AM27C1024-105	
AM27C1024-120	
AM27C1024-125	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C1024-150	
AM27C1024-155	
AM27C1024-175	
AM27C1024-255	
AM27C1024-305	
AM27C1024-170	
AM27C1024-200	
AM27C1024-250	
AM27C1024-300	

### Valid Combinations

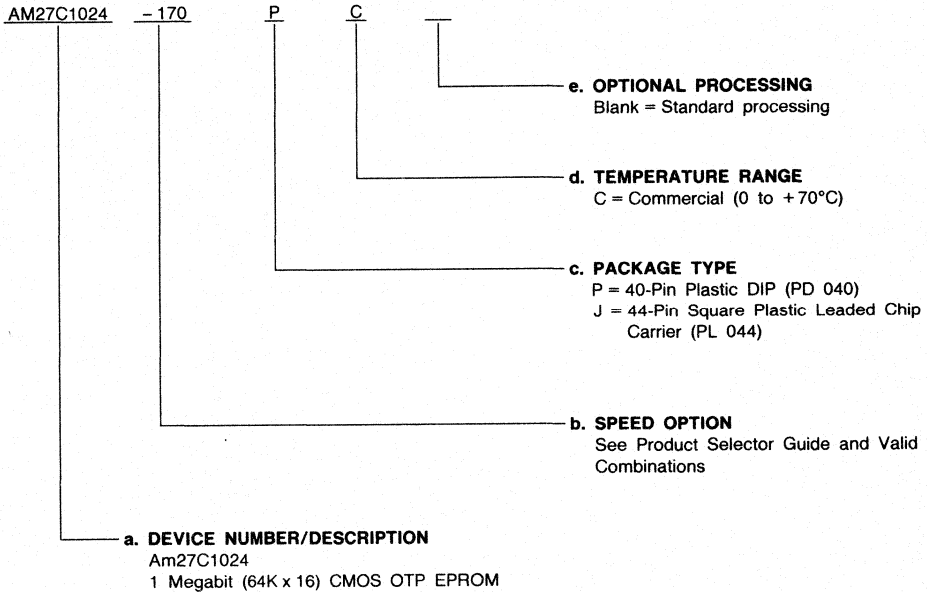
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION (Cont'd.)

### OTP Products (Preliminary)

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option**
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM27C1024-170	PC, JC
AM27C1024-175	
AM27C1024-200	
AM27C1024-205	
AM27C1024-250	
AM27C1024-255	
AM27C1024-300	
AM27C1024-305	

#### Valid Combinations

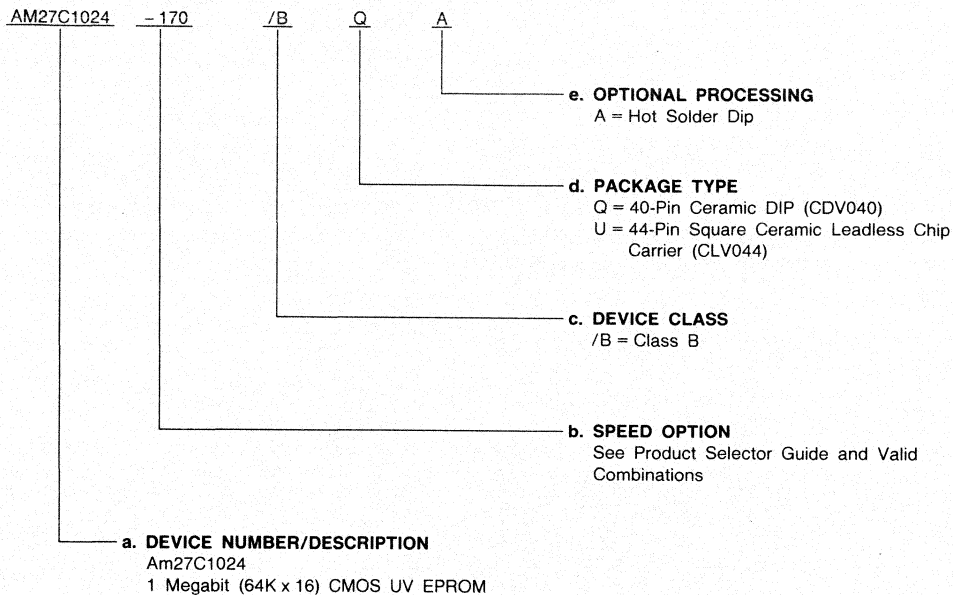
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM27C1024-170	/BQA, /BUA
AM27C1024-200	
AM27C1024-250	
AM27C1024-300	
AM27C1024-350	

For other Surface Mount Package options, contact NVD Military Marketing.

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## FUNCTIONAL DESCRIPTION

### Erasing the Am27C1024

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C1024 to an ultraviolet light source. A dosage of 15 W seconds/cm<sup>2</sup> is required to completely erase an Am27C1024. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm<sup>2</sup> for 15 to 20 minutes. The Am27C1024 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C1024, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C1024 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

### Programming the Am27C1024

Upon delivery, or after each erasure, the Am27C1024 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROS" are loaded into the Am27C1024 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5 V is applied to the V<sub>pp</sub> pin, and  $\overline{CE}$  and  $\overline{PGM}$  are at V<sub>IL</sub>.

For programming, the data to be programmed is applied 16 bits in parallel to the data pins.

The flowchart in Figure 1 shows AMD's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C1024. This part of the algorithm is done at V<sub>CC</sub> = 6.0 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at V<sub>CC</sub> = 5 V ± 5%.

### Flashrite™

The OTP EPROM Flashrite programming algorithm (shown in Figure 2) reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the OTP EPROM.

The Flashrite programming algorithm programs and verifies at V<sub>CC</sub> = 6.25 V and V<sub>pp</sub> = 12.75 V. After the final address is completed, all bytes are compared to the original data with V<sub>CC</sub> = V<sub>pp</sub> = 5.25 V.

### Program Inhibit

Programming of multiple Am27C1024s in parallel with different data is also easily accomplished. Except for  $\overline{CE}$ , all like inputs of the parallel Am27C1024 may be common. A TTL low-level program pulse applied to an Am27C1024  $\overline{CE}$  input with V<sub>pp</sub> = 12.5 ± 0.5 V and  $\overline{PGM}$  LOW will program that

Am27C1024. A high-level  $\overline{CE}$  input inhibits the other Am27C1024s from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with  $\overline{OE}$  and  $\overline{CE}$ , at V<sub>IL</sub>, PGM at V<sub>IH</sub>, and V<sub>pp</sub> between 12.0 V to 13.0 V.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C1024.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A<sub>9</sub> of the Am27C1024. Two identifier bytes may then be sequenced from the device outputs by toggling address line A<sub>0</sub> from V<sub>IL</sub> to V<sub>IH</sub>. All other address lines must be held at V<sub>IL</sub> during auto select mode.

Byte 0 (A<sub>0</sub> = V<sub>IL</sub>) represents the manufacturer code, and byte 1 (A<sub>0</sub> = V<sub>IH</sub>), the device identifier code. For the Am27C1024, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ<sub>7</sub>) defined as the parity bit.

### Read Mode

The Am27C1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t<sub>ACC</sub>) is equal to the delay from  $\overline{CE}$  to output (t<sub>CE</sub>). Data is available at the outputs t<sub>OE</sub> after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least t<sub>ACC</sub> - t<sub>OE</sub>.

### Standby Mode

The Am27C1024 has a CMOS standby mode which reduces the maximum V<sub>CC</sub> current to 200 μA. It is placed in CMOS-standby when  $\overline{CE}$  is at V<sub>CC</sub> ± 0.3 V. The Am27C1024 also has a TTL-standby mode which reduces the maximum V<sub>CC</sub> current to 1.0 mA. It is placed in TTL-standby when  $\overline{CE}$  is at V<sub>IH</sub>. When in standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading



of the device. At a minimum, a 0.1- $\mu$ F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM

arrays, a 4.7- $\mu$ F bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

**MODE SELECT TABLE**

PINS		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	$A_0$	$A_9$	$V_{PP}$	OUTPUTS
Read		$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	$V_{CC}$	D <sub>OUT</sub>
Output Disable		$V_{IL}$	$V_{IH}$	$V_{IH}$	X	X	$V_{CC}$	High Z
Standby (TTL)		$V_{IH}$	X	X	X	X	$V_{CC}$	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	$V_{CC}$	High Z
Program		$V_{IL}$	X	$V_{IL}$	X	X	$V_{PP}$	D <sub>IN</sub>
Program Verify		$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$	D <sub>OUT</sub>
Program Inhibit		$V_{IH}$	X	X	X	X	$V_{PP}$	High Z
Auto Select (Note 3)	Manufacturer Code	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_H$	$V_{CC}$	01H
	Device Code	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_H$	$V_{CC}$	8CH

- Notes: 1. X can be either  $V_{IL}$  or  $V_{IH}$   
 2.  $V_H = 12.0$  V  $\pm 0.5$  V  
 3.  $A_1$ - $A_8 = A_{10}$  -  $A_{15} = V_{IL}$   
 4. See DC Programming Characteristics for  $V_{PP}$  voltage during programming.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	-65 to +125°C
All Other Products	-65 to +150°C
Ambient Temperature	
with Power Applied	-55 to +125°C
Voltage with Respect to Ground:	
All pins except A <sub>9</sub> , V <sub>PP</sub> , and	
V <sub>CC</sub>	-0.6 to V <sub>CC</sub> + 0.5 V
A <sub>9</sub> and V <sub>PP</sub>	-0.6 to 13.5 V
V <sub>CC</sub>	-0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

- Notes: 1. Minimum DC voltage on input or I/O is -0.5 V. During transitions, the inputs may undershoot GND to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O is V<sub>CC</sub> + 0.5 V which may overshoot to V<sub>CC</sub> + 2.0 V for periods up to 20 ns.
2. For A<sub>9</sub> and V<sub>PP</sub> the minimum DC input is -0.5 V. During transitions, A<sub>9</sub> and V<sub>PP</sub> may undershoot GND to -2.0 V for periods of up to 20 ns. A<sub>9</sub> and V<sub>PP</sub> must not exceed 13.5 V for any period of time.

## OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T <sub>C</sub> )	0 to +70°C
Industrial (I) Devices	
Case Temperature (T <sub>C</sub> )	-40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T <sub>C</sub> )	-55 to +125°C
Military (M) Devices	
Case Temperature (T <sub>C</sub> )	-55 to +125°C
Supply Read Voltages:	
V <sub>CC</sub> /V <sub>PP</sub> for Am27C1024-XX5	+4.75 to +5.25 V
V <sub>CC</sub> /V <sub>PP</sub> for Am27C1024-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

### TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -400 μA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA		0.45	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	+0.8	V
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0 V to V <sub>CC</sub>		1.0	μA
				5.0	
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>		10	μA
				10	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$ , f = 5 MHz, I <sub>OUT</sub> = 0 mA (Open Outputs)		50	mA
				60	
I <sub>CC2</sub>	V <sub>CC</sub> Standby Current (Note 9)	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$		1.0	mA
				1.5	
I <sub>PP1</sub>	V <sub>PP</sub> Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$ , V <sub>PP</sub> = V <sub>CC</sub>		100	μA

### CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -400 μA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA		0.45	V
V <sub>IH</sub>	Input HIGH Voltage		V <sub>CC</sub> - 0.3	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	+0.8	V
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0 V to V <sub>CC</sub>		1.0	μA
				5.0	

## DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4 & 5) (Cont'd.)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>	C/I Devices		10	μA
			E/M Devices		10	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current (Notes 5 & 9)	$\overline{CE} = V_{IL}$ , f = 5 MHz, I <sub>OUT</sub> = 0 mA (Open Outputs)	C/I Devices		50	mA
			E/M Devices		60	
I <sub>CC2</sub>	V <sub>CC</sub> Standby Current (Note 9)	$\overline{CE} = V_{CC} \pm 0.3$ V	C/I Devices		200	μA
			E/M Devices		240	
I <sub>PP1</sub>	V <sub>PP</sub> Supply Current (Read) (Notes 6 & 9)	$\overline{CE} = \overline{OE} = V_{IL}$ , V <sub>PP</sub> = V <sub>CC</sub>			100	μA

## CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV040		CLV044		Unit
			Typ.	Max.	Typ.	Max.	
C <sub>IN1</sub>	Address Input Capacitance	V <sub>IN</sub> = 0 V	8	12	6	9	pF
C <sub>IN2</sub>	$\overline{OE}$ Input Capacitance	V <sub>IN</sub> = 0 V	12	20	9	15	pF
C <sub>IN3</sub>	$\overline{CE}$ Input Capacitance	V <sub>IN</sub> = 0 V	9	12	7	9	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0 V	8	12	6	9	pF

- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>pp</sub>, and removed simultaneously or after V<sub>pp</sub>.  
2. Typical values are for nominal supply voltages.  
3. This parameter is only sampled and not 100% tested.  
4. **Caution:** The Am27C1024 must not be removed from, or inserted into, a socket or board when V<sub>pp</sub> or V<sub>CC</sub> is applied.  
5. I<sub>CC1</sub> is tested with  $\overline{OE} = V_{IH}$  to simulate open outputs.  
6. Maximum active power usage is the sum of I<sub>CC</sub> and I<sub>pp</sub>.  
7. T<sub>A</sub> = 25°C, f = 1 MHz.  
8. Minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for periods less than 20 ns.  
Maximum DC voltage on output pins is V<sub>CC</sub> + 0.5 V which may overshoot to V<sub>CC</sub> + 2.0 V for periods less than 20 ns.  
9. For Am27C1024-305 I<sub>CC2</sub> (TTL) = 5 mA, I<sub>CC2</sub> (CMOS) = 1 mA, I<sub>pp</sub> = 1 mA maximum.

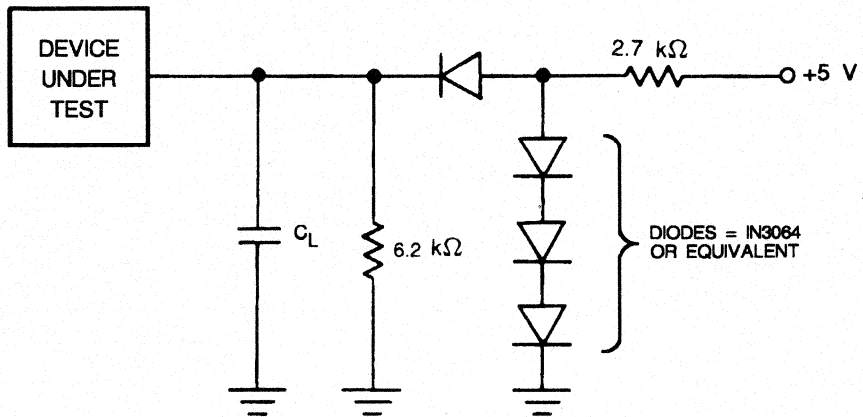
3

## SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

JEDEC	Standard	Parameter Description	Test Conditions	Am27C1024								Unit	
				-100, -105	-120, -125	-150, -155	-170, -175	-200, -205	-250, -255	-300, -305	-350, -		
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.									ns
				Max.	100	120	150	170	200	250	300	350	
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.									ns
				Max.	100	120	150	170	200	250	300	350	
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.									ns
				Max.	50	50	65	65	75	100	120	120	
t <sub>EHQZ</sub> , t <sub>GHQZ</sub>	t <sub>DF</sub>	Output Enable HIGH to Output Float (Note 2)		Min.	0	0	0	0	0	0	0	0	ns
				Max.	50	50	50	50	60	60	60	80	
t <sub>AXQX</sub>	t <sub>OH</sub>	Output Hold from Addresses, $\overline{CE}$ , or $\overline{OE}$ , whichever occurred first		Min.	0	0	0	0	0	0	0	0	ns
				Max.	-	-	-	-	-	-	-	-	

- Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>pp</sub>, and removed simultaneously or after V<sub>pp</sub>.  
2. This parameter is only sampled and not 100% tested.  
3. **Caution:** The Am27C1024 must not be removed from, or inserted into, a socket or board when V<sub>pp</sub> or V<sub>CC</sub> is applied.  
4. Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF, Input Rise and Fall Times: 20 ns, Input Pulse Levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V  
Outputs: 0.8 V and 2 V

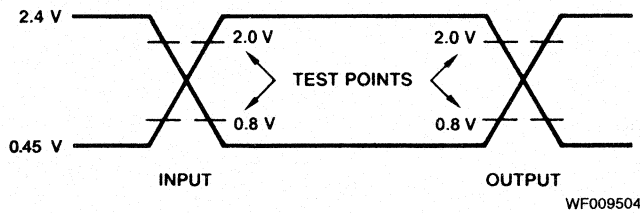
## SWITCHING TEST CIRCUITS



TC003195

$C_L = 100 \text{ pF}$  including jig capacitance






## SWITCHING TEST WAVEFORMS



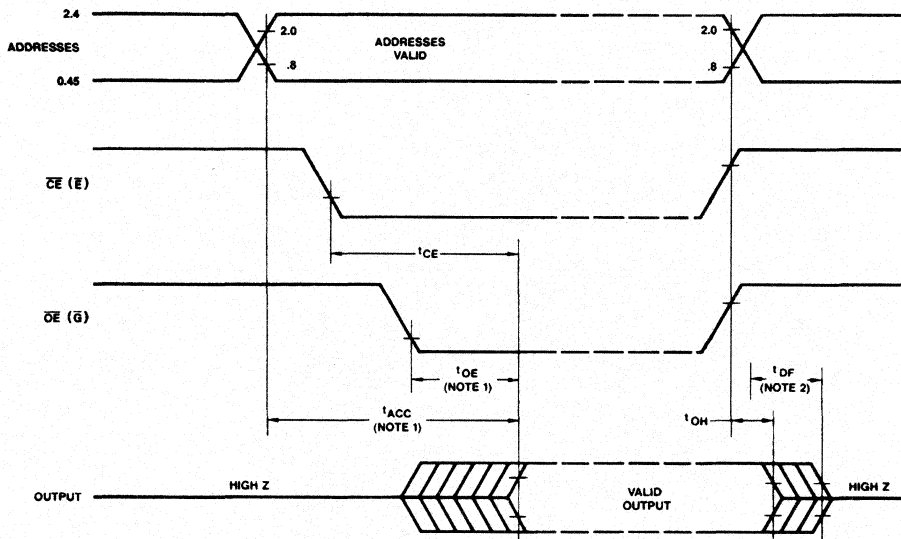
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are  $\leq 20 \text{ ns}$ .

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



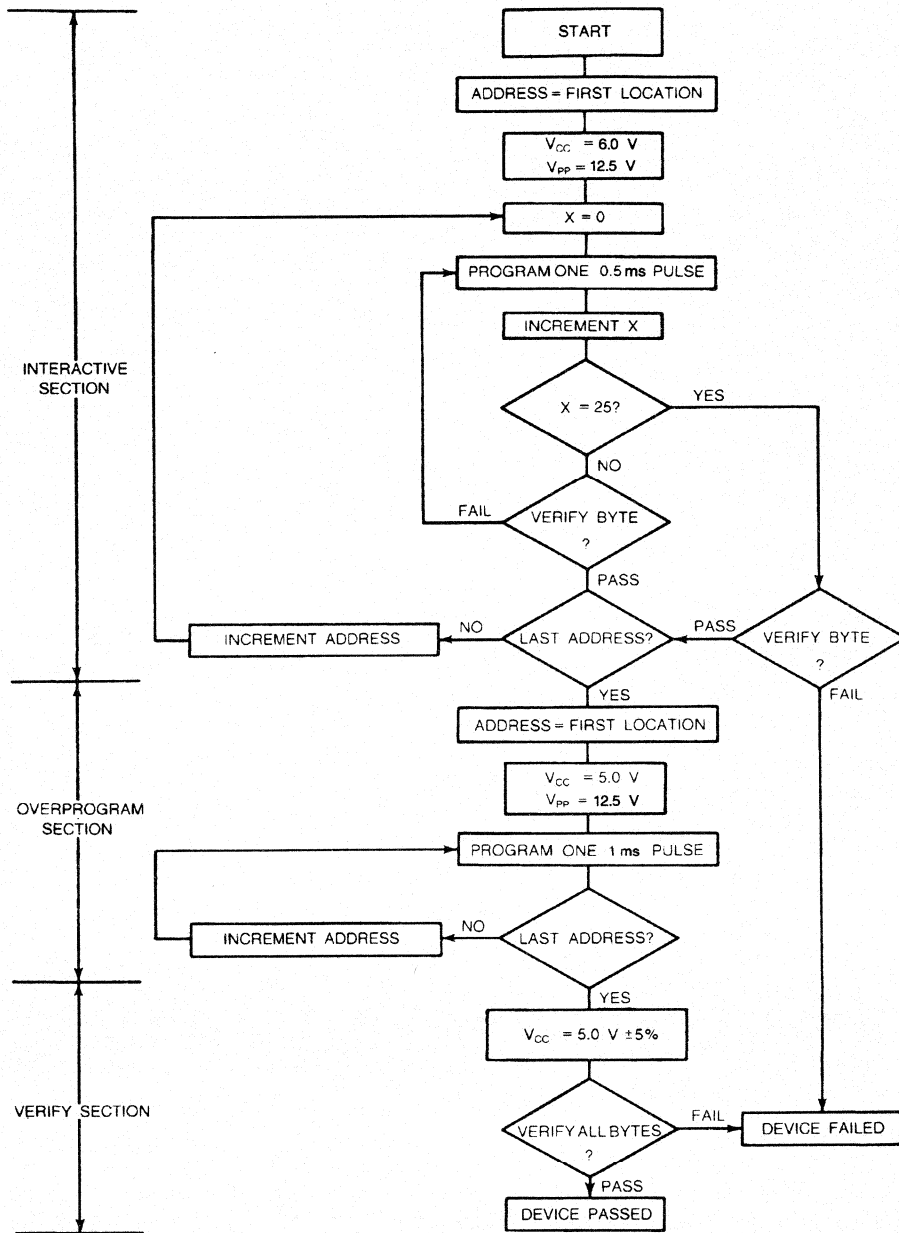
WF001296

### Read Cycle

- Notes: 1.  $\overline{OE}$ (G) may be delayed up to  $t_{ACC}-t_{OE}$  after the falling edge of  $\overline{CE}$ (E) without impact on  $t_{ACC}$ .  
 2.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.

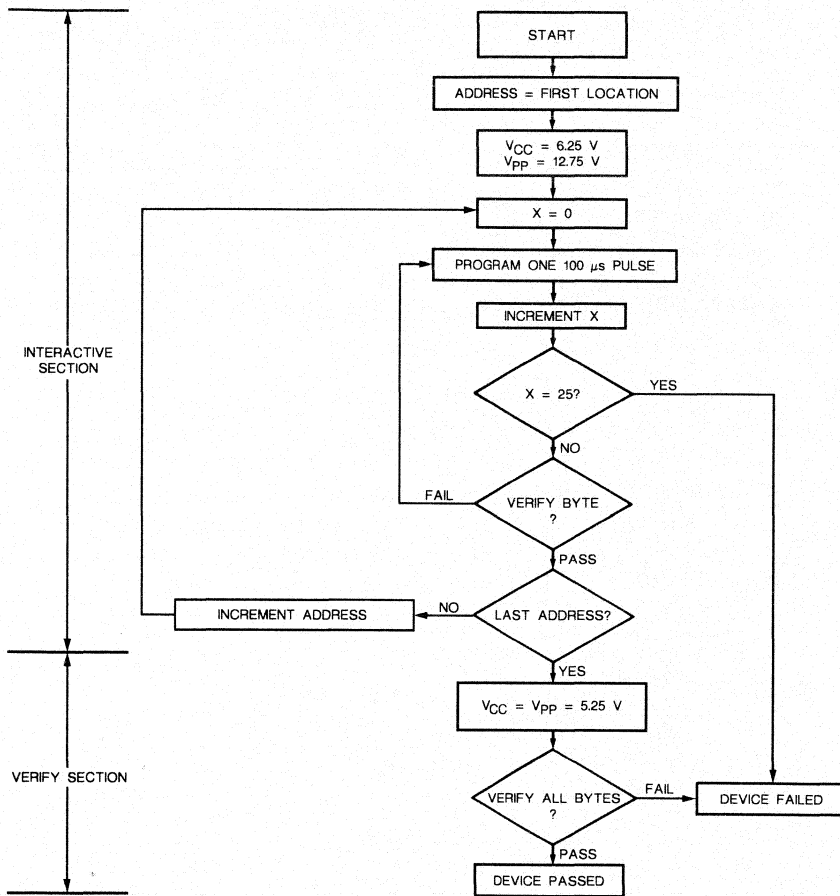
3

## PROGRAMMING FLOW CHARTS



PF002850

Figure 1. Interactive Programming Flow Chart



10205B-008A  
PF002490

Figure 2. Flashrite Programming Flow Chart for OTP EPROM

## DC PROGRAMMING CHARACTERISTICS (T<sub>A</sub> = +25°C ±5°C) (Notes 1, 2, & 3).

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I <sub>LI</sub>	Input Current (All Inputs)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>		10.0	μA
V <sub>IL</sub>	Input LOW Level (All Inputs)		-0.3	0.8	V
V <sub>IH</sub>	Input HIGH Level		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output LOW Voltage During Verify	I <sub>OL</sub> = 2.1 mA		0.45	V
V <sub>OH</sub>	Output HIGH Voltage During Verify	I <sub>OH</sub> = -400 μA	2.4		V
V <sub>H</sub>	A <sub>9</sub> Auto Select Voltage		11.5	12.5	V
I <sub>CC3</sub>	V <sub>CC</sub> Supply Current (Program & Verify)			50	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current (Program)	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$		50	mA
V <sub>CC1</sub>	Interactive Supply Voltage		5.75	6.25	V
V <sub>PP1</sub>	Interactive Programming Voltage		12.0	13.0	V
V <sub>CC2</sub>	Flashrite Supply Voltage		6.00	6.50	V
V <sub>PP2</sub>	Flashrite Programming Voltage		12.5	13.0	V

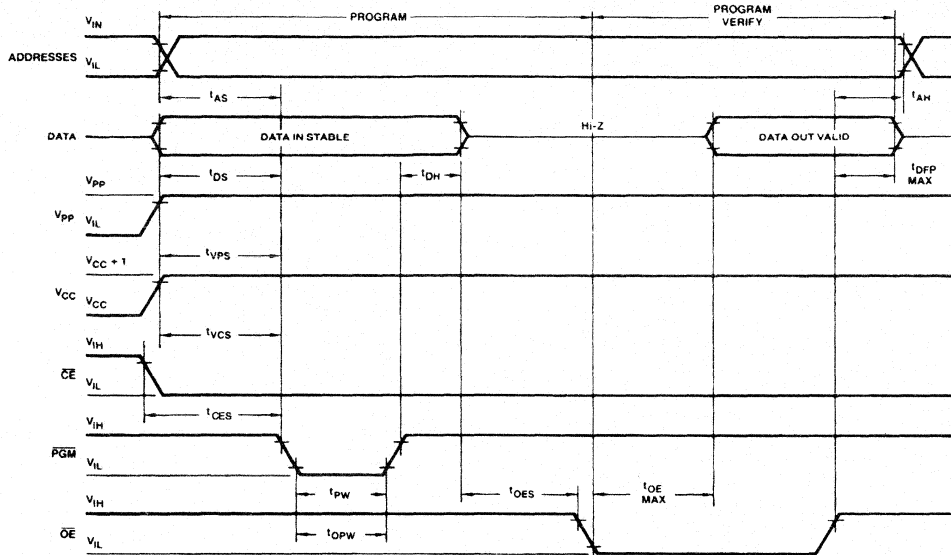
## SWITCHING PROGRAMMING CHARACTERISTICS (T<sub>A</sub> = +25°C ±5°C) (Notes 1, 2, & 3).

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t <sub>AVEL</sub>	t <sub>AS</sub>	Address Setup Time	2		μs
t <sub>DZGL</sub>	t <sub>OES</sub>	$\overline{OE}$ Setup Time	2		μs
t <sub>DVEL</sub>	t <sub>DS</sub>	Data Setup Time	2		μs
t <sub>GHAX</sub>	t <sub>AH</sub>	Address Hold Time	0		μs
t <sub>EHDX</sub>	t <sub>DH</sub>	Data Hold Time	2		μs
t <sub>GHQZ</sub>	t <sub>DFP</sub>	Output Enable to Output Float Delay	0	130	ns
t <sub>VPS</sub>	t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	2		μs
t <sub>ELEH1</sub>	t <sub>PW</sub>	Flashrite	95	105	μs
		Interactive	0.45	0.55	ms
t <sub>ELEH2</sub>	t <sub>OPW</sub>	$\overline{PGM}$ Overprogram Pulse Width (Interactive)	0.95	1.05	ms
t <sub>VCS</sub>	t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	2		μs
t <sub>ELPL</sub>	t <sub>CES</sub>	$\overline{CE}$ Setup Time	2		μs
t <sub>GLQV</sub>	t <sub>OE</sub>	Data Valid from $\overline{OE}$		150	ns

- Notes:**
1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.
  2. When programming the Am27C1024, a 0.1-μF capacitor is required across V<sub>PP</sub> and ground to suppress spurious voltage transients which may damage the device.
  3. Programming characteristics are sampled but not 100% tested at worst-case conditions.



**PROGRAMMING ALGORITHM WAVEFORMS** (Notes 1 & 2)



WF000555

- Notes: 1. The input timing reference level is 0.8 for  $V_{IL}$  and 2 V for  $V_{IH}$ .  
 2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device, but must be accommodated by the programmer.

# Am27C020

2 MBit (256K x 8) CMOS EPROM



Advanced  
Micro  
Devices

## DISTINCTIVE CHARACTERISTICS

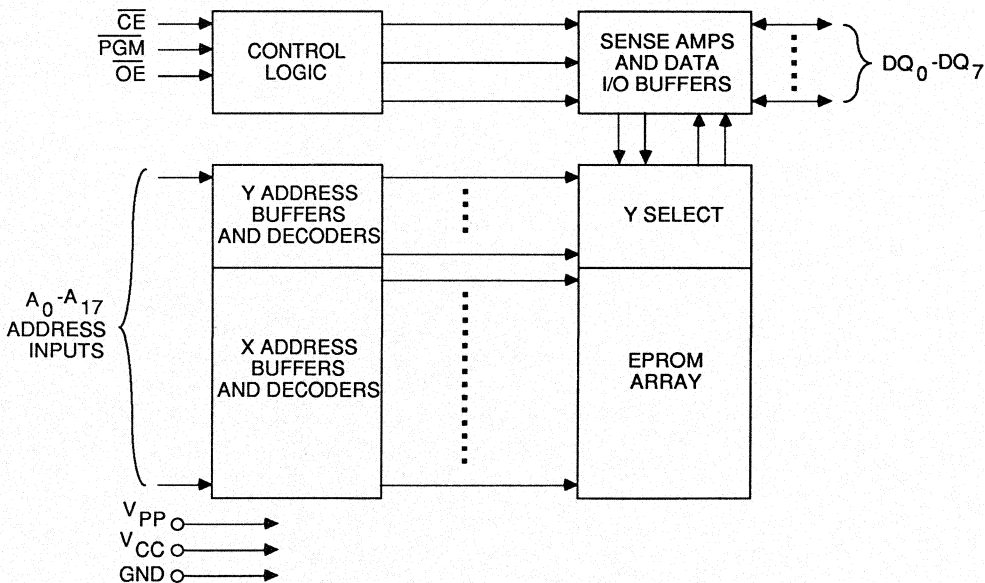
- High-performance CMOS technology
- Fast access time
  - 100 ns
- Low power dissipation
  - 100  $\mu$ A maximum standby current
- Easy upgrade from 28-pin JEDEC EPROMs
- Compact 32-pin DIP package requires no hardware change for upgrades to 8 Mbit
- Flashrite™ programming
- Ceramic DIP and LCC packages
- Latch-up protected to 100 mA from  $-1$  V to  $V_{cc} +1$  V

## GENERAL DESCRIPTION

The Am27C020 is a 2,097,152-bit ultraviolet-light-erasable, programmable read-only memory (UV EPROM) device organized as 256K bytes of 8 bits each. Its pin compatibility with byte-wide JEDEC EPROMs allows easy upgrades from 512K through 8-Mbit densities. AMD's CMOS process technology provides high-speed and low power consumption.

The standard Am27C020 offers access times as fast as 150 ns, allowing operation with high-speed microprocessors without any wait states. The Am27C020 also offers separate Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) controls, which eliminates bus contention in a multiple-bus microprocessor system.

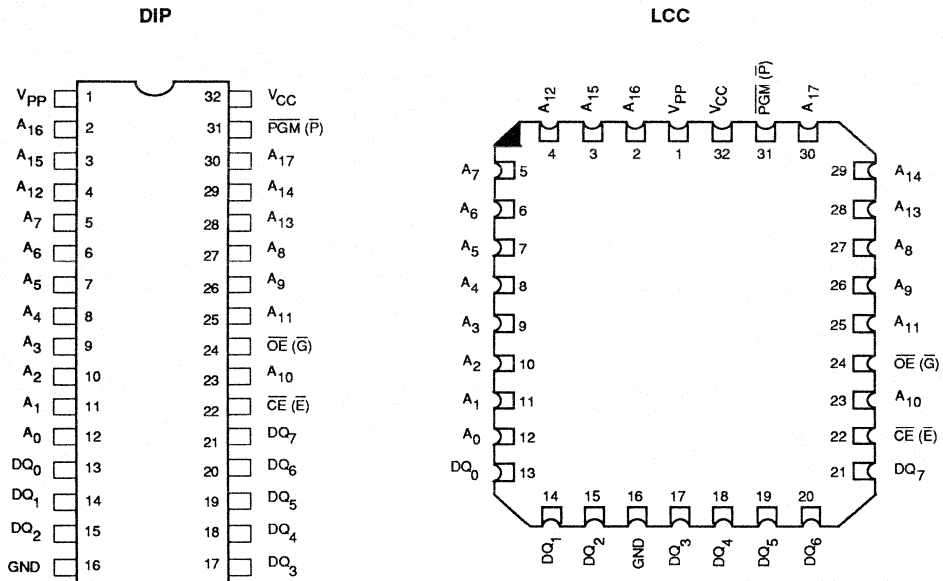
## BLOCK DIAGRAM



11507-001A

## CONNECTION DIAGRAMS

### Top View

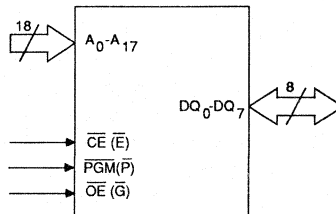


- Note: 1. JEDEC nomenclature is in parentheses.  
 2. The 32-Pin DIP to 32-Pin LCC configuration varies from the JEDEC 28-Pin DIP to 32-Pin LCC configuration.

11507-002A

3

### LOGIC SYMBOL



11507-003A

### Pin Description

- $A_0$ – $A_{17}$  = Address Inputs
- $\overline{CE}$  ( $\overline{E}$ ) = Chip Enable Input
- $DQ_0$ – $DQ_7$  = Data Input/Outputs
- $\overline{OE}$  ( $\overline{G}$ ) = Output Enable Input
- $\overline{PGM}$  ( $\overline{P}$ ) = Program Enable Input
- $V_{CC}$  =  $V_{CC}$  Supply Voltage
- $V_{PP}$  = Program Supply Voltage
- GND = Ground



# Am27C2048

131,072 x 16-Bit CMOS UV EPROM

## DISTINCTIVE CHARACTERISTICS

- Fast access time — 100 ns
- Low power consumption:
  - 100  $\mu$ A maximum standby current
- Programming voltage: 12.5 V
- Single +5-V power supply
- JEDEC-approved pinout
- $\pm 10\%$  power supply tolerance available
- Flashrite™ programming
- Latch-up protected to 100 mA from  $-1$  V to  $V_{CC} + 1$  V

## GENERAL DESCRIPTION

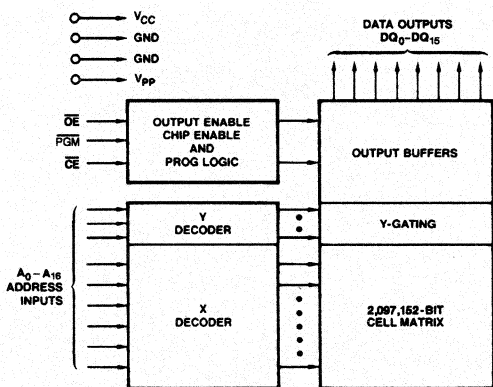
The Am27C2048 is a 2 megabit, ultraviolet erasable programmable read-only memory. It is organized as 131,072 words by 16 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without WAIT states. The Am27C2048 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 500  $\mu$ W in standby mode.

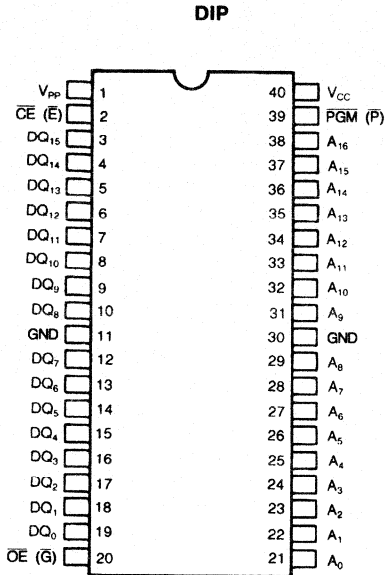
All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C2048 supports both AMD's interactive programming algorithm (0.5 ms pulses) and Flashrite algorithm (0.1 ms pulses).

## BLOCK DIAGRAM

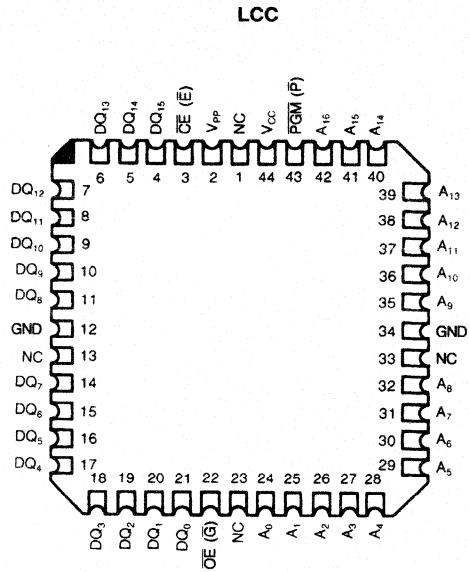


BD008370

## CONNECTION DIAGRAMS Top View



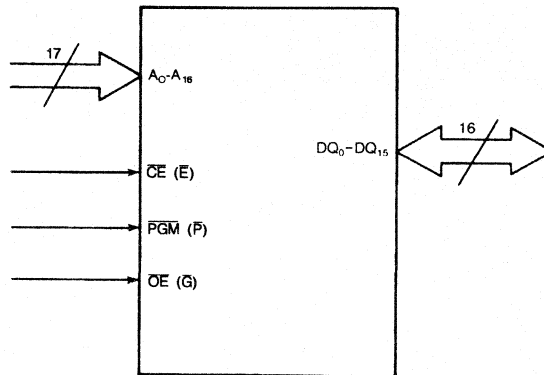
CD009305



CD009318

Note: 1. JEDEC nomenclature is in parentheses.

## LOGIC SYMBOL



LS002299

V<sub>CC</sub> = 5.0-V Power Supply  
 GND = 0-V Power Supply  
 V<sub>PP</sub> = 12.5 V Power Supply



# Am27C4096

262,144 x 16-Bit CMOS UV EPROM

Advanced  
Micro  
Devices

## DISTINCTIVE CHARACTERISTICS

- Fast access time — 120 ns
- Low power consumption:
  - 100  $\mu$ A maximum standby current
- Programming voltage: 12.5 V
- Single +5-V power supply
- JEDEC-approved pinout
- $\pm 10\%$  power supply tolerance available
- Flashrite™ programming
- Latch-up protected to 100 mA from -1 V to  $V_{CC} + 1$  V

## GENERAL DESCRIPTION

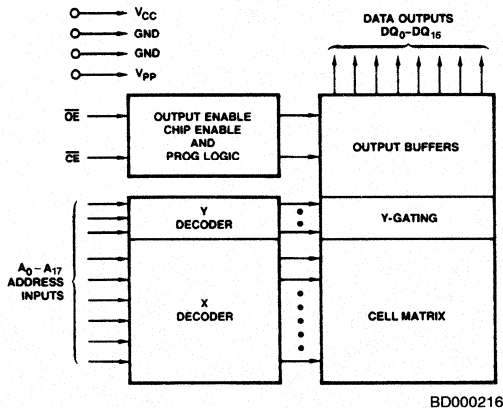
The Am27C4096 is a 4 megabit, ultraviolet erasable programmable read-only memory. It is organized as 262,144 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming.

Typically, any byte can be accessed in less than 120 ns, allowing operation with high-performance microprocessors with reduced WAIT states. The Am27C4096 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus microprocessor system.

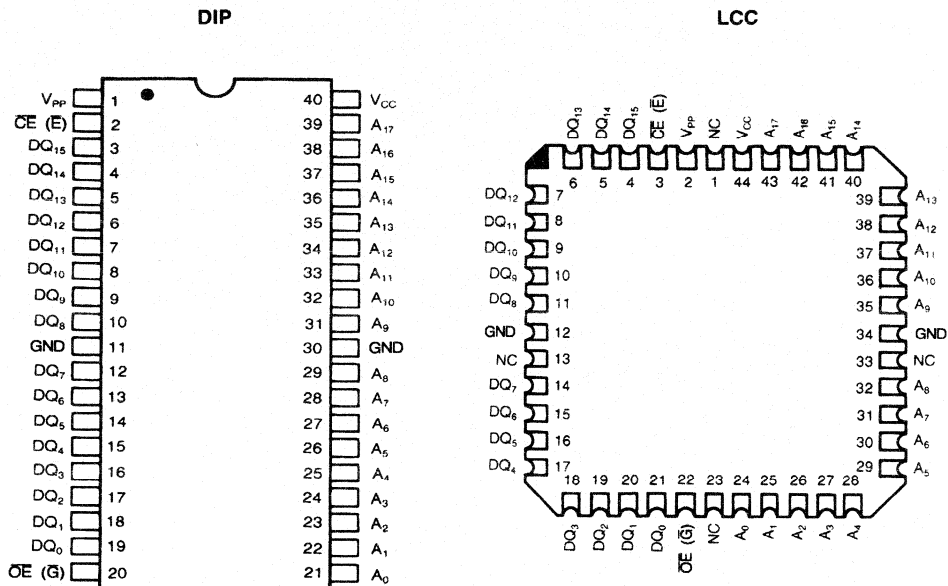
AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 500  $\mu$ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C4096 supports both AMD's interactive programming algorithm (1-ms pulses) and Flashrite algorithm (0.1 ms pulses).

## BLOCK DIAGRAM



## CONNECTION DIAGRAMS Top View



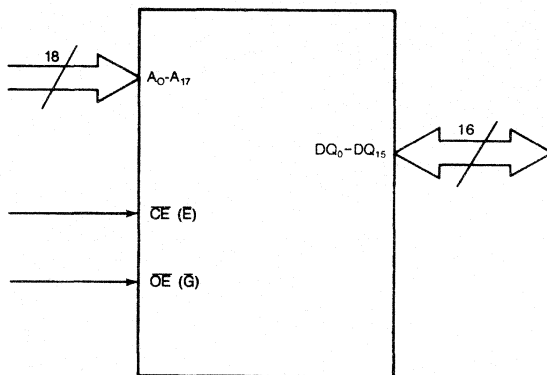
CD009302

CD009316

Notes: 1. Pin 1 is marked for orientation.

3

### LOGIC SYMBOL



LS002298

V<sub>CC</sub> = 5.0-V Power Supply  
 GND = 0-V Power Supply  
 V<sub>PP</sub> = 12.5 V Power Supply

# EPROM SPEEDS FOR POPULAR MICROPROCESSORS

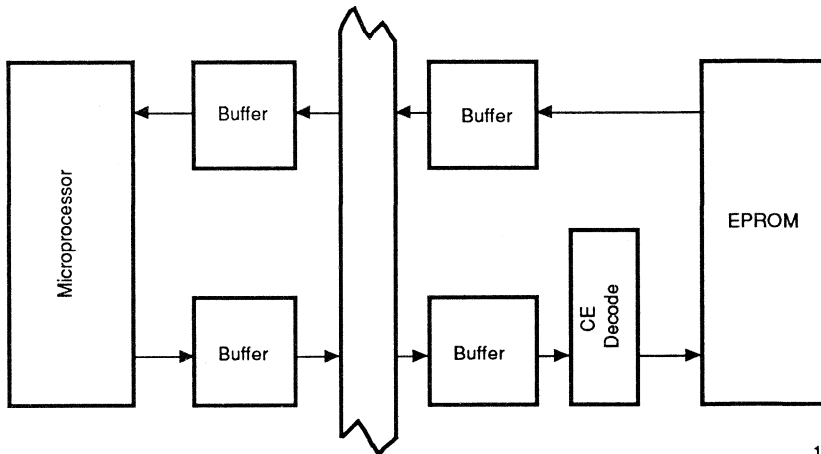
by  
Ken Pope



The speed of a microprocessor is determined by the clock frequency at which it can operate, the number of cycles per instruction, and the speed of the external devices (memories, peripherals, etc.). If the memory access is slow, the system throughput will be slow no matter how fast the clock frequency is. When the memory is seldom accessed (diagnostics or a boot EPROM) it is cost effective to use slower EPROMs which create wait states. This will not degrade throughput significantly and will allow cost savings. For memories

that incorporate operating systems or other heavily used code wait states are intolerable because the overall performance is degraded dramatically.

The following table shows access times that can be expected over a number of microprocessors at their rated frequencies. This table is based on the microprocessor based system shown in Figure 1.



**Figure 1.**

The buffer delays are 7.5 ns and the logic delay is 4 ns. If faster buffers or logic are used, EPROM access time increases.



## EPROM Speeds for Popular Microprocessors

### TABLE 1

Processor	Frequency	Wait States	EPROM Access
80C31	16 MHz	-	150 ns
80C186	12 MHz	0	150 ns
	16 MHz	0	120 ns
	16 MHz	1	150 ns
80C196	10 MHz	-	150 ns
	12 MHz	-	100 ns
80186	10 MHz	0	200 ns
	12 MHz	0	150 ns
	12 MHz	1	350 ns
80286	12 MHz	0	120 ns
	16 MHz	0	90 ns
	16 MHz	1	170 ns
80386	16 MHz	0	90 ns
	20 MHz	0	70 ns
	20 MHz	1	120 ns
68000	12 MHz	0	150 ns
68010	12 MHz	0	150 ns
	16 MHz	0	100 ns
	16 MHz	1	150 ns
29000	25 MHz	0	55 ns*

\* Bank interleaved

# Am2864AE

8192 x 8-Bit Electrically Erasable PROM



## DISTINCTIVE CHARACTERISTICS

- 5-V only operation
- Military temperature range available
- Self-timed Write Cycle with on-chip latches
- Data Polling for end-of-write indication
- Data protection features to prevent writes from occurring during V<sub>CC</sub> power-up/down
- 32-byte page write mode
- Minimum endurance of 10,000 write cycles per byte with a 10-year retention. For detailed information, see the reliability section within this Handbook.
- Allows WE and CE controlled Writes

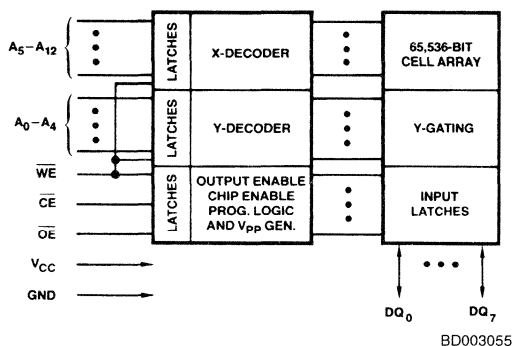
## GENERAL DESCRIPTION

The Am2864AE is a 65,536-bit Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 8192 words by 8 bits per word. It operates from a single 5-volt supply and has a fully self-timed write cycle with address, data, and control lines latched during the write operation. The 32-byte page write mode allows programming in as little as 2.6 seconds. The Am2864AE is fabricated on AMD's highly manufacturable N-Channel Silicon gate process, and uses AMD's proprietary EEPROM

technology to achieve electrically alterable nonvolatile storage. This technology employs the industry-accepted Fowler-Nordheim tunneling across a thin oxide.

The Am2864AE provides the on-chip logic necessary to interface with most microprocessors. The latched inputs and self-timed write cycle free the microprocessor to perform other tasks during a write. A transparent automatic erase before write enhances system performance.

## BLOCK DIAGRAM



## MODE SELECT TABLE

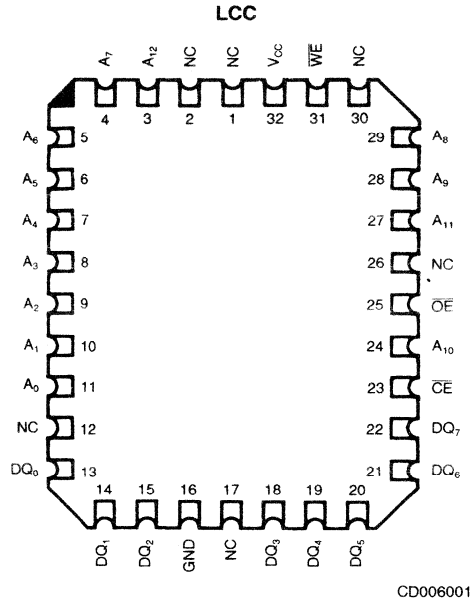
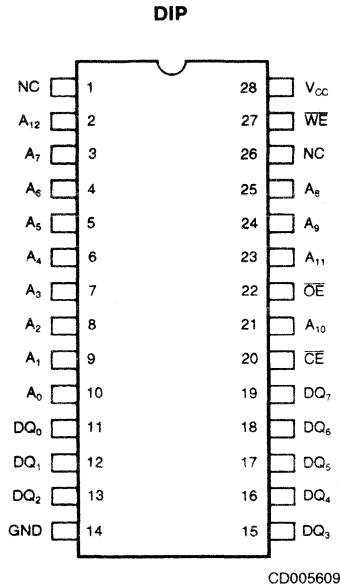
Inputs			Outputs		
CE	OE	WE	I/O	A <sub>9</sub>	Mode
L	L	H	Data Out	X	Read
L	H	H	Data In	X	Write
$\overline{\text{Pulse}}$	H	L	Data In	X	Write
H	X	X	Hi-Z	X	Standby
L	H	H	Hi-Z	X	Read Inhibit
X	L	X	-	X	Write Inhibit
L	L	H	Code	V <sub>H</sub>	Auto Select
L	L	H	$\overline{\text{DIN}}$	X	Data Polling

V<sub>H</sub> = 12.0 V ± .5 V  
 H = HIGH  
 L = LOW  
 X = Don't Care  
 $\overline{\text{Pulse}}$  = Pulse

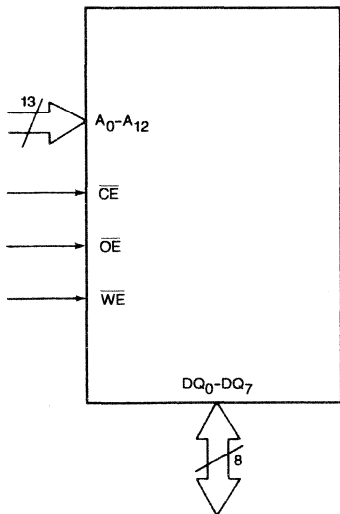
## PRODUCT SELECTOR GUIDE

Part Number	Am2864AE-205	Am2864AE-200	Am2864AE-255	Am2864AE-250	Am2864AE-305	Am2864AE-300	Am2864AE-355	Am2864AE-350
Maximum Access Time	200 ns		250 ns		300 ns		350 ns	
V <sub>CC</sub> Supply Tolerance	±5%	±10%	±5%	±10%	±5%	±10%	±5%	±10%

## CONNECTION DIAGRAMS Top View



## LOGIC SYMBOL



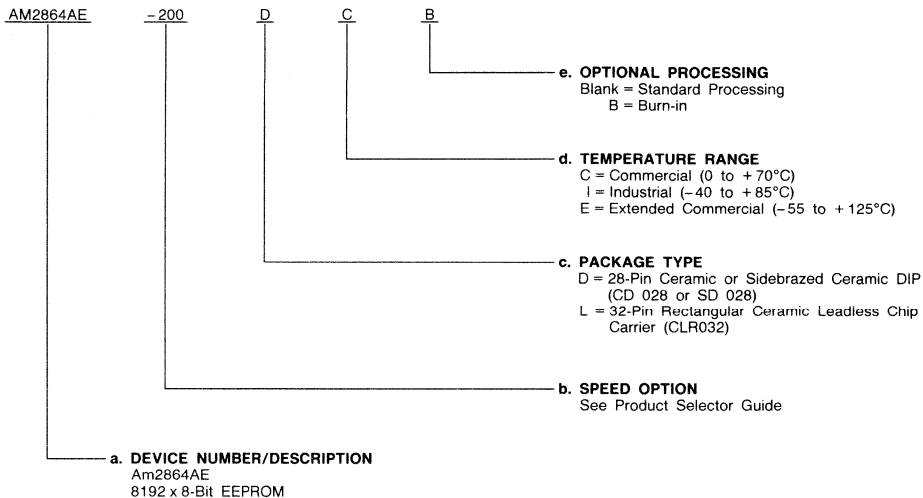
- A<sub>0</sub> - A<sub>12</sub> = Address Pins
- $\overline{CE}$  = Chip Enable
- DQ<sub>0</sub> - DQ<sub>7</sub> = Data Pins
- GND = Ground
- NC = No Connect
- $\overline{OE}$  = Output Enable
- V<sub>CC</sub> = Power Supply
- WE = Write Enable
- NC = No Connect

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option**
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM2864AE-205	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM2864AE-200	
AM2864AE-255	
AM2864AE-250	
AM2864AE-305	
AM2864AE-300	
AM2864AE-355	
AM2864AE-350	

#### Valid Combinations

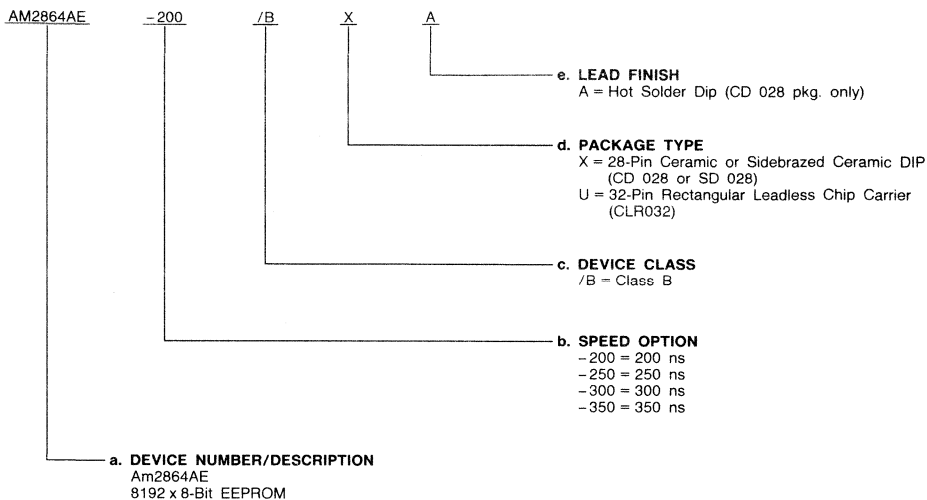
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM2864AE-200	/BXA, /BUA
AM2864AE-250	
AM2864AE-300	
AM2864AE-350	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

**3**

## FUNCTIONAL DESCRIPTION

### Read Mode

The Am2864AE has two control functions which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the outputs  $t_{OE}$  after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least  $t_{ACC-tOE}$ .

### Standby Mode

The Am2864AE has a standby mode which reduces the active power dissipation by 50%, from 735 mW to 368 mW ( $V_{CC} \pm 5\%$ ). The Am2864AE is placed in the standby mode by applying a TTL HIGH signal to the  $\overline{CE}$  input. When in the standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Data Protection

The Am2864AE incorporates several features that prevent unwanted write cycles during  $V_{CC}$  power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during  $V_{CC}$  power-up and power-down, a write cycle is locked out for  $V_{CC}$  less than 3.0 volts (typical 3.3 V). It is the users's responsibility to ensure that the control levels are logically correct when  $V_{CC}$  is above 3.0 volts.

There is a  $\overline{WE}$  lockout circuit that prevents  $\overline{WE}$  pulses of less than 20 ns duration from initiating a write cycle.

When the  $\overline{OE}$  control is in logic zero condition, a write cycle cannot be initiated.

### Write Cycle Control Pins

For system design simplification, the Am2864AE is designed in such a way that either  $\overline{CE}$  or  $\overline{WE}$  can be used to initiate a write cycle. During a system write cycle, the address is latched into the internal address latches upon the last falling edge of  $\overline{WE}$  or  $\overline{CE}$  providing that  $\overline{OE}$  is a logic "1". The first rising edge of  $\overline{WE}$  or  $\overline{CE}$  latches the data into the data latches. All setup and hold times are with respect to the  $\overline{WE}$  signal.

To simplify the following discussion, the  $\overline{WE}$  pin is used as the write cycle control pin throughout the rest of this functional description.

### Page Write Mode

The page write allows from 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. The page write mode consists of a load sequence followed by an automatic write sequence.

During the load portion, sequential  $\overline{WE}$  pulses load the byte address and the byte data into a 32-byte register. The bytes can be loaded into this register in any order. On each  $\overline{WE}$  pulse, the "Y" address is latched on the falling edge of the  $\overline{WE}$ , the data input is latched on the rising edge of  $\overline{WE}$ , and the page address ( $A_5-A_{12}$ ) is latched on the falling edge of the last  $\overline{WE}$ . Note that in order for a write to occur,  $\overline{CE}$  and  $\overline{WE}$  must be LOW and  $\overline{OE}$  must be HIGH. The load portion of the page write is complete when all the data (up to 32 bytes) is loaded into the register.

The automatic write portion starts  $t_{WW}$  after each transition of  $\overline{WE}$  from LOW-to-HIGH. If  $\overline{WE}$  transitions from HIGH-to-LOW before  $t_{WW}$  minimum (100  $\mu$ s), the timer is reset and the automatic write portion does not start. This is how the bytes

are loaded into the register. If  $\overline{WE}$  is held LOW, this  $t_{WW}$  timer never starts and the write cycle is held indefinitely.

When a write pulse is not given to the device within the  $t_{WW}$  minimum time (100  $\mu$ s) from the rising edge of the previous write pulse, the automatic write sequence is initiated. At completion of the automatic write sequence ( $t_{WB}$  maximum time has elapsed, or Data Polling indicates the write operation is complete), at least one of the control pins must deselect the device from accidental writes ( $\overline{OE}$  LOW,  $\overline{CE}$  HIGH, or  $\overline{WE}$  HIGH).

The automatic write sequence consists of an erase cycle, which erases any data that existed in each addressed cell; and a write cycle, which puts data back into the erased cells. Note that a page write will only write data to the locations being addressed and will not rewrite the entire page.

### Byte Mode Write

When  $\overline{WE}$  is toggled once, the Am2864AE operates in the byte mode. A single byte is loaded into the register, and after  $\overline{WE}$  goes HIGH and  $t_{WW}$  is satisfied, the automatic write cycle starts. It is in this mode that the Am2864AE is identical to the Am2864BE and Am9864.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EEPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional at 25°C  $\pm$ 5°C ambient temperature.

To activate this mode, programming equipment must force 11.5 V to 12.5 V on address line  $A_9$  of the Am2864AE. Two identifier bytes may then be sequenced from the device outputs by toggling address line  $A_0$  from  $V_{IL}$  to  $V_{IH}$ . All other address lines must be held at  $V_{IL}$  during auto select mode.

Byte 0 ( $A_0 = V_{IL}$ ) represents the manufacturer code and byte 1 ( $A_0 = V_{IH}$ ) the device identifier code. For the Am2864AE, these two identifier bytes are given in Table 1. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit. The auto select code for the Am2864AE is identical to the Am2864BE.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and be connected to the read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### Data Polling

Data Polling makes the Am2864AE highly flexible. It allows the designer the option of a software polling technique for end-of-write indication. Data Polling requires a simple software routine that performs a read operation when the chip is in the automatic write mode. The data that becomes valid during this Data Polling read is the inverse of all 8 bits last written to the outputs. The true data ( $DQ_0 - DQ_7$ ) will become valid when the automatic write has been completed. Note that all 8 bits invert during Data Polling, thereby giving the user more flexibility during design and layout.

## Chip Clear Mode (Military only)

Another feature included on AMD's Am2864AE for military applications is a single-pulse chip erase. This optional mode allows the user to program all bits to a logic ONE with a single 10-ms write. Additional information is available from AMD regarding this test mode — consult the local AMD sales office.

## Endurance

Since endurance testing is a destructive test, it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide, the oxide becomes conductive and reliable storage of charge on the floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant-mortality failures to be screened out. For the next 20,000 to 30,000 write cycles the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere

above this region, typically well above the guarantee of  $10^4$  total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD test screens will write a minimum of 10,000 times and retain data for a period of ten years at every byte location with a maximum failure rate of 5%. In other words, 5% (maximum) of a sample of devices will fail to write or to retain information after write if they are written 10,000 times. Those devices that fail will typically have a single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability failure mechanisms are measured.

For more detailed information on how this data was obtained please refer to the reliability section within this Handbook.

## APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1  $\mu\text{F}$  ceramic capacitor (high frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7  $\mu\text{F}$  bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## PROGRAMMING

TABLE 1. IDENTIFIER BYTES (Notes 1, 2 & 3)

Identifier	A <sub>0</sub>	DQ <sub>7</sub>	DQ <sub>6</sub>	DQ <sub>5</sub>	DQ <sub>4</sub>	DQ <sub>3</sub>	DQ <sub>2</sub>	DQ <sub>1</sub>	DQ <sub>0</sub>	Hex
Manufacturer Code	V <sub>IL</sub>	0	0	0	0	0	0	0	1	01
Device Code	V <sub>IH</sub>	1	0	0	0	1	0	1	0	8A

Legend: 1 = HIGH  
0 = LOW

- Notes: 1. A<sub>9</sub> = 12.0 V  $\pm$  0.5 V  
2. A<sub>1</sub> - A<sub>8</sub>, A<sub>10</sub> - A<sub>12</sub>,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$  = V<sub>IL</sub>  
3.  $\overline{\text{WE}}$  = V<sub>IH</sub>

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65 to +150°C  
 Ambient Temperature with Power Applied ..... -65 to +135°C  
 Voltage on All Inputs with Respect  
 to GND ..... +7.0 to -1.0 V  
 Voltage on A<sub>g</sub> with Respect  
 to GND ..... +13.5 to -0.6 V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices  
 Temperature (T<sub>C</sub>) ..... 0 to +70°C  
 Supply Voltage (V<sub>CC</sub> ±5%) ..... +4.75 to +5.25 V  
 (V<sub>CC</sub> ±10%) ..... +4.50 to +5.50 V

Industrial (I) Devices  
 Temperature (T<sub>C</sub>) ..... -40 to +85°C  
 Supply Voltage (V<sub>CC</sub> ±5%) ..... +4.75 to +5.25 V  
 (V<sub>CC</sub> ±10%) ..... +4.50 to +5.50 V

Extended Commercial (E) and Military (M) Devices  
 Temperature (T<sub>C</sub>) ..... -55 to +125°C  
 Supply Voltage (V<sub>CC</sub> ±10%) ..... +4.50 to +5.50 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Condition	Min.	Typ.	Max.	Unit
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = 0 and 5.5 V			10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 and 5.5 V			10	μA
I <sub>CC1</sub>	V <sub>CC</sub> Current (Standby)	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$			70	mA
I <sub>CC2</sub>	V <sub>CC</sub> Current (Active)	All Outputs Open			140	mA
V <sub>IL</sub>	Input LOW Voltage		-1.0		.8	V
V <sub>IH</sub>	Input HIGH Voltage		2.0		V <sub>CC</sub> +1	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA			.4	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -400 μA	2.4			V
C <sub>IN</sub>	Input Capacitance (Note 1, 2)	V <sub>IN</sub> = 0 V		4	8	pF
C <sub>OUT</sub>	Output Capacitance (Note 1, 2)	$\overline{OE} = \overline{CE} = V_{IH}, V_{OUT} = 0 V$		8	10	pF
V <sub>WI</sub>	Write Inhibit Voltage		3.0	3.3		V

- Notes: 1. This parameter is measured only for the initial qualification and after process or design changes which affect capacitance.  
 2. Freq. = 1 MHz @ 25°C.  
 3. Typical values are for nominal supply voltages.



**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Condition	Am2864AE-205, Am2864AE-200		Am2864AE-255, Am2864AE-250		Am2864AE-305, Am2864AE-300		Am2864AE-355, Am2864AE-350		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ</b>												
1	t <sub>ACC</sub>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		350	ns
2	t <sub>CE</sub>	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		350	ns
3	t <sub>OE</sub>	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		150		150		150		150	ns
4	t <sub>DF</sub> (Note 1)	Output Enable or Chip Enable HIGH to Output Float		10	60	10	60	10	80	10	80	ns
5	t <sub>OH</sub> (Note 1)	Output Hold from Address Change	$\overline{CE} = \overline{OE} = V_{IL}$	20		20		20		20		ns
6	t <sub>RC</sub>	Read Cycle Time	$\overline{CE} = \overline{OE} = V_{IL}$	200		250		300		350		ns
7	t <sub>DA</sub> (Note 1)	Output Enable or Chip Enable LOW to Output Active		10		10		10		10		ns
<b>WRITE</b>												
8	t <sub>AS</sub>	Address to Write Setup Time		10		10		10		20		ns
9	t <sub>CS</sub>	$\overline{CE}$ to Write Setup Time		0		0		0		0		ns
10	t <sub>WP</sub>	$\overline{WE}$ or $\overline{CE}$ Write Pulse Width		150		150		150		200		ns
11	t <sub>AH</sub>	Address Hold Time		200		200		200		200		ns
12	t <sub>DS</sub>	Data Setup Time		100		100		100		120		ns
13	t <sub>DH</sub>	Data Hold Time		20		20		20		30		ns
14	t <sub>CH</sub>	$\overline{CE}$ Hold Time		0		0		0		0		ns
15	t <sub>OES</sub>	$\overline{OE}$ Setup Time		10		10		10		10		ns
16	t <sub>OEH</sub>	$\overline{OE}$ Hold Time		10		10		10		10		ns
17	t <sub>WC</sub>	Byte Load Cycle Time		3		3		3		3		μs
18	t <sub>WW</sub>	Page Write Window (Note 3)		20		20		20		20		μs
19	t <sub>WH</sub>	$\overline{WE}$ or $\overline{CE}$ Write Pulse HIGH Time		50		50		50		100		ns
20	t <sub>WB</sub>	Byte or Page Write Cycle Time (Note 4)			10		10		10		10	ms
21	t <sub>WPH</sub>	Write Deselect Hold Time (Note 5)		50		50		50		50		ns
22	(Notes 1 & 2)	Number of Writes per Byte		10		10		10		10		x1000

- Notes: 1. This parameter is measured only at the initial qualification and after process or design changes which affect the parameter.  
2. See Reliability Section within this HANDBOOK.  
3. A timer of t<sub>WW</sub> duration starts at every LOW-to-HIGH transition of  $\overline{WE}$ . If it is allowed to time out, a page write will start. A transition of  $\overline{WE}$  from HIGH-to-LOW will stop the timer.  
4. When t<sub>WB</sub> maximum time has elapsed or Data Polling indicates the write operation is complete, at least one of the control pins must deselect the device ( $\overline{WE}$  HIGH,  $\overline{CE}$  HIGH, or  $\overline{OE}$  LOW). Once the write cycle is complete, the device is available for the next operation.  
5. This is the time from deselecting the device ( $\overline{WE}$  or  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IL}$ ) to the other control pins becoming don't cares.

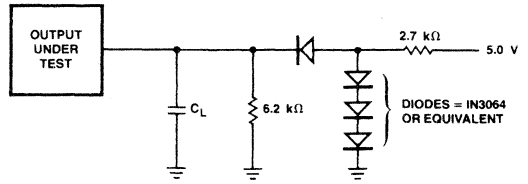
## SWITCHING TEST CONDITIONS

Output load: 1 TTL gate and  $C_L = 100$  pF  
 Input pulse levels: 0.45 V to 2.4 V

### Timing Measurement Reference Levels

Input: 0.8 V and 2.0 V  
 Output: 0.8 V and 2.0 V

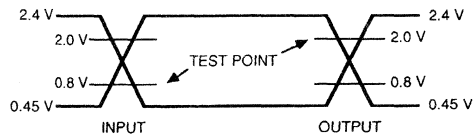
### SWITCHING TEST CIRCUIT



TC002491

$C_L = 100$  pF, including jig capacitance.

## SWITCHING TEST WAVEFORM



WF025110

AC Testing: Inputs are driven at 2.4 V for logic "1" and 0.45 V for logic "0". Timing measurements are made at 0.8 V and 2.0 V. Input pulse rise and fall times are 10 ns.

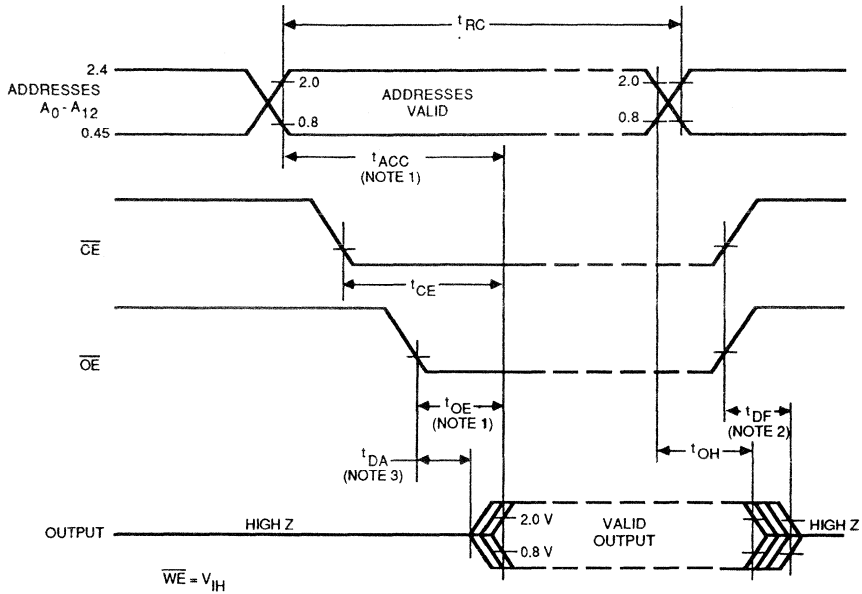
## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

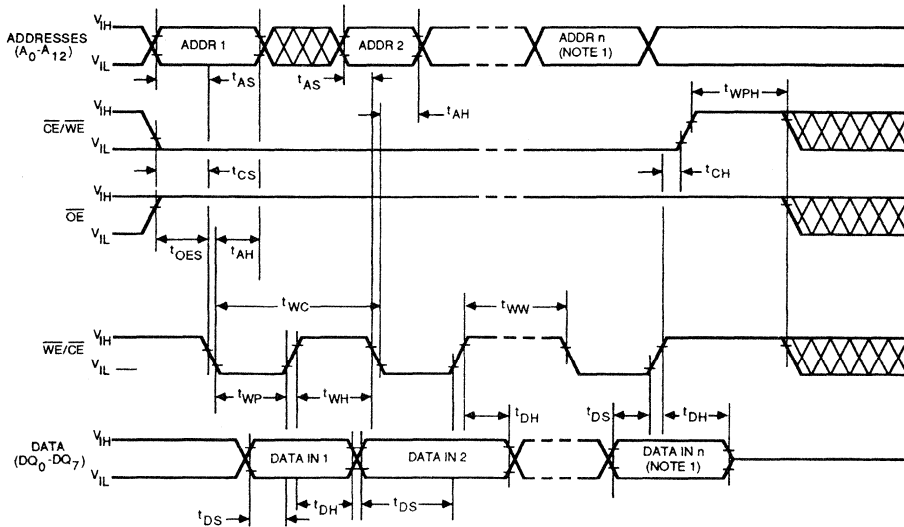
SWITCHING WAVEFORMS (Cont'd.)



WF025120

Read

- Notes: 1.  $\overline{OE}$  may be delayed up to  $t_{ACC}-t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .  
 2.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.  
 3.  $t_{DA}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs last.

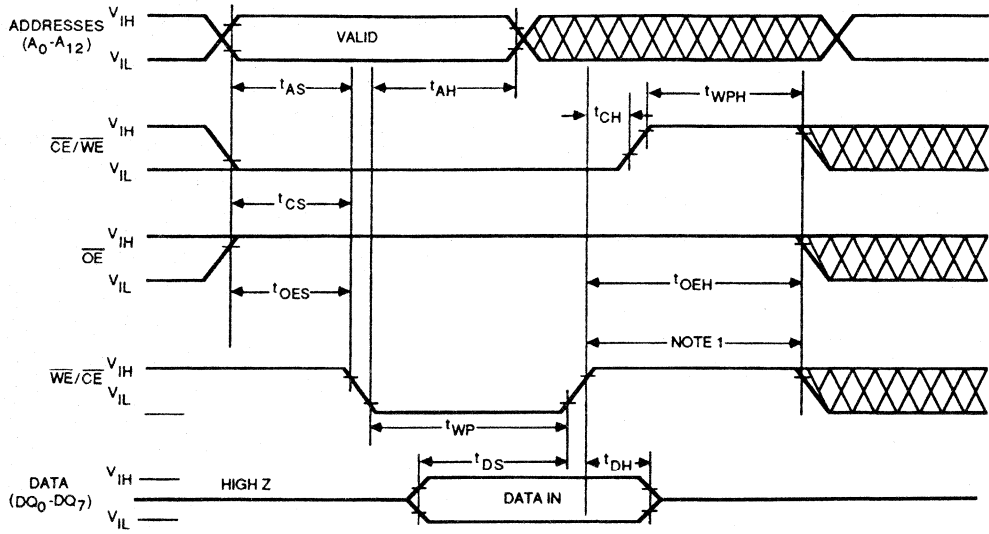


WF025132

Page Write

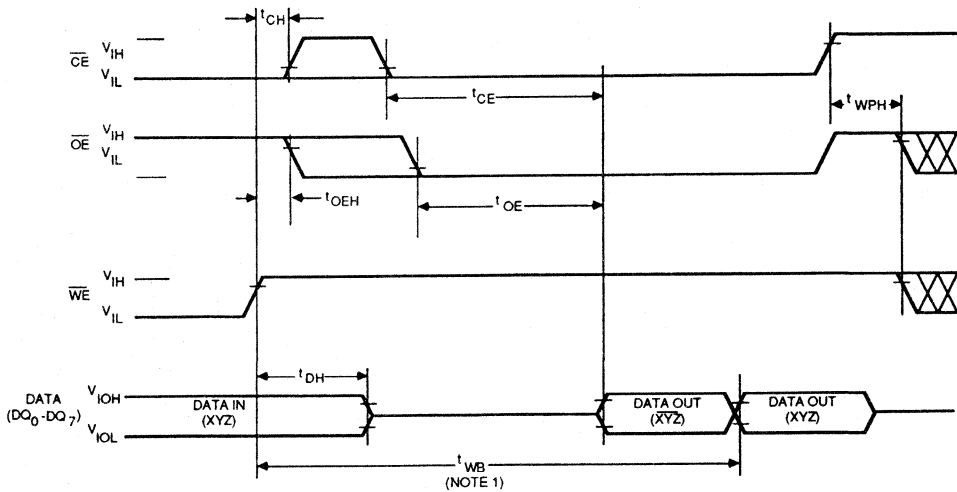
Notes: 1.  $n \leq 32$ .

## SWITCHING WAVEFORMS (Cont'd.)



### Byte Write

Notes: 1. This time period =  $t_{CH} + t_{RISE} + t_{WPH}$ .



### Data Polling

Notes: 1. When the write cycle is completed (data out TRUE), the user must meet one of the following conditions to prevent an accidental write:  $\overline{OE}$  LOW,  $\overline{CE}$  HIGH, or  $\overline{WE}$  HIGH.

# Am2864BE

8192 x 8-Bit Electrically Erasable PROM



## DISTINCTIVE CHARACTERISTICS

- 5-V only operation
- Military temperature range available
- Self-timed Write Cycle with on-chip latches
- Ready/Busy pin and Data Polling for end-of-write indication
- Allows  $\overline{WE}$  and  $\overline{OE}$  controlled Writes
- Data protection features to prevent writes from occurring during  $V_{CC}$  power-up/down
- 32-byte page write mode
- Minimum endurance of 10,000 write cycles per byte with a 10-year retention. For detailed information, see the reliability section within this Handbook.

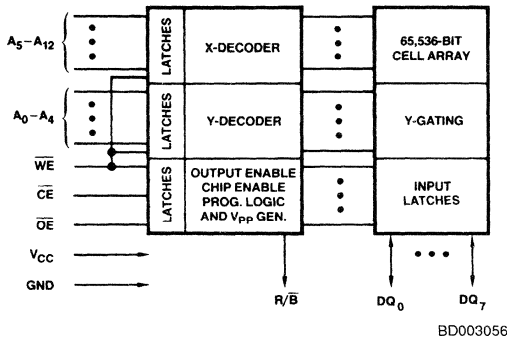
## GENERAL DESCRIPTION

The Am2864BE is a 65,536-bit Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 8192 words by 8 bits per word. It operates from a single 5-volt supply and has a fully self-timed write cycle with address, data, and control lines latched during the write operation. The 32-byte page write mode allows programming in as little as 2.6 seconds. The Am2864BE is fabricated on AMD's highly manufacturable N-Channel Silicon gate process, and uses AMD's proprietary EEPROM

technology to achieve electrically alterable nonvolatile storage. This technology employs the industry-accepted Fowler-Nordheim tunneling across a thin oxide.

The Am2864BE provides the on-chip logic necessary to interface with most microprocessors. The latched inputs and self-timed write cycle free the microprocessor to perform other tasks during a write. A transparent automatic erase before write enhances system performance.

## BLOCK DIAGRAM



## MODE SELECT TABLE

Inputs			Outputs			
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	R/B	I/O	$A_9$	Mode
L	L	H	Hi Z	Data Out	X	Read
L	H	$\square$	$\square$	Data In	X	Write
$\square$	H	L	$\square$	Data In	X	Write
H	X	X	Hi Z	Hi Z	X	Standby
L	H	H	Hi Z	Hi Z	X	Read Inhibit
X	L	X	-	-	X	Write Inhibit
L	L	H	Hi Z	Code	$V_H$	Auto Select
L	L	H	L	$\overline{D}_{in}$	X	Data Polling

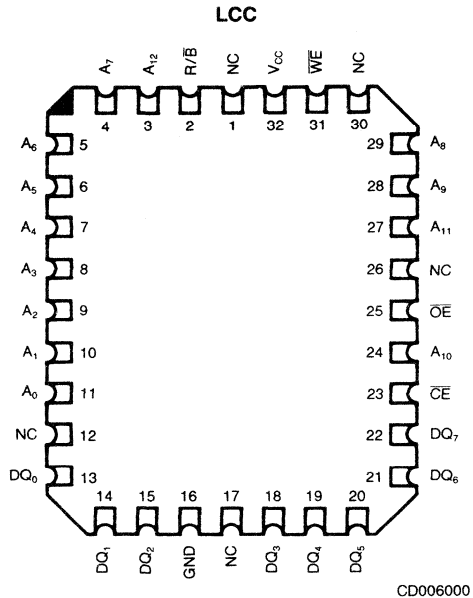
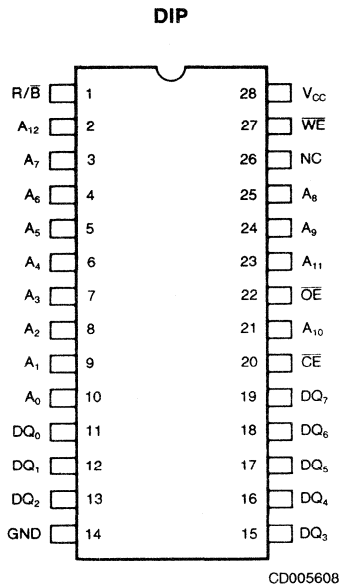
$V_H = 12.0 \text{ V} \pm .5 \text{ V}$   
 H = HIGH  
 L = LOW  
 X = Don't Care  
 $\square$  = Pulse

## PRODUCT SELECTOR GUIDE

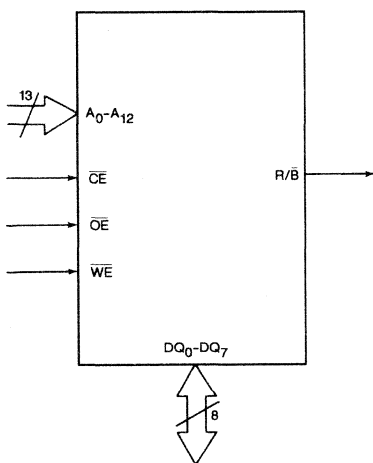
Part Number	Am2864BE-205	Am2864BE-200	Am2864BE-255	Am2864BE-250	Am2864BE-305	Am2864BE-300	Am2864BE-355	Am2864BE-350
Maximum Access Time	200 ns		250 ns		300 ns		350 ns	
$V_{CC}$ Supply Tolerance	$\pm 5\%$	$\pm 10\%$	$\pm 5\%$	$\pm 10\%$	$\pm 5\%$	$\pm 10\%$	$\pm 5\%$	$\pm 10\%$

## CONNECTION DIAGRAMS

### Top View



### LOGIC SYMBOL



- A<sub>0</sub> - A<sub>12</sub> = Address Pins
- $\overline{CE}$  = Chip Enable
- DQ<sub>0</sub> - DQ<sub>7</sub> = Data Pins
- GND = Ground
- $\overline{OE}$  = Output Enable
- R/ $\overline{B}$  = Ready/Busy
- V<sub>CC</sub> = Power Supply
- $\overline{WE}$  = Write Enable
- NC = No Connect

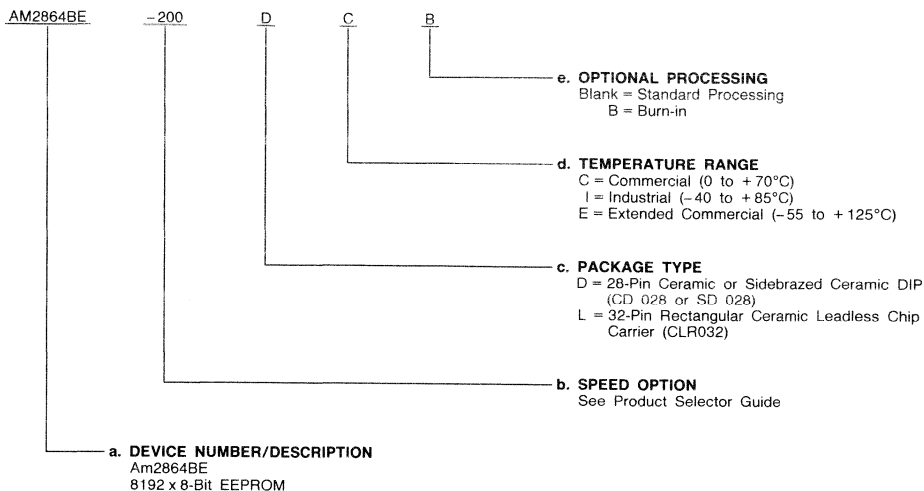
LS002271

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM2864BE-205	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM2864BE-200	
AM2864BE-255	
AM2864BE-250	
AM2864BE-305	
AM2864BE-300	
AM2864BE-355	
AM2864BE-350	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

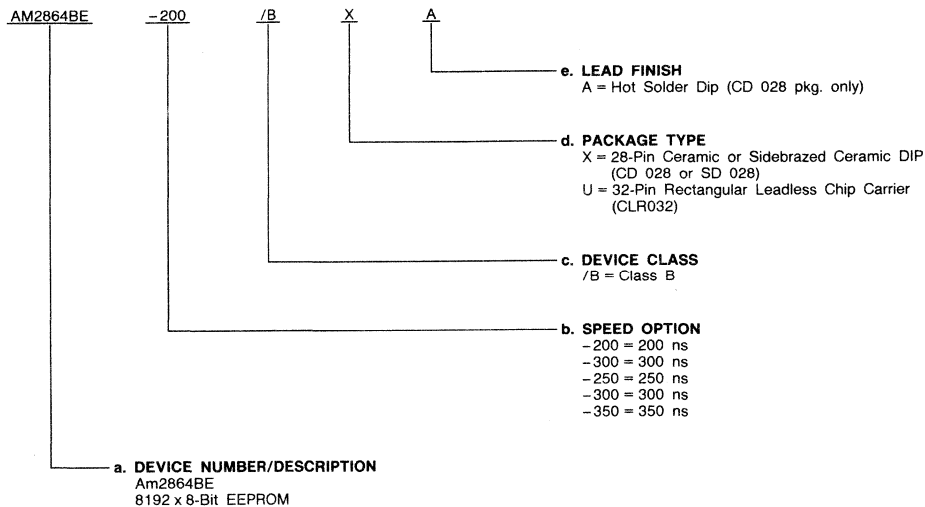


## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option**
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM2864BE-200	/BXA, /BUA
AM2864BE-250	
AM2864BE-300	
AM2864BE-350	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.



## FUNCTIONAL DESCRIPTION

### Read Mode

The Am2864BE has two control functions which must both be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the outputs  $t_{OE}$  after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least  $t_{ACC}-t_{OE}$ .

### Standby Mode

The Am2864BE has a standby mode which reduces the active power dissipation by 50%, from 735 mW to 368 mW ( $V_{CC} \pm 5\%$ ). The Am2864BE is placed in the standby mode by applying a TTL HIGH signal to the  $\overline{CE}$  input. When in the standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Data Protection

The Am2864BE incorporates several features that prevent unwanted write cycles during  $V_{CC}$  power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during  $V_{CC}$  power-up and power-down, a write cycle is locked out for  $V_{CC}$  less than 3.0 volts (typical 3.3 V). It is the users' responsibility to ensure that the control levels are logically correct when  $V_{CC}$  is above 3.0 volts.

There is a  $\overline{WE}$  lockout circuit that prevents  $\overline{WE}$  pulses of less than 20 ns duration from initiating a write cycle.

When the  $\overline{OE}$  control is in logic zero condition, a write cycle cannot be initiated.

### Write Cycle Control Pins

For system design simplification, the Am2864BE is designed in such a way that either  $\overline{CE}$  or  $\overline{WE}$  can be used to initiate a write cycle. During a system write cycle, the address is latched into the internal address latches upon the last falling edge of  $\overline{WE}$  or  $\overline{CE}$  providing that  $\overline{OE}$  is a logic '1'. The first rising edge of  $\overline{WE}$  or  $\overline{CE}$  latches the data into the data latches. All setup and hold times are with respect to the  $\overline{WE}$  signal.

To simplify the following discussion, the  $\overline{WE}$  pin is used as the write cycle control pin throughout the rest of this functional description.

### Page Write Mode

The page write allows from 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. The page write mode consists of a load sequence followed by an automatic write sequence.

During the load portion, sequential  $\overline{WE}$  pulses load the byte address and the byte data into a 32-byte register. The bytes can be loaded into this register in any order. On each  $\overline{WE}$  pulse, the "Y" address is latched on the falling edge of  $\overline{WE}$ , the data input is latched on the rising edge of  $\overline{WE}$ , and the page address ( $A_5-A_{12}$ ) is latched on the falling edge of the last  $\overline{WE}$ . Note that in order for a write to occur,  $\overline{CE}$  and  $\overline{WE}$  must be LOW and  $\overline{OE}$  must be HIGH. The load portion of the page write is complete when all the data (up to 32 bytes) is loaded into the register.

The automatic write portion starts  $t_{WW}$  after each transition of  $\overline{WE}$  from LOW-to-HIGH. If  $\overline{WE}$  transitions from HIGH-to-LOW before  $t_{WW}$  minimum (100  $\mu$ s), the timer is reset and the automatic write portion does not start. This is how the bytes are loaded into the register. If  $\overline{WE}$  is held LOW, this  $t_{WW}$  timer never starts and the write cycle is held indefinitely.

When a write pulse is not given to the device within the  $t_{WW}$  minimum time (100  $\mu$ s) from the rising edge of the previous write pulse, the automatic write sequence is initiated. At completion of the automatic write sequence ( $t_{WB}$  maximum time has elapsed, or Data Polling or R/ $\overline{B}$  indicates the write operation is complete), at least one of the control pins must deselect the device from accidental writes ( $\overline{OE}$  LOW,  $\overline{CE}$  HIGH, or  $\overline{WE}$  HIGH).

The automatic write sequence consists of an erase cycle, which erases any data that existed in each addressed cell; and a write cycle, which puts data back into the erased cells. Note that a page write will only write data to the locations being addressed and will not rewrite the entire page. The Ready/Busy pin (R/ $\overline{B}$ ) goes to a logic LOW level during the automatic write sequence. This could signal a microprocessor host that the system bus is free for other activity. When R/ $\overline{B}$  transitions to a HIGH state, the Am2864BE has completed writing and is ready to accept another cycle.

### Byte Mode Write

When  $\overline{WE}$  is toggled once, the Am2864BE operates in the byte mode. A single byte is loaded into the register, and after  $\overline{WE}$  goes HIGH, and  $t_{WW}$  is satisfied, the automatic write cycle starts. It is in this mode that the Am2864BE is similar to the Am9864.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EEPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional at 25°C  $\pm$  5°C ambient temperature.

To activate this mode, programming equipment must force 11.5 V to 12.5 V on address line  $A_9$  of the Am2864BE. Two identifier bytes may then be sequenced from the device outputs by toggling address line  $A_0$  from  $V_{IL}$  to  $V_{IH}$ . All other address lines must be held at  $V_{IL}$  during auto select mode.

Byte 0 ( $A_0 = V_{IL}$ ) represents the manufacturer code and byte 1 ( $A_0 = V_{IH}$ ) the device identifier code. For the Am2864BE, these two identifier bytes are given in Table 1. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (0<sub>7</sub>) defined as the parity bit.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and be connected to the read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.



## Ready/Busy Pin

The Ready/Busy (R/B) pin is an open-drain output which allows two or more R/B signals to be OR-tied together. The value of the pullup resistor required is as follows:

$$R_{pu} = \frac{4.6 \text{ volts}}{2.1 \text{ mA} - I_{IL}}$$

$I_{IL}$  = total  $V_{IL}$  input current of devices connected to R/B

A typical pullup resistor value for R/B is 3 k $\Omega$ , assuming  $I_{IL}$  is less than 0.5 mA.

## Data Polling

Data Polling makes the Am2864BE highly flexible. It allows the designer the option of a software polling technique as well as the hardware interrupt Ready/Busy technique for end-of-write indication. Data Polling requires a simple software routine that performs a read operation when the chip is in the automatic write mode. The data that becomes valid during this Data Polling read is the inverse of all 8 bits last written to the outputs. The true data (DQ<sub>0</sub> – DQ<sub>7</sub>) will become valid when the automatic write has been completed. Note that all 8 bits invert during Data Polling, thereby giving the user more flexibility during design and layout.

## Chip Clear Mode (Military only)

Another feature included on AMD's Am2864BE for military applications is a single-pulse chip erase. This optional mode allows the user to program all bits to a logic ONE with a single 10-ms write. Additional information is available from AMD regarding this test mode — consult the local AMD sales office.

## Endurance

Since endurance testing is a destructive test, it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide, the oxide becomes conductive and reliable storage of charge on the

floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant-mortality failures to be screened out. For the next 20,000 to 30,000 write cycles the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere above this region, typically well above the guarantee of 10<sup>4</sup> total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD test screens will write a minimum of 10,000 times and retain data for a period of ten years at every byte location with a maximum failure rate of 5%. In other words, 5% (maximum) of a sample of devices will fail to write or to retain information after write if they are written 10,000 times. Those devices that fail will typically have a single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability failure mechanisms are measured.

For more detailed information on how this data was obtained, please refer to the reliability section within this Handbook.

## APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1- $\mu$ F ceramic capacitor (high-frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7- $\mu$ F bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## PROGRAMMING

TABLE 1. IDENTIFIER BYTES (Notes 1, 2 & 3)

Identifier	A <sub>0</sub>	DQ <sub>7</sub>	DQ <sub>6</sub>	DQ <sub>5</sub>	DQ <sub>4</sub>	DQ <sub>3</sub>	DQ <sub>2</sub>	DQ <sub>1</sub>	DQ <sub>0</sub>	Hex
Manufacturer Code	$V_{IL}$	0	0	0	0	0	0	0	1	01
Device Code	$V_{IH}$	1	0	0	0	1	0	1	0	8A

Legend: 1 = HIGH

0 = LOW

Notes: 1.  $A_g = 12.0 \text{ V} \pm 0.5 \text{ V}$

2.  $A_1 - A_8, A_{10} - A_{12}, \overline{CE}, \overline{OE} = V_{IL}$

3.  $\overline{WE} = V_{IH}$

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65 to +150°C  
 Ambient Temperature with Power Applied . -65 to +135°C  
 Voltage on All Inputs with Respect  
 to GND .....+6.50 to -0.6 V  
 Voltage on A<sub>g</sub> with Respect  
 to GND .....+13.5 to -0.6 V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices  
 Temperature (T<sub>C</sub>)..... 0 to +70°C  
 Supply Voltage (V<sub>CC</sub> ±5%) .....+4.75 to +5.25 V  
 (V<sub>CC</sub> ±10%) .....+4.50 to +5.50 V  
 Industrial (I) Devices  
 Temperature (T<sub>C</sub>).....-40 to +85°C  
 Supply Voltage (V<sub>CC</sub> ±5%) .....+4.75 to +5.25 V  
 (V<sub>CC</sub> ±10%) .....+4.50 to +5.50 V  
 Extended Commercial (E) and Military (M) Devices  
 Temperature (T<sub>C</sub>).....-55 to +125°C  
 Supply Voltage (V<sub>CC</sub> ±10%) .....+4.50 to +5.50 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Condition	Min.	Typ.	Max.	Unit
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = 0 and 5.5 V			10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 and 5.5 V			10	μA
I <sub>CC1</sub>	V <sub>CC</sub> Current (Standby)	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$			70	mA
I <sub>CC2</sub>	V <sub>CC</sub> Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$			140	mA
V <sub>IL</sub>	Input LOW Voltage		-1.0		.8	V
V <sub>IH</sub>	Input HIGH Voltage		2.0		V <sub>CC</sub> +1	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA			.45	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -400 μA	2.4			V
V <sub>RB</sub>	R/ $\overline{B}$ Output LOW	I <sub>RB</sub> = 2.1 mA			.45	V
C <sub>IN</sub>	Input Capacitance (Note 1, 2)	V <sub>IN</sub> = 0 V		4	8	pF
C <sub>OUT</sub>	Output Capacitance (Note 1, 2)	$\overline{OE} = \overline{CE} = V_{IH}, V_{OUT} = 0 V$		8	10	pF
V <sub>WI</sub>	Write Inhibit Voltage		3.0	3.3		V

Notes: 1. This parameter is measured only for the initial qualification and after process or design changes which affect capacitance.  
 2. Freq. = 1 MHz @ 25°C.  
 3. Typical values are for nominal supply voltages.



**SWITCHING CHARACTERISTICS** over operating ranges (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Condition	Am2864BE-205, Am2864BE-200		Am2864BE-255, Am2864BE-250		Am2864BE-305, Am2864BE-300		Am2864BE355, Am2864BE-350		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ</b>												
1	t <sub>ACC</sub>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		350	ns
2	t <sub>CE</sub>	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		350	ns
3	t <sub>OE</sub>	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		90		90		110		120	ns
4	t <sub>DF</sub> (Note 1)	Output Enable or Chip Enable HIGH to Output Float		10	60	10	60	10	70	10	80	ns
5	t <sub>OH</sub> (Note 1)	Output Hold from Address Change	$\overline{CE} = \overline{OE} = V_{IL}$	20		20		20		20		ns
6	t <sub>RC</sub>	Read Cycle Time		200		250		300		350		ns
7	t <sub>DA</sub> (Note 1)	Output Enable or Chip Enable LOW to Output Active		10		10		10		10		ns
<b>WRITE</b>												
8	t <sub>AS</sub>	Address to Write Setup Time		10		10		10		20		ns
9	t <sub>CS</sub>	$\overline{CE}$ to Write Setup Time		0		0		0		0		ns
10	t <sub>WP</sub>	$\overline{WE}$ or $\overline{CE}$ Write Pulse Width		150		150		150		200		ns
11	t <sub>AH</sub>	Address Hold Time		80		80		80		100		ns
12	t <sub>DS</sub>	Data Setup Time		100		100		100		120		ns
13	t <sub>DH</sub>	Data Hold Time		20		20		20		30		ns
14	t <sub>CH</sub>	$\overline{CE}$ Hold Time		0		0		0		0		ns
15	t <sub>OES</sub>	$\overline{OE}$ Setup Time		10		10		10		10		ns
16	t <sub>OEH</sub>	$\overline{OE}$ Hold Time		10		10		10		10		ns
17	t <sub>DB</sub>	Time to Device Busy			100		100		100		100	ns
18	t <sub>WC</sub>	Byte Load Cycle Time		1		1		1		1		μs
19	t <sub>WW</sub>	Page Write Window (Note 3)		100		100		100		100		μs
20	t <sub>WH</sub>	$\overline{WE}$ or $\overline{CE}$ Write Pulse HIGH Time		50		50		50		100		ns
21	t <sub>WB</sub>	Byte or Page Write Cycle Time (Note 4)			10		10		10		10	ms
22	t <sub>WPH</sub>	Write Deselect Hold Time (Note 5)		10		10		10		10		ns
23	(Notes 1 & 2)	Number of Writes per Byte		10		10		10		10		x1000

- Notes: 1. This parameter is measured only at the initial qualification and after process or design changes which affect the parameter.  
2. See Reliability Section within this HANDBOOK.  
3. A timer of t<sub>WW</sub> duration starts at every LOW-to-HIGH transition of  $\overline{WE}$ . If it is allowed to time out, a page write will start. A transition of  $\overline{WE}$  from HIGH-to-LOW will stop the timer.  
4. When t<sub>WB</sub> maximum time has elapsed or Data Polling (or R/ $\overline{B}$ ) indicates the write operation is complete, at least one of the control pins must deselect the device ( $\overline{WE}$  or  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IL}$ ). Once the write cycle is complete, the device is available for the next operation.  
5. This is the time from deselecting the device ( $\overline{WE}$  or  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IL}$ ) to the other control pins being a don't care.

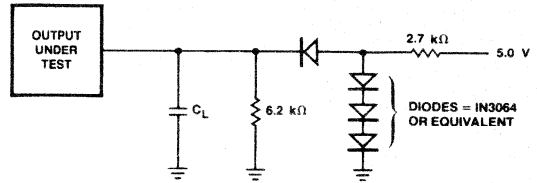
## SWITCHING TEST CIRCUIT

### Switching Test Conditions

Output load: 1 TTL gate and  $C_L = 100$  pF  
 Input pulse levels: 0.45 V to 2.4 V

### Timing Measurement Reference Levels

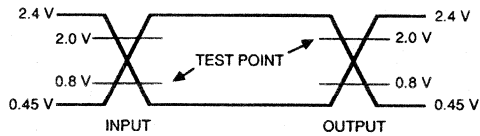
Input: 0.8 V and 2.0 V  
 Output: 0.8 V and 2.0 V



TC002491

$C_L = 100$  pF, including jig capacitance.

## SWITCHING TEST WAVEFORM



WF025160

AC Testing: Inputs are driven at 2.4 V for logic "1" and 0.45 V for logic "0". Timing measurements are made at 0.8 V and 2.0 V. Input pulse rise and fall times are 10 ns.

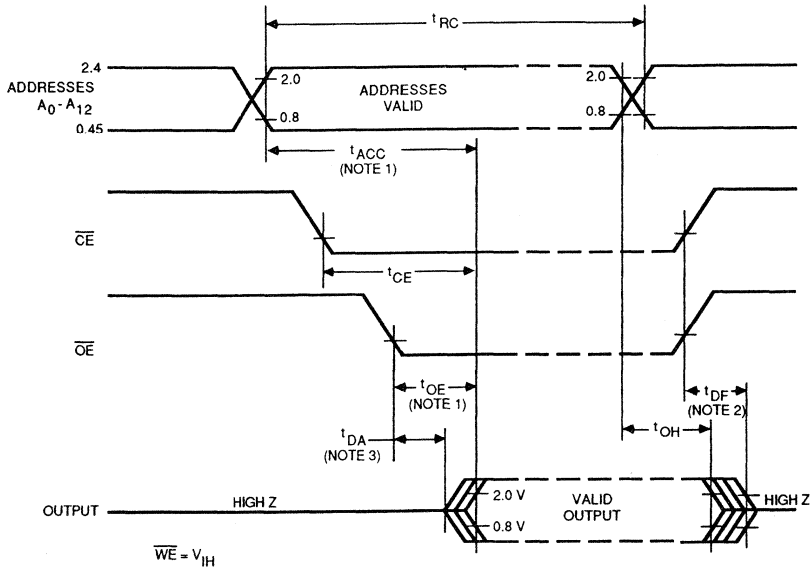
## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

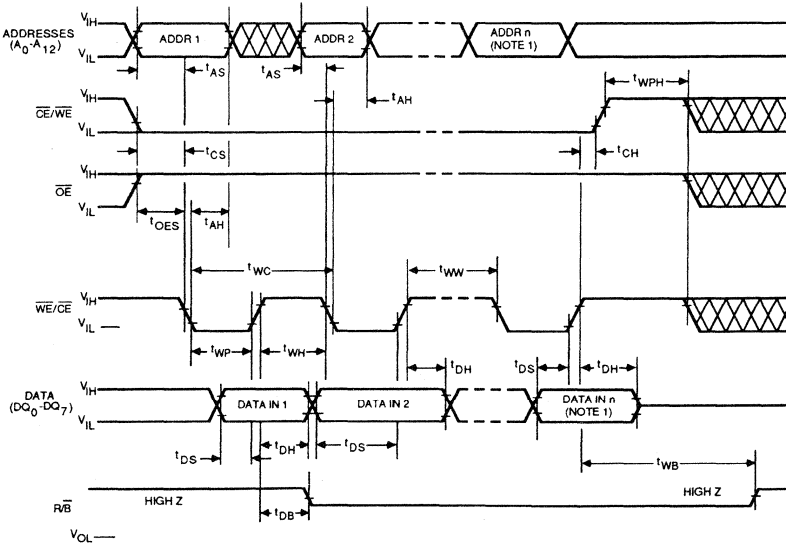
## SWITCHING WAVEFORMS (Cont'd.)



WF025180

### Read

- Notes: 1.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .  
 2.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.  
 3.  $t_{DA}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs last.

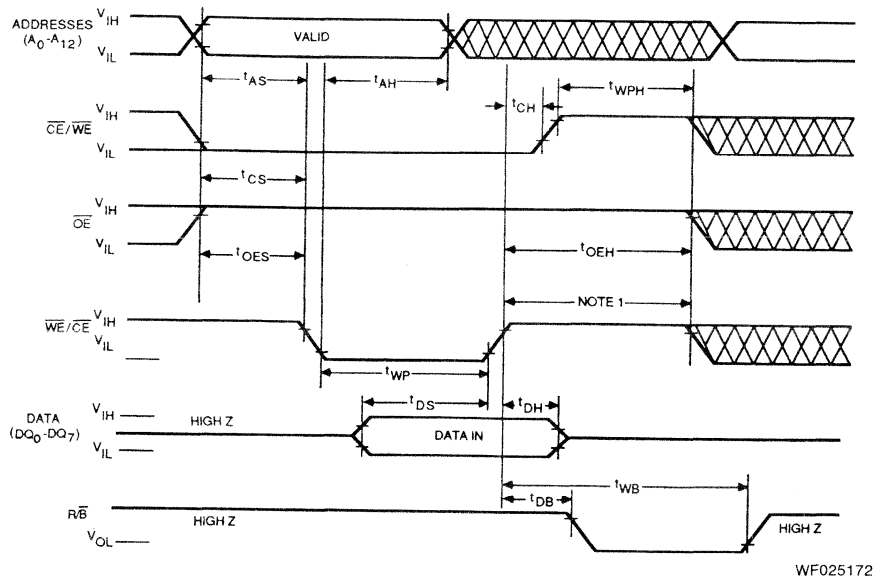


WF025202

### Page Write

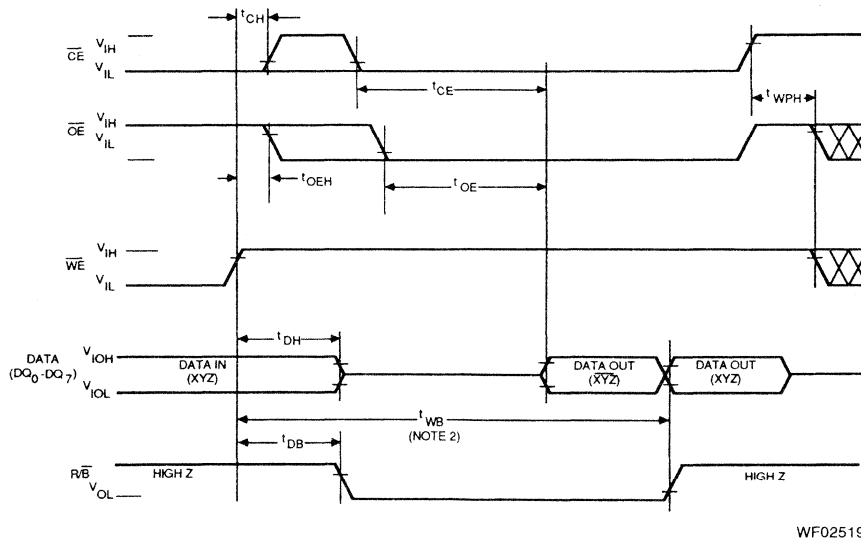
- Notes: 1.  $n \leq 32$ .

## SWITCHING WAVEFORMS (Cont'd.)



### Byte Write

Notes: 1. This time period =  $t_{CH} + t_{RISE} + t_{WPH}$ .



### Data Polling

Notes: 1. This is shown for single byte write. In page write,  $R/\bar{B}$  goes LOW on first LOW-to-HIGH transition of  $\bar{WE}$ .

2. When the Write cycle is completed ( $R/\bar{B}$  is HIGH or data out TRUE), the user must meet one of the following conditions to prevent an accidental write:  $\bar{OE}$  LOW,  $\bar{CE}$  HIGH, or  $\bar{WE}$  HIGH.



# EEPROM Highlights

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## WHY USE EEPROMS?

A wide spectrum of memory devices have been developed to fill particular needs. Read-Only Memories (ROMs) have high density and fast data access. The biggest disadvantage is the production volume required with an unalterable data pattern. Random-Access Memories (RAMs) may be easy to use and very fast to read and write, but cannot hold their data without power. Programmable Read-Only Memories (PROMs) can hold their data without power, but can only be programmed once. UV-Erasable PROMs (EPROMs) are reprogrammable, but must be removed from the system to do so. Electrically Erasable PROMs (EEPROMs) combine the advantages of the RAM and EPROM to offer a wide range of features which include:

- 5-V only operation
- In-system reprogrammability with RAM-compatible control signals
- Page write capability
- 10-year data retention
- Full military temperature range

The limitations of EEPROMs are the limited number of Write Cycles—10K cycles (endurance) and the write time.

## EEPROM APPLICATIONS

EEPROMs are used in many varied applications where a combination of non-volatility and occasional reprogramming are required. Some of these "read-mostly" applications are listed here.

- **Computers and Peripherals**
  - Computer configuration
  - Tape and disk drives
  - CRT terminals
  - Printers
- **Communications**
  - Data encryption
  - Radio telephones
  - Telephone configuration
  - Office equipment configuration

- **Consumer**
  - Appliance features
  - Smart credit cards
  - Automatic tellers
  - Games
- **Industrial**
  - Process and numerical control
  - Robotics
  - Transducers
  - Engine control
  - Data logging
- **Instrumentation**
  - Medical equipment
  - Test equipment
  - Portable equipment
- **Military**
  - Flight recorders
  - Terrain mapping
  - Portable equipment
  - Bomb fuses

## Am2864AE and Am2864BE USER BENEFITS

### Requires No Additional Glue Logic (Operates on 5 V)

These are AMD's most advanced 64K EEPROMs. Originally, EEPROMs required 21 V for programming as well as external timing and latch circuits. The Am2864AE and Am2864BE incorporate:

- a high-voltage generator
- address and data latches
- filtering and timing circuits

This results in an easier and less expensive design requiring less PC board space.



## EEPROM Highlights

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### False Write Protection

When a system is powering up or down, the voltage levels on the pins fluctuate. This may result in the initiation of an unwanted Write Cycle. This situation is minimized by locking out the Write Cycle when  $V_{CC}$  is below 3.0 V. The Output-Enable and Write-Enable pins must also be in the correct and opposite states to initiate a Write Cycle.

### Faster Write Cycle—Page Write Mode

One to 32 bytes may be written into the page-mode buffer in a single Write Cycle. Once the write window closes, the Am2864AE/BE gets off the system bus and writes to the desired bytes in the page window within a 10 ms (Max.) period. This mode will write data only to the locations being addressed, and will not affect the endurance of the unselected bytes. With page mode, an entire 8K-byte memory array may be written in 2.6 seconds.

### Data Polling

This is a software technique for detecting the end of the non-volatile Write Cycle. In multi-chip systems, new Write Cycles can begin as soon as the device examined has completed the previous non-volatile Write Cycle.

### Ready/Busy Pin

Pin 1 on the Am2864BE DIP (pin 2 on the LCC version) provides a hardware interrupt to the CPU to indicate when the Write Cycle is complete. On the Am2864AE, pin 1 is a No Connect.



# EEPROM Process Information

## PROCESS AND TECHNOLOGY

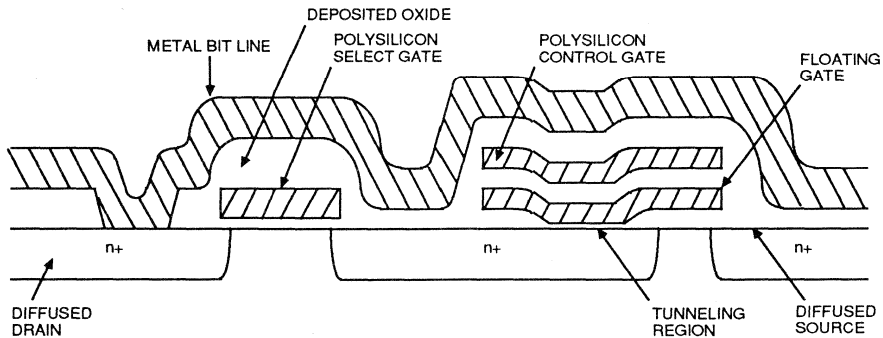
AMD's EEPROM technology is based on the highly successful N-channel EPROM process that has had years of manufacturing history at AMD. To achieve the goal of electrical erasability, an additional masking step was added so that a small region of thin, high-quality tunnel oxide could be located between the memory cell drain and the floating polysilicon gate. An idealized cross-section of the memory cell is shown in Figure 1. A top view of the cell is shown in Figure 2.

Compared to an EPROM, an additional (enhancement) transistor has been added (word line select) to the cell, as depicted in Figure 2-3. This transistor has two functions: to prevent leakage during read in non-selected discharged cells since they have a negative threshold, and to protect non-selected EEPROM cells on the same word line during charge. The tunnel-oxidation process was developed to result in a reproducible ultra-high quality, thermally grown oxide (of approximately 100 Å thickness) capable of withstanding the high fields associated with Fowler-Nordheim tunneling through a thin oxide. This approach to EEPROM memory permits a high degree of synergy between the EEPROM and EPROM technologies. The technology advances made for

EPROMs can, for the most part, be carried over and be of benefit to EEPROMs. A key example is the requirement of high-quality, very low leakage oxide between the two levels of polysilicon.

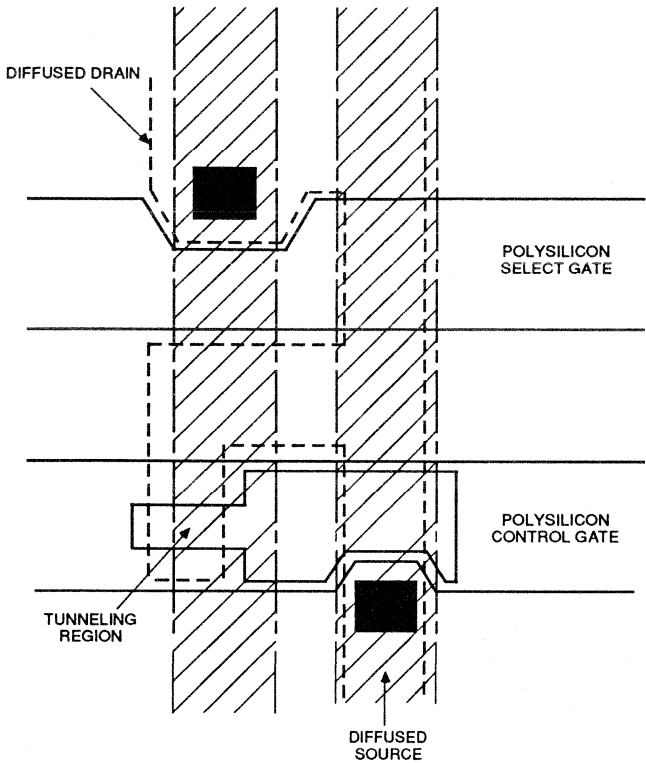
The NS-18 process used for the fabrication of the Am2864AE and Am2864BE utilizes 5X stepper lithography. AMD's six-inch wafer fabrication area is located in Austin, Texas. The key features of the N-channel MOS floating gate technology include:

- 100 Å thermally grown tunnel oxide
- Polysilicon floating gates and word lines
- Silicon-doped aluminium metallization
- A sacrificial gate oxide to ensure quality of the finished (regrown) gate oxide
- Cell size: 188  $\mu^2$
- Contact size: 2  $\mu$
- Gate width: 2  $\mu$
- Metal pitch: 6.75  $\mu$
- Junction depth: .5  $\mu$
- Die size: 201 x 231 mils



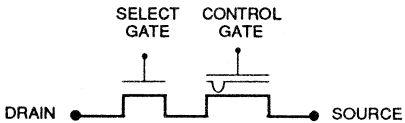
10324A-001A

Figure 1. Am2864AE/BE Cell Cross-Section



10324A-002A

Figure 2. Am2864AE/BE Cell—Top View



10324A-003A

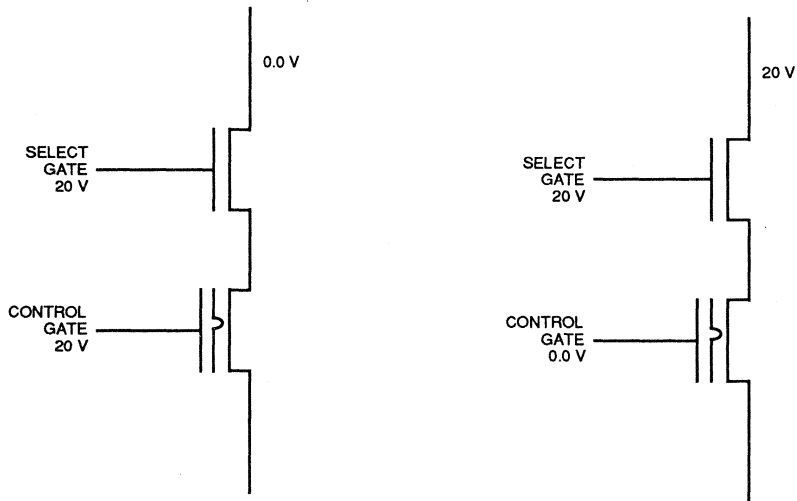
Figure 3. EEPROM Memory Cell

**NOTE ON FLOATING-GATE CHARGE STORAGE**

EEPROMs exploit floating-gate charge storage to achieve non-volatile storage of data. The charge is stored on an oxide-encapsulated polysilicon gate (see Figure 1). The "floating" gates offer excellent charge-retention characteristics. When the floating gate is charged negatively (electrons on floating gate), the source/drain current in the floating-gate transistor is essentially zero, as the negatively charged floating gate has induced positive charge accumulation under the gate, blocking any current flow between the n+ source/drain areas. When the floating gate is charged positively (lack of electrons on the floating gate), the source/drain current is very high, as the positively charged gate has induced an n-type channel under the floating gate, allowing conduction between the n+ source/drain areas.

Programming the floating-gate transistor is achieved by applying high voltages to the cells in question so that electrons are deposited on, or erased from, the floating

gate. To program a "one", electrons must be "tunneled" onto the floating gate. The voltages required to achieve this are shown in Figure 4a. Electrons are supplied from the diffused drain (see Figure 1), which is held at 0 V potential. These electrons are conducted in the channel of the select-gate transistor, which is turned "on" as the select-gate voltage approaches 20 V. The control-gate voltage also approaches 20 V. Electrons are now available at the n+ side of the tunnel oxide, and may "tunnel" onto and be stored on the floating gate. To program a "zero", electrons must "tunnel" (be erased) off of the floating gate. The voltages required to achieve this are shown in Figure 2-4b. Electrons are available from the floating gate. The diffused drain is raised to 20 V, as is the select gate, while the control gate is held at 0 V. The electrons may now "tunnel" from the floating gate, through the thin oxide to the n+ diffusion under the thin oxide, and be conducted through the channel under the select-gate transistor to the diffused drain.

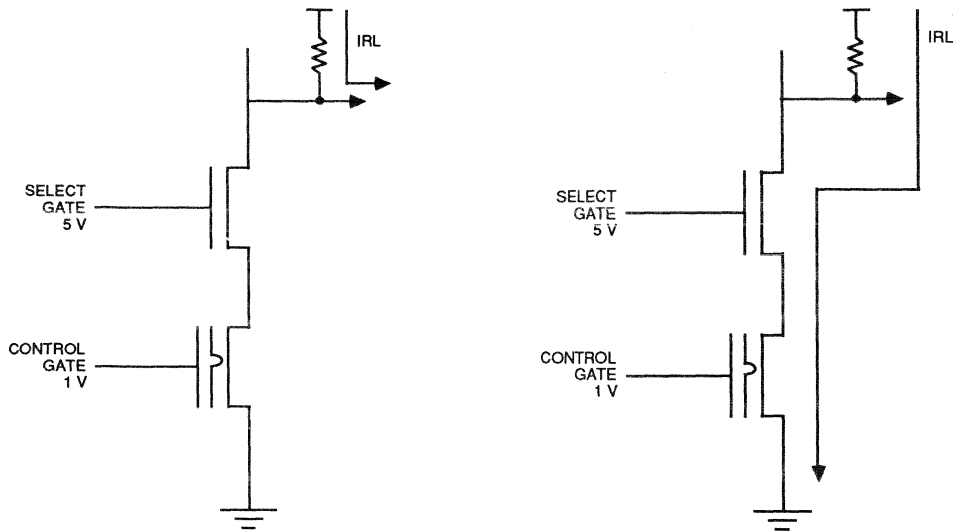


10324A-004A

a. Programming a "1" on an EEPROM Memory Cell

b. Programming a "0" on an EEPROM Memory Cell

**Figure 4. Programming on an EEPROM Memory Cell**



10324A-005A

a. Programming a "1" on an EEPROM Memory Cell

b. Programming a "0" on an EEPROM Memory Cell

Figure 5. Reading on an EEPROM Memory Cell

Figures 5a and 5b illustrate the cell operation during a "read" of the memory cell. Figure 5a, for a programmed transistor, will be read by applying approximately 5 V to the select gate and approximately 1 V to the control gate. Since the floating gate has been programmed to "one" (electrons on the floating gate), the floating-gate transistor does not conduct current from source to drain. The current (available through the "generic" resistor IRL) is made available to the sense amplifier, and is read as a "one". In Figure 5b, the floating gate has been programmed to zero (electrons "erased" from the floating gate). In the selected state, it will conduct source/drain current to ground, depriving the sense amplifier of current, and reading a "zero".

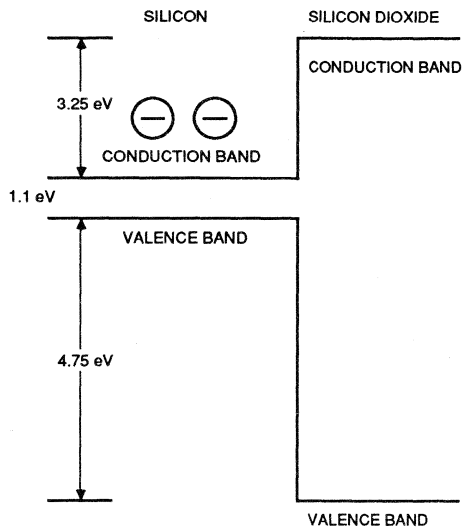
### NOTE ON CHARGE TUNNELING

Since EEPROMs rely on electron tunneling through thin oxides, an explanation of how these charges move from a semiconductor (polysilicon) through an insulator (silicon dioxide) is useful.

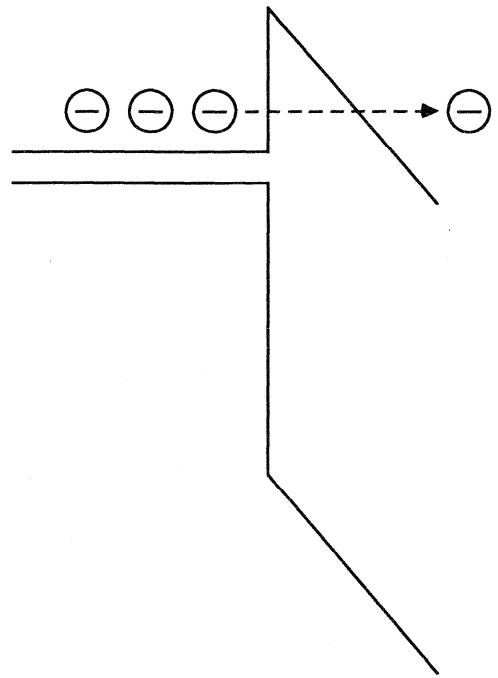
Consider the silicon-to-silicon-dioxide interface at equilibrium. The energy difference between the conduction and valence bands in silicon is approximately 1.1 eV. The difference between the conduction and valence bands in silicon dioxide is approximately 9 eV. When these materials are joined, the conduction band of silicon dioxide is approximately 3.25 eV above that of the silicon. Because an electron possesses a thermal energy of only approximately 0.025 eV at room temperature, the probability of an electron in silicon gaining enough energy to overcome the difference in energy and emerge in the conduction band in silicon is quite small (see Figure 6a).

However, under the presence of a strong electric field, the energy bands will become distorted, as in Figure 6b. Under these circumstances, a finite probability exists that an electron in the silicon may "tunnel" through the energy barrier and emerge in the conduction band of

**Process Information**



10324A-006A



10324A-007A

**Figure 6a. Energy Band During Equilibrium**

**Figure 6b. Energy Band During Tunneling**

silicon dioxide. It may now pass through the insulation and be "stored" on the floating gate. By reversing the electric field, the electron can be removed from the floating gate through the tunnel oxide in a similar fashion.

This effect was first observed by Fowler and Nordheim in the early 1900's for electrons emitted from metals in a vacuum. In 1969, Lenzlinger and Snow observed the phenomenon in the silicon dioxide system.



# EEPROM Reliability

The reliability of AMD's NS-18 process used in the fabrication of 64K EEPROMs is described in this report. The reliability monitors used at AMD were designed to predict the future operating life results by accelerating failure rates. The monitors include data from endurance testing, data retention, high-temperature operating life (HTOL), and temperature cycling. These reliability monitors were designed to catch specific kinds of failure mechanisms, such as endurance failures, oxide failures, and read disturb failures. The qualification data for the Am2864AE/BE was not completed when this report was published. The Am2864B uses the same process as the Am2864AE/BE. The following Am2864B data demonstrates that the NS-18 process is highly reliable.

## FAILURE MECHANISMS AND RELATED RELIABILITY DATA

The failures of an EEPROM memory are very closely related to the nature of the cell. Since the cell is a floating-gate cell with a thin tunnel oxide region, the failure modes are logically the well-understood EPROM failures, plus those associated with the presence of the tunnel oxide. Each of these failure modes is described in the following section.

## EPROM-Type Cell Failure

Because the excellent charge retention of floating-gate structures has been proven on EPROMs, the failure rate is very low. However, EPROM-type failures are typically single-bit failures; the cell can be programmed and erased, but cannot retain the information over a long period of time. This is due to a charge loss or charge gain through the gate or interpoly silicon oxide of the cell. The screening methods included in the standard test flow are similar to those used for EPROMs. They include a high-temperature bake (at 200°C) and a dynamic burn-in (at 150°C). The design of the Am2864AE/BE incorporates margin testing capabilities that allow the detection of shifts in any of the cell thresholds due to charge loss.

## Peripheral-Oxide Failure

To charge and discharge an electrically erasable EE cell array, high voltages ( $\approx 20$  V) are generated in the peripheral circuitry and applied to each cell via the accessing circuitry. Because an EEPROM must endure at least  $10^4$  cycles, numerous peripheral-gate oxides are subjected to high electric fields, resulting in possible breakdowns. Standard oxide-screening techniques and careful internal  $V_{pp}$  control are used in the test flow to minimize this problem.



**Table 1. EEPROM Reliability Monitor Data**  
(From 1/1/84 to 12/31/87)

Type of Stress	No. Lots	Sample Size	No. Rej.	Failure Rate	Failure Rate at *55°C**	Failure Rate at 70°C**
Early life, 160 hours, 125°C	12	3,017	3	0.1	-	-
HTOL, 1000 hours, 125°C	6	718	0	0.13	31 FITS	77 FITS
HTOL, 1000 hours, 150°C	12	874	0	0.11	9 FITS	23 FITS
Temperature Cycle, 1000 cycles, -65 to 150°C	10	497	1	0.20	-	-

All units in early life and HTOL stresses are dynamically exercised while in stress.

\* Failure rate calculated using 60% upper confidence level at test temperature.

\*\* Failure rates calculated using activation energy of 0.6 eV in FITS (failures per billion unit hours).

### Read-Disturb Mechanism

During the reading of an EE cell, the voltage applied between the drain and the control gate of the cell may induce a very weak Fowler-Nordheim tunneling that can modify the charge of the floating gate. A very long stress is necessary to detect a shift in threshold voltage of the cell. In the Am2864AE/BE the drain voltage during read has been set very close to the control-gate voltage to minimize the electric field across the tunnel oxide. Figure 1. illustrates an accelerated read-disturb experiment for a single typical cell, and the worst-case cell in the array. The voltage applied on the drain (4 V) creates an acceleration factor of  $10^3$  for the tunneling current, compared with normal (1.5 V) read conditions. This clearly shows that even the worst bit cell of the array keeps enough charge after ten years to assure correct reading.

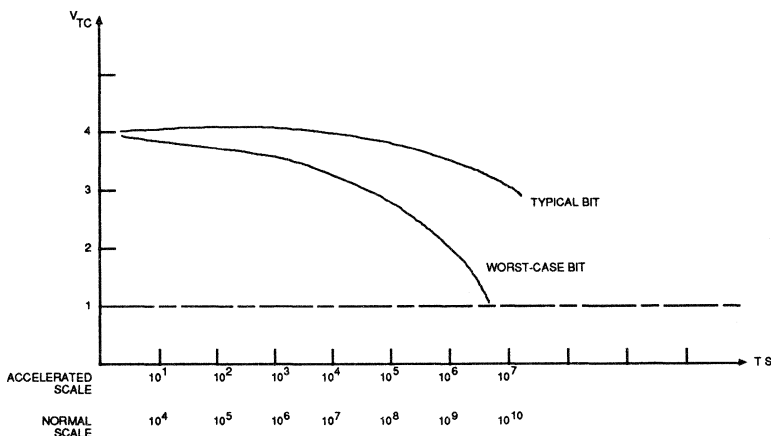
### Thin-Oxide Failures

These are single-bit failures caused by tunnel-oxide breakdown or degradation due to charge trapping that may occur during the programming of the cell. A catastrophic tunnel-oxide breakdown can be immediately detected since the cell cannot be written. A degradation of the tunnel oxide induces leakages that will affect the data retention of the cell.

The following parameters affect this failure mechanism:

- 1) The maximum value of the electric field across the tunnel oxide during programming has to be kept as low as possible. The Am2864AE/BE uses a cell that inherently minimizes this value (lower coupling). The internally generated  $V_{pp}$  is trimmable to  $\pm 1.0$  V around its normal value to compensate for process variations. A 1-ms  $V_{pp,n}$  rise time reduces the maximum transient electric field across the tunnel oxide.
- 2) The amount of charge that tunnels through the thin oxide is directly related to the number of write-erase operations. The Am2864AE/BE is specified for  $10^4$  cycles.
- 3) The quality and thickness uniformity of the tunnel oxide.

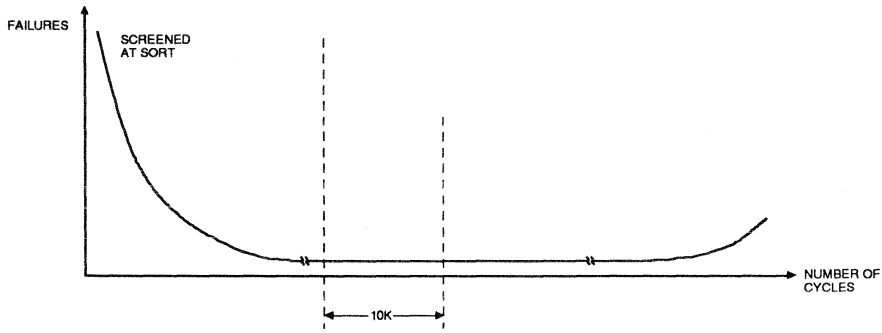
Screening for thin oxide failure is more complex because each write operation may alter the electrical properties of the tunnel oxide. Nevertheless, Figure 2. shows that thin-oxide failures follow a classical "bathtub" failure curve that makes the cycling performed during the test flow very effective in screening most of the thin oxide failures.



10324A-008A

Figure 1. Accelerated Read Disturb





10324A-009A

Figure 2. Thin-Oxide Failures

**Endurance Testing**

During 2864B endurance testing (Table 2), each byte of the memory is written and erased 10<sup>4</sup> times. At the end of the 10<sup>4</sup> cycles, the integrity of each bit is checked by an Erase-Write-Read Cycle and a 24-hour 250°C bake followed by a read. A damaged tunnel oxide loses

charge in a few hours. Since the degradation is due to multiple Write-Erase Cycles, this charge loss must be considered an endurance failure. During 2864B 100K endurance testing (Table 3), each byte of memory is written and erased 100,000 times (total). The integrity of each bit is checked at each point by an Erase-Write-Read Cycle and a 24-hour 250°C bake followed by a read.



Table 2. Am2864B Endurance Data

Number of Devices	Number of Failures After 10 <sup>4</sup> Write-Erase Cycles	Percent Failure
150 (4 lots)	2 - Charge Loss	2.0
	1 - Fails to Program Prior to Bake	
	3 - Total	

Table 3. Am2864B 100K Endurance Test

Read Point (Cycles)	7-V V <sub>cc</sub> —60 Units (3 Lots) # Fail	5.5-V V <sub>cc</sub> —138 Units (4 Lots) # Fail
10K	0	0
20K	2	5
100K	25	29
Total Fail	27	34
% Fail/10K (Cycles)	4.5	2.46
# Bits Charge Loss	23	23
# Bits Charge Gain	22	19

## EEPROM Reliability

Table 4. 2864B Data Retention Bake (250°) Reliability

Sample Size	168 Hours	500 Hours	668 Hours	1000 Hours	Cumulative Failures
323 (3 lots)	2	2	5	0	9

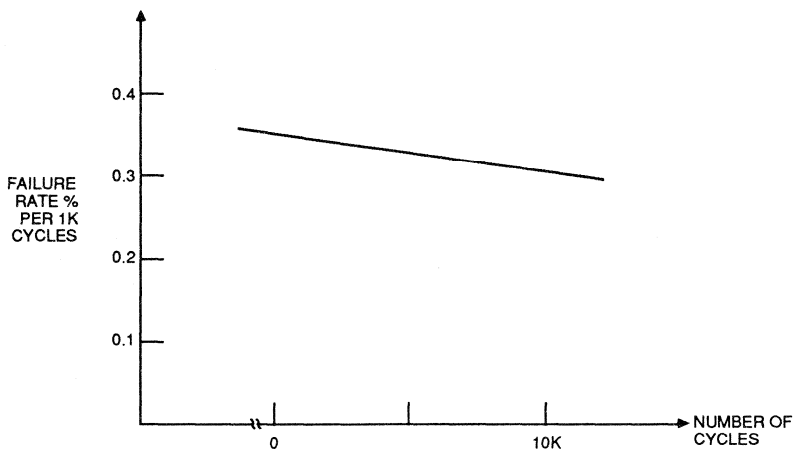
Failure Rate\*: 3.2

Failure Rate at 55°C\*\*: 12 FITS

Failure Rate at 70°C\*\*: 30 FITS

\* Failure rate calculated using 60% confidence level at test temperature.

\*\* Failure rates calculated using activation energy of 0.6 eV in FITS (failures per billion unit hours).



10324A-010A

Figure 3. Failure Rates

Figure 3 shows the failure rate as a function of number of cycles. Since most of the infant mortality has been screened during the test flow, this failure rate only slightly decreases with the number of cycles.

The 7-V  $V_{CC}$  has been estimated to have a 2X-6X acceleration factor as compared to the 5.5-V  $V_{CC}$ .

## SUMMARY

In this report we discussed a number of different EEPROM failure mechanisms.

The Am2864AE/BE data-retention results are comparable to those found on EPROMs. There is no read-disturb problem, and once written, the memory can be read indefinitely. Endurance failures (mainly through tunnel oxide degradation) are the main contributors to the overall failure rate.



# Cross-Reference and Conversion Guides

## COMPETITOR CROSS-REFERENCE GUIDE

The following table serves as a cross-reference guide for competitive EEPROM devices. In some cases, AMD's devices are exactly equivalent. In others, there are AC

and DC timing and operating characteristics that are different. Please consult the data sheets or your local AMD representative for more details.

Table 1a. XICOR Functional Equivalence

XICOR	AMD	XICOR	AMD
<b>"A" Series—28-Pin DIP</b>		<b>"A" Series—32-Pin LCC (continued)</b>	
<b>COMMERCIAL</b>		<b>MILITARY TEMP</b>	
X2864AD-25	Am2864AE-255DC *	X2864AEM-25	Am2864AE-250LE
X2864AD	Am2864AE-305DC *	X2864AEM	Am2864AE-300LE
X2864AD-35	Am2864AE-355DC *	X2864AEM-35	Am2864AE-350LE
X2864AD-45	Am2864AE-355DC *, †	X2864AEM-45	Am2864AE-350 LE †
<b>INDUSTRIAL</b>		<b>MILITARY 883-C</b>	
X2864ADI-25	Am2864AE-250DI	X2864AEMB-25	Am2864AE-250/BUA
X2864ADI	Am2864AE-300DI	X2864AEMB	Am2864AE-300/BUA
X2864ADI-35	Am2864AE-350DI	X2864AEMB-35	Am2864AE-350/BUA
X2864ADI-45	Am2864AE-350DI †	X2864AEMB-45	Am2864AE-350/BUA †
<b>MILITARY TEMP</b>		<b>"B" Series—28-Pin DIP</b>	
X2864ADM-25	Am2864AE-250DE	<b>COMMERCIAL</b>	
X2864ADM	Am2864AE-300DE	X2864BD-18	Am2864AE-205DC *, #
X2864ADM-35	Am2864AE-350D	<b>INDUSTRIAL</b>	
X2864ADM-45	Am2864AE-350DE †	X2864BDI-18	Am2864AE-205DI *, #
<b>MILITARY 883-C</b>		<b>MILITARY TEMP</b>	
X2864ADMB-25	Am2864AE-250/BXA	X2864BDM-18	Am2864AE-205DE *, #
X2864ADMB	Am2864AE-300/BXA	<b>MILITARY 883-C</b>	
X2864ADMB-35	Am2864AE-350/BXA	X2864BDMB-18	Am2864AE-250/BXA *, #
X2864ADMB-45	Am2864AE-350/BXA †	<b>"B" Series—32-Pin LCC</b>	
<b>"A" Series—32-Pin LCC</b>		<b>COMMERCIAL</b>	
X2864AE	Am2864AE-255LC *	X2864BE-18	Am2864AE-205LC *, #
X2864AE	Am2864AE-305LC *	<b>INDUSTRIAL</b>	
X2864AE-35	Am2864AE-355LC *	X2864BEI-18	Am2864AE-205LI *, #
X2864AE-45	Am2865AE-355LC *, †	<b>MILITARY TEMP</b>	
<b>INDUSTRIAL</b>		X2864BEM-18	Am2864BE-205LE *, #
X2864AEI-25	Am2864AE-250LI	<b>MILITARY 883-C</b>	
X2864AEI	Am2864AE-300LI	X2864BEMB-18	Am2864AE-250/BUA *, #
X2864AEI-35	Am2864AE-350LI		
X2864AEI-45	Am2864AE-350LI †		

Notes: \* Also available in  $\pm 10\%$   $V_{cc}$ .

† AMD is 100 ns faster.

# Functionally equivalent. AC and DC differences.

## Cross-Reference and Conversion Guides

Table 1b. SEQ Functional Equivalence

SEEQ	AMD	SEEQ	AMD
<b>28-Pin DIP</b>		<b>32-Lead LCC</b>	
<b>COMMERCIAL</b>		<b>COMMERCIAL</b>	
DQ2864-250	Am2864BE-250DC #	LQ2864-250	Am2864BE-250LC #
DQ2864-300	Am2864BE-300DC #	LQ2864-300	Am2864BE-300LC #
DQ2864-35	Am2864BE-355DC #	LQ2864-35	Am2864BE-355LC #
<b>MILITARY TEMP</b>		<b>MILITARY TEMP</b>	
DM2864-250	Am2864BE-250DE #	LM2864-250	Am2864BE-250LE #
DM2864-300	Am2864BE-300DE #	LM2864-300	Am2864BE-300LE #
DM2864-35	Am2864BE-355DE #	LM2864-35	Am2864BE-355LE #

Note: # Functionally equivalent. AC and DC differences.

### 64K CONVERSION GUIDE

The following tables serve as a cross-reference from AMD's obsolete 64K EEPROMs (the Am9864, Am2864A, and Am2864B) to the Am2864AE and Am2864BE.

### Am9864 Conversion to Am2864BE

Most Am9864 applications can be filled by the Am2864BE. Tables 2 and 3 indicate where the obsolete Am9864 has tighter parameters than the Am2864BE. Special screening may be performed for a particular application. Consult the local AMD Sales Office for feasibility and cost.

Table 2. AC Characteristics (Am9864 Conversion to Am2864BE)

Parameter Symbol	Parameter Description		-205, -200		-255, -250		-305, -300		-355, -350		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{DF}$	Output Enable or Chip Enable HIGH to Output Float	9864	-	-	0	-	0	-	0	-	ns
		2864BE	-	-	10	-	10	-	10	-	
$t_{OH}$	Output Hold from Address Change	9864	-	-	0	-	0	-	0	-	ns
		2864BE	-	-	20	-	20	-	20	-	
$t_{WP}$	$\overline{WE}$ or $\overline{CE}$ Write Pulse Width	9864	-	-	100	-	100	-	150	-	ns
		2864BE	-	-	150	-	150	-	200	-	
$t_{DS}$	Data Setup Time	9864	-	-	50	-	50	-	70	-	ns
		2864BE	-	-	100	-	100	-	120	-	
$t_{DH}$	Data Hold Time	9864	-	-	-	-	-	-	20	-	ns
		2864BE	-	-	-	-	-	-	30	-	

Table 3. DC Characteristics (Am9864 Conversion to Am2864BE)

Parameter Symbol	Parameter Description		Min.	Max.	Unit
$I_{CC1}$	$V_{CC}$ Current (Standby)	9864	–	40	mA
		2864BE	–	70	
$I_{CC2}$	$V_{CC}$ Current (Active) (Includes Write Operation)	9864	–	100	mA
		2864BE	–	140	

**Am2864A/B Conversion to Am2864AE/BE**

Most of the current Am2864A and Am2864B applications can be filled by the Am2864AE and Am2864BE. Tables 4 and 5 indicate where the soon-to-be-obsolete Am2864A/B have tighter parameters than

the Am2864AE/BE. The 2864AE/BE are both screened to the tighter 2864BE test tape. Provisions are made to account for the pin 1 No Connect on the 2864AE. Special screening may be performed for a particular application. Consult the local AMD Sales Office for feasibility and cost.

Table 4. AC Characteristics (Am2864A/B Conversion to Am2864AE/BE)

Parameter Symbol	Parameter Description		-205, -200		-255, -250		-305, -300		-355, -350		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{DF}$	Output Enable or Chip Enable HIGH to Output Float	2864A/B	0	–	0	–	0	–	0	–	ns
		2864AE/ 2864BE	10	–	10	–	10	–	10	–	
$t_{OH}$	Output Hold from Address Change	2864A/B 2864AE/ 2864BE	0	–	0	–	0	–	0	–	ns
$t_{WP}$	$\overline{WE}$ or $\overline{CE}$ Write Pulse Width	2864A/B	100	–	100	–	120	–	150	–	ns
		2864AE/ 2864BE	150	–	150	–	150	–	200	–	
$t_{DS}$	Data Setup Time	2864A/B	50	–	50	–	50	–	70	–	ns
		2864AE/ 2864BE	100	–	100	–	100	–	120	–	
$t_{OES}$	$\overline{OE}$ Setup Time	2864A/B	0	–	0	–	0	–	0	–	ns
		2864AE/ 2864BE	10	–	10	–	10	–	10	–	
$t_{OEH}$	$\overline{OE}$ Hold Time	2864A/B	0	–	0	–	0	–	0	–	ns
		2864AE/ 2864BE	10	–	10	–	10	–	10	–	

$t_{WW}$  Max. is not specified on the Am2864AE/BE since it is not a gating factor for initiating a Write Cycle.

## Cross-Reference and Conversion Guides

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**Table 5. DC Characteristics (Am2864A/B Conversion Am2864AE/BE)**

Parameter Symbol	Parameter Description		Min.	Max.	Unit
$I_{CC1}$	$V_{CC}$ Current (Standby)	2864A/B	–	40	mA
		2864AE/ 2864BE	–	70	
$I_{CC2}$	$V_{CC}$ Current (Active) (Includes Write Operation)	2864A/B	–	120	mA
		2864AE/ 2864BE	–	140	



# Die Business

## Am2864AE/BE DICE AGREEMENT

AMD sells EEPROM dice at the commercial grade level to authorized distributors and OEM customers. Full testing is not possible on EEPROM dice. The

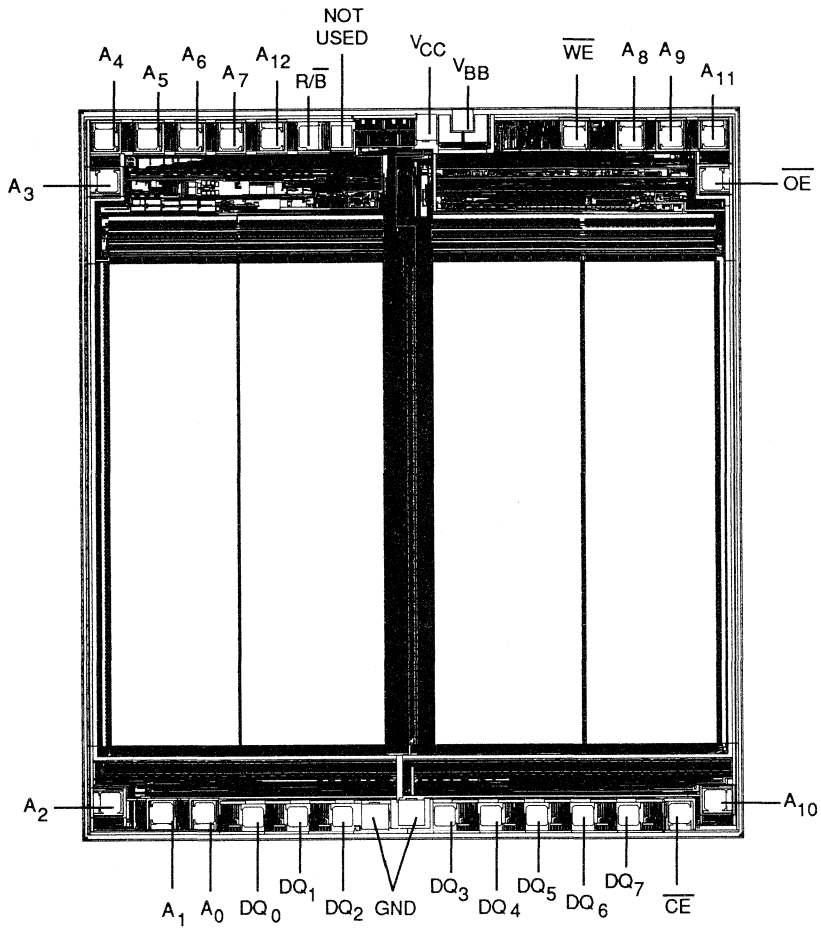
Am2864AE/BE Dice Agreement (see Figure 5-1 for an example) describes the guarantees and limitations associated with this business.

Am2864AE/BE DICE AGREEMENT			
A) Specifications:	Operating Temperature Range = 0 to +70°C Power Supply = $V_{CC} \pm 10\%$ $t_{AA} = 250$ ns $V_{IN} = 0.45$ to 2.4 V Die Thickness = 675 $\pm$ 20 microns		
B) Test Requirements:	<ol style="list-style-type: none"><li>1. AMD will perform the following tests:<ol style="list-style-type: none"><li>a) 2000 cycles for endurance are done. Tests performed by AMD would have screened infant endurance failures.</li><li>b) Wafer sort at 25°C. AC/DC testing at 25°C guard-banded for 0 to +70°C operation (dice are programmed).</li><li>c) Wafers are baked at 200°C (24 hours).</li><li>d) Probe for data loss and AC/DC tested again.</li><li>e) Scribe/die plate/second optical inspection.</li></ol></li><li>2. Customer to perform the following tests as a minimum:<ol style="list-style-type: none"><li>a) Program (dice will arrive with pattern).</li><li>b) AC/DC testing at +70°C.</li><li>c) Perform burn-in at 125°C for 168 hours.</li></ol></li></ol>		
C) Liability Agreement	<ol style="list-style-type: none"><li>1. AMD will be liable for all process-related failures.</li><li>2. AMD will take no responsibility for yield losses and/or reliability failures that are assembly-related.</li></ol>		
D) Yield Guarantees	<ol style="list-style-type: none"><li>1. AMD will provide the customer all technical information concerning recommended test programs and procedures, as required, to optimize yield.</li><li>2. No guarantees exist on yields for:<ol style="list-style-type: none"><li>a) Speed (<math>t_{ACC}</math>) better than 250 ns</li><li>b) Assembly yield</li><li>c) Yields at temperatures outside 0 to +70°C</li></ol></li></ol>		
E) Data Pattern	<ol style="list-style-type: none"><li>1. Data pattern of all memory cells will be initialized to all "1"s before shipment.</li></ol>		
Customer/Title _____	(Date) _____	AMD/Title _____	(Date) _____

3

Figure 1. Am2864AE/BE Dice Agreement Example

10324A-011A



10324A-012A

Die Size: 201 x 231 mils  
Equivalent Gate Count: 60, 517

Figure 2. Metalization and Pad Layout





# False-Write-Protect Circuit Design

by Brian T. Johansen, Syntrex, Inc., and Anthony DiColli, Advanced Micro Devices, Inc.

## INTRODUCTION

The Am2864AE/BE EEPROMs are internally protected from false writes when  $V_{CC}$  is below 3.0 V. When system logic levels are undefined, it is the supply voltage range between 3.0 and 4.5 V that causes problems for EEPROM users. The following text describes an effective means to protect against false writes during power-up/power-down.

## EEPROM WRITE-PROTECT MECHANISMS

An EEPROM requires that the  $\overline{CE}$ ,  $\overline{WE}$ , and  $\overline{OE}$  pins be in the proper state to allow a data Write Cycle to occur. The Am2864AE/BE are designed in such a way that either the  $\overline{CE}$  or the  $\overline{WE}$  pins can be used to initiate a Write Cycle. During a system Write Cycle, the address is latched into the internal address latch on the last falling edge of  $\overline{WE}$  or  $\overline{CE}$ , providing that  $\overline{OE}$  is a logic "1". The first rising edge of  $\overline{WE}$  or  $\overline{CE}$  latches the data into the data latches. In addition, there is a  $\overline{WE}$  lockout circuit that

prevents  $\overline{WE}$  pulses of less than 20 ns duration from initiating a Write Cycle. If these logic inputs can be forced into a non-Write-Cycle state during power-up/power-down, then data security will be assured. There are two ways to do this: hold  $\overline{OE}$  LOW, or hold  $\overline{CE}$  HIGH during power-up/power-down (reference Table 1).

Write-protect schemes that utilize the  $\overline{OE}$  pin may cause the EEPROM data pins ( $DQ_0$ - $DQ_7$ ) to be in a driven state during power-up/power-down. This could cause data bus contention if other devices share the data bus. Techniques that use this control pin should only be considered if 1) the EEPROM data bus is not shared with any other chip, or 2) in shared data bus designs, the other chips can be prevented from driving the bus during power-up/power-down.

Designs that use the  $\overline{CE}$  pin to write-protect the contents of EEPROMs ensure that the data bus will remain in the high-impedance mode, thereby eliminating any possibility for bus contention during power-up/power-down.

Table 1. Mode Selection

Inputs			Outputs			
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$R/\overline{B}$	I/O	$A_0$	Mode
L	L	H	Hi-Z	Data Out	X	Read
L	H			Data In	X	Write
	H	L		Data In	X	Write
H	X	X	Hi-Z	Hi-Z	X	Standby
L	H	H	Hi-Z	Hi-Z	X	Read Inhibit
L	L		Hi-Z	Hi-Z	X	Write Inhibit
L	L	H	Hi-Z	Code	$V_H$	Auto Select
L	L	H	L	$\overline{D}_n$	X	$\overline{\text{Data}}$ Polling

Key:  $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$   
 H = HIGH  
 L = LOW  
 X = Don't Care  
 = Pulse

## False-Write-Protect Circuit Design

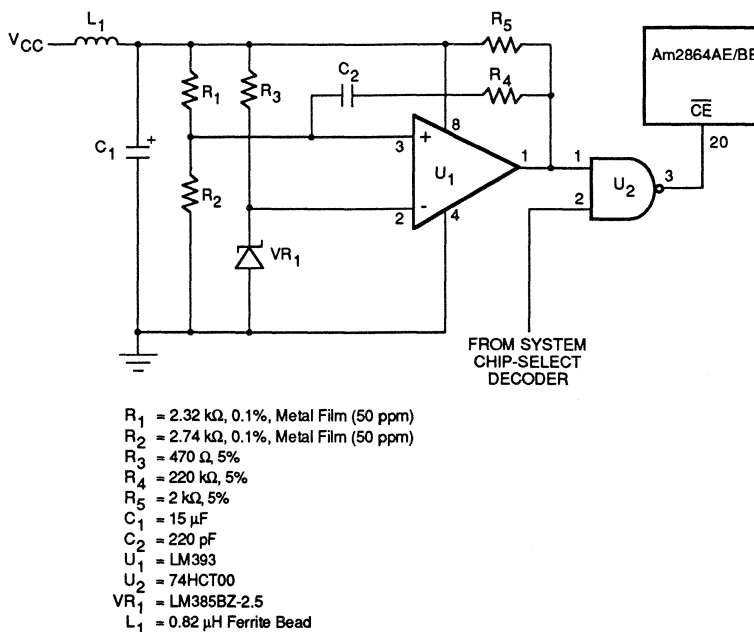


Figure 1. Am2864AE/BE False Write Protection

The design described in this chapter utilizes the  $\overline{\text{CE}}$  pin to provide the write-protect function. However, this same design can be used in  $\overline{\text{OE}}$  write-protect schemes simply by using a non-inverting gate at location  $U_2$  in Figure 1.

### CIRCUIT OPERATION

The circuit schematic is shown in Figure 6-1. An LM 393 comparator is used to sense when  $V_{\text{CC}}$  exceeds 4.5 V. The inverting input to the comparator is set to a 2.5 V reference by  $VR_1$ . The voltage divider formed by  $R_1$  and  $R_2$  allows the sense voltage to set the trip point. If adjustment of this threshold is desired, then a potentiometer can be substituted for either  $R_1$  or  $R_2$ . When  $V_{\text{CC}}$  is below 4.5 V, the inverting input to the comparator will be at a higher voltage than the non-inverting input, thereby forcing the comparator's output LOW. This LOW is applied to the 74HCT00 which then provides a HIGH to

the  $\overline{\text{CE}}$  pin of the Am2864AE/BE. An HC- or HCT-type of gate must be used to ensure correct operation at  $V_{\text{CC}}$  voltages under 3.0 V. When the input voltage exceeds 4.5 V, the comparator's non-inverting input will be at a higher voltage than the inverting input. The open-collector comparator output will be pulled up by  $R_5$ , allowing the system access to the EEPROM. On power-down, similar circuit operation takes place—when the  $V_{\text{CC}}$  falls below 4 V, the  $\overline{\text{CE}}$  pin is forced HIGH, prohibiting Write Cycles.

$L_1$  is a 0.82  $\mu\text{H}$  ferrite bead, used in conjunction with  $C_1$  to help filter out any noise spikes or ripple from the  $V_{\text{CC}}$  line.  $VR_1$  is a precision 2.5 V reference, biased into its calibration range by  $R_3$ .  $C_2$  and  $R_4$  provide AC-coupled hysteresis into the non-inverting input of the comparator to ensure an oscillation-free transition for the slow rise time of the  $V_{\text{CC}}$  input. These components also provide the overdrive to the comparator input, increasing the switching speed.



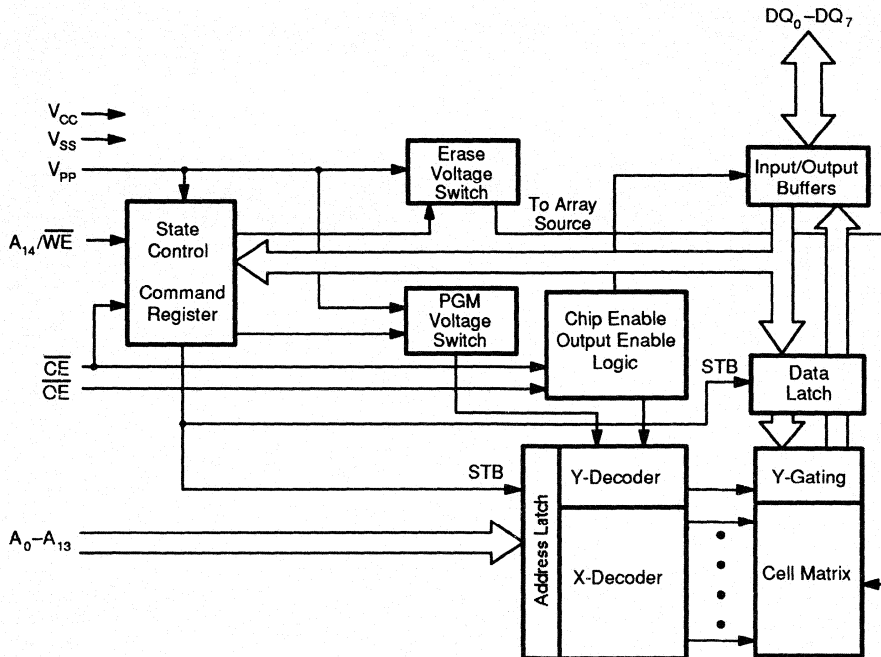
# Am27F256

## 32,768 x 8-Bit CMOS Windowless EPROM

### DISTINCTIVE CHARACTERISTICS

- **Flasherase™ Electrical Bulk Chip-Erase**
  - One Second Typical Chip-Erase
- **Compatible with JEDEC Standard Byte Wide EPROM pinouts**
  - 28-pin DIP
  - 32-pin PLCC
- **Flashrite™ Programming**
  - 10μS Typical Byte-Program
  - Less than 0.5 Second Typical Chip Program
- **Advanced CMOS Technology**
  - EPROM Compatible Process
  - Extensive Manufacturing Experience
- **Low Power Consumption**
  - 30mA Maximum Active Current
  - 100 μA Maximum Standby Current
- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**
- **100 Program/Erase Cycles**
- **Program and Erase Voltage**  
**+12.75V ± 0.25V V<sub>PP</sub>**
- **High Performance**
  - 90ns Maximum Access Time
- **Allows for Auto-Insertion**
- **5V±10% Single Power Supply**

### BLOCK DIAGRAM



11557-001A

The document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product, AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication #	Rev.	Amendment
11557	A	/0
Issue Date: February, 1989		

## GENERAL DESCRIPTION

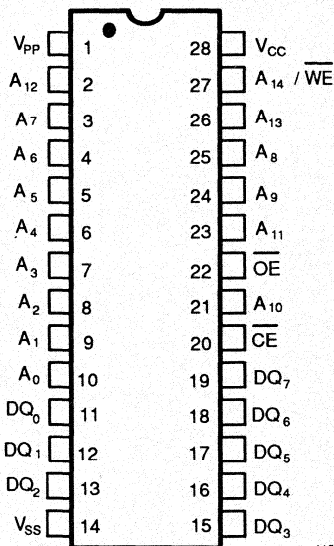
This device is an alternative to the standard U.V. EPROM.

The Am27F256 CMOS windowless EPROM provides the industry's highest performance and most cost-effective alternative for reprogrammable non-volatile memory. It is organized as 32K bytes of 8 bits each. The Am27F256 is pin compatible with the 28 pin byte-wide JEDEC 256K EPROM. The 27F256 is targeted for alterable code- or data-storage applications where ultraviolet erasure is impractical or time consuming. The window-

less EPROM adds electrical Flash chip-erasure and reprogrammability in plastic packaging to AMD's EPROM technology. The device may be packaged in plastic DIP or PLCC and is ideal for use in auto-insertion manufacturing systems. The entire memory content may be erased and reprogrammed using AMD's Flasherase™ and Flashrite™ programming algorithms respectively in a standard PROM programmer. Electrical erasure increases the memory's flexibility, while providing time savings over traditional UV erasing.

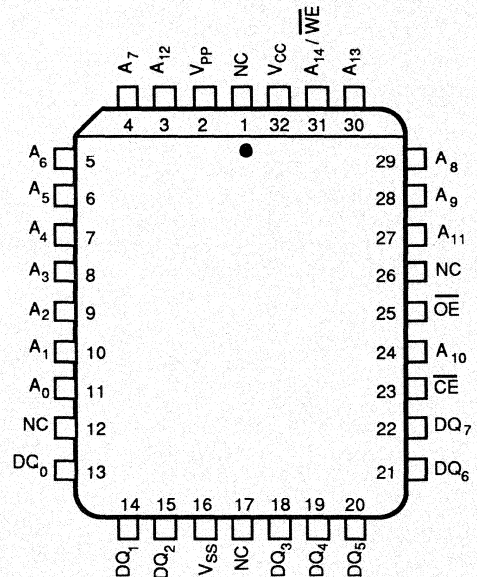
## CONNECTION DIAGRAMS

DIP



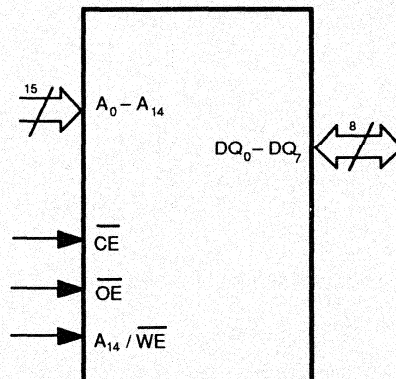
11557-002A

LCC/PLCC



11157-003A

## LOGIC SYMBOL



11557-004A

---

## FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming increases flash memory's flexibility over EPROM. Standard PROM programmers may be used for erasing and programming. A command register in the windowless EPROM manages these functions. The command register allows for fixed power supplies during the erase and programming functions, does not require high voltage on control pins, and provides maximum EPROM compatibility.

### Read Mode

The windowless EPROM device functions as a read only memory when high voltage is not applied to the  $V_{pp}$  pin. In this mode the external memory control signals produce the standard EPROM read, standby, output disable, and Auto-select modes.

### Programming/Read Mode

High voltage on the  $V_{pp}$  pin enables the erase and programming functions of the device. The same EPROM read, standby, and output disable functions are available to the system when high voltage is applied to the  $V_{pp}$  pin. All functions associated with altering memory

contents: erase, erase-verify, program, and program-verify—are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes.

The command register is alterable only when high voltage is applied to  $V_{pp}$ . When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory.

### Performance

AMD's windowless EPROMs offer access times as fast as 90ns which allows operation of high-speed microprocessors and microcontrollers without wait-states. The windowless EPROM architecture supports separate chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) controls in order to eliminate bus contention.

---

## OPERATING RANGES

### Commercial (C) Devices

Case Temperature ( $T_c$ )                      0°C to +70°C

### Industrial (I) Devices

Case Temperature ( $T_c$ )                      -40°C to +85°C

### Extended (E) Devices

Case Temperature ( $T_c$ )                      -55°C to +125°C

### Military (M) Devices

Case Temperature ( $T_c$ )                      -55°C to +125°C

*Operating ranges define those limits between which the functionality of the device is guaranteed.*



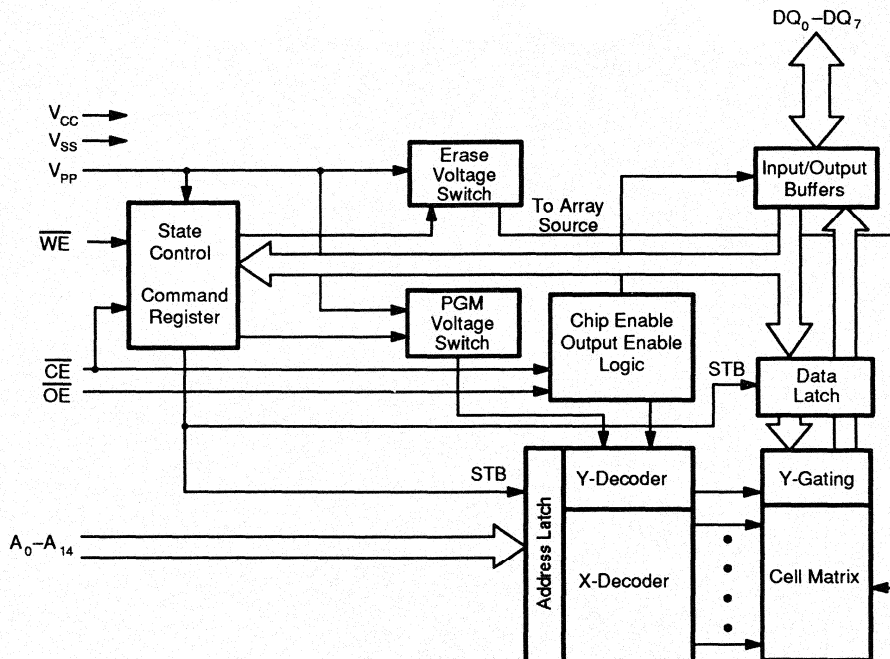
# Am28F256

32,768 x 8-Bit Flash E<sup>2</sup>PROM

## DISTINCTIVE CHARACTERISTICS

- **Flasherase™ Electrical Bulk Chip-Erase**
  - One Second Typical Chip-Erase
- **Compatible with JEDEC Standard Byte Wide 32-pin EEPROM Pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **Flashrite™ Programming**
  - 10 μS Typical Byte-Program
  - Less than 0.5 Second Typical Chip Program
- **Program and Erase Voltage 12.0V ± 5% V<sub>PP</sub>**
- **Advanced CMOS Technology**
  - EPROM Compatible Process
  - Extensive Manufacturing Experience
- **Low Power Consumption**
  - 30 mA Maximum Active Current
  - 100 μA Maximum Standby Current
- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**
- **10,000 Program/Erase Cycles**
- **Provides On-Board Functionality for In-System-Write**
- **High Performance**
  - 90 nS Maximum Access Time
- **On Board Address and Data Latches**
- **5V ±10% Single Power Supply**

## BLOCK DIAGRAM



11560-001A

## GENERAL DESCRIPTION

This device is an alternative to the full-featured EEPROM.

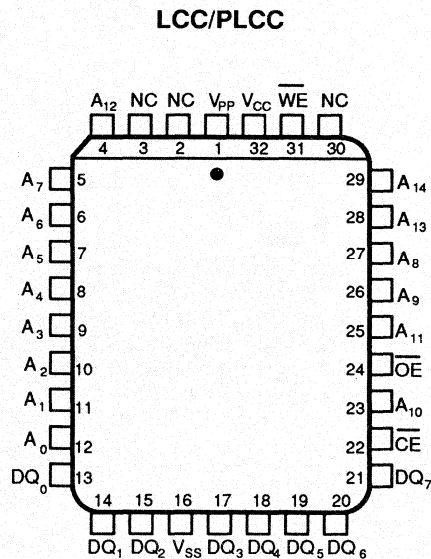
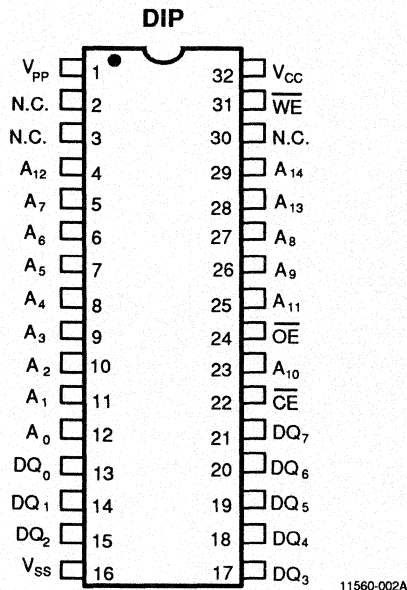
The 28F256 is targeted for in-system alterable code- or data-storage applications where full-feature EEPROM functionality is either not required or not cost effective. The Am28F256 CMOS Flash memory provides the highest performance and most cost-effective alternative for rewritable non-volatile memory. Flash memory adds electrical chip-erase and reprogramming to AMD's EPROM technology. The entire memory content may be Flash erased and reprogrammed OR PROM programmer, or test socket, on board during subassembly test, in-system during final test or after sale. In-system electrical erasure increases the memory's flexibility, while providing time and cost savings.

The device may be packaged in plastic DIP or PLCC and is ideal for use in auto-insertion manufacturing systems. The entire memory array may be erased and reprogrammed on-board using AMD's Flasherase™ and Flashrite™ programming algorithms respectively.

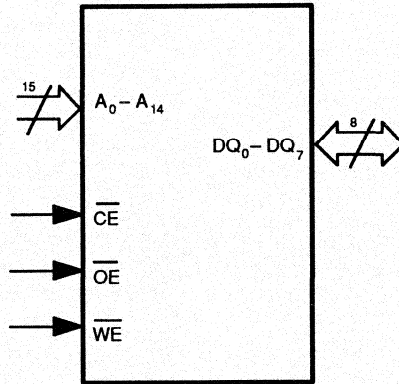
## Typical Applications

Flash memory is ideal for storing code or data-tables in embedded control applications where periodic updates or data down-loading may be required. Code updates may occur throughout the entire life of a system. Beginning with prototyping, code updates may also be necessary during subassembly or even in after-sale service. Electrical chip erasure eliminates the 15 to 20 minute ultraviolet erase and streamlines code updates. In addition both DIP or PLCC Flash devices may be soldered to the circuit board during subassembly. Test codes may be programmed into the device on board. Prior to shipment final code is downloaded to the device. Thus, Flash technology eliminates unnecessary handling and less reliable socketed connections, saves board space, and adds increased manufacturing flexibility. After-sale code updates are performed locally via an edge-connector, or remotely over a serial communication link.

## CONNECTION DIAGRAMS



## LOGIC SYMBOL



11560-004A

## FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming gives flash memory the flexibility of EEPROM. A command register in the Flash device manages the electrical erasure and reprogramming. The command register architecture allows for fixed power supplies during erasure and programming and does not require high voltage on control pins.

### Read Mode

The Flash device functions as a read only memory when high voltage is not applied to the  $V_{pp}$  pin. In this mode the external memory control signals produce the standard EPROM read, standby, output disable, and Auto-select modes.

### Programming / Read Mode

High voltage on the  $V_{pp}$  pin enables the erase and programming functions of the device. The same EPROM read, standby, and output disable functions are available to the system when high voltage is applied to the  $V_{pp}$  pin. All functions associated with altering memory contents (erase, erase-verify, program, and program-verify) are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as

input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes. As with EEPROM devices, the 28F256 uses a dedicated  $\overline{WE}$  control pin for command execution.

The command register is alterable only when high voltage is applied to  $V_{pp}$ . When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory.  $V_{pp}$  may be controlled with system hardware to provide secure write protect.

### Performance

AMD's Flash memories offer access times as fast as 90ns. This high performance allows operation of high-speed microprocessors and microcontrollers without wait-states. The Flash architecture supports separate chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) controls in order to eliminate bus contention.

## OPERATING RANGES

### Commercial (C) Devices

Case Temperature ( $T_c$ ) 0°C to +70°C

### Industrial (I) Devices

Case Temperature ( $T_c$ ) -40°C to +85°C

### Extended Commercial (E) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

### Military (M) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

*Operating ranges define those limits between which the functionality of the device is guaranteed.*





# Am27F512

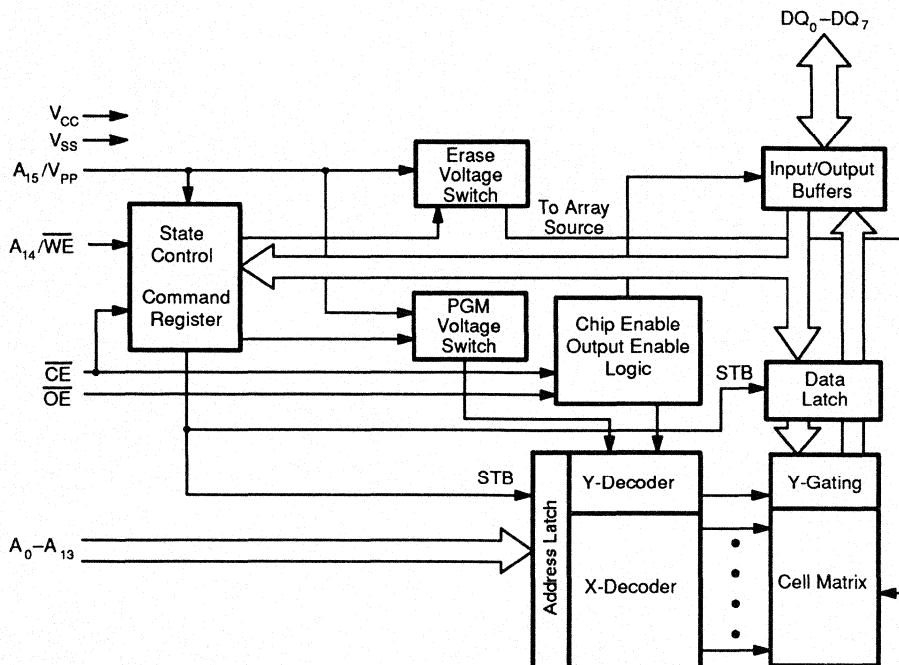
Advanced  
Micro  
Devices

## 65,536 x 8-Bit CMOS Windowless EPROM

### DISTINCTIVE CHARACTERISTICS

- **Flasherase™ Electrical Bulk Chip-Erase**
  - One Second Typical Chip-Erase
- **Compatible with JEDEC Standard Byte Wide EPROM Pinouts**
  - 28-pin DIP
  - 32-pin PLCC
- **Flashrite™ Programming**
  - 10 μS Typical Byte-Program
  - Less than 1 Second Typical Chip Program
- **Advanced CMOS Technology**
  - EPROM Compatible Process
  - Extensive Manufacturing Experience
- **Low Power Consumption**
  - 30 mA Maximum Active Current
  - 100μA Maximum Standby Current
- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**
- **100 Program/Erase Cycles**
- **Program and Erase Voltage +12.75V ±0.25V<sub>PP</sub>**
- **High Performance**
  - 100 nS Maximum Access Time
- **Allows for Auto-insertion**
- **5V ±10% Single Power Supply**

### BLOCK DIAGRAM



11558-001A

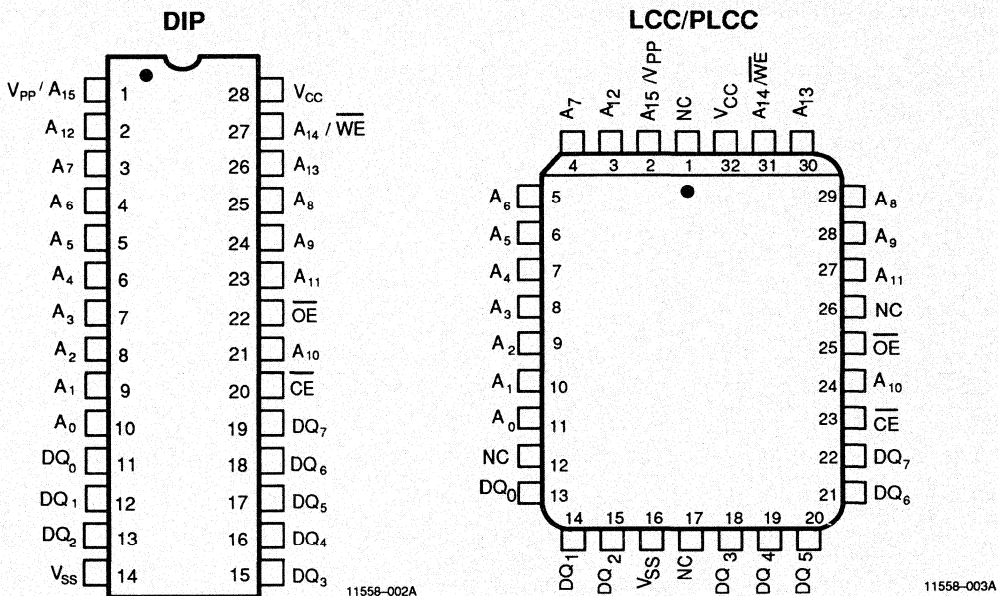
## GENERAL DESCRIPTION

This device is an alternative to the standard U.V. EPROM.

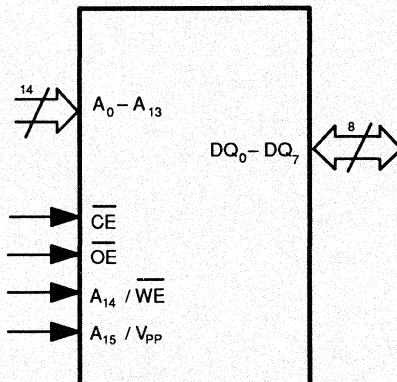
The Am27F512 CMOS windowless EPROM provides the industry's highest performance and most cost-effective alternative for reprogrammable non-volatile memory. It is organized as 64K bytes of 8 bits each. The Am27F512 is pin compatible with the 28 pin byte-wide JEDEC 512K EPROM. The 27F512 is targeted for alterable code- or data-storage applications where ultraviolet erasure is impractical or time consuming. The window-

less EPROM adds electrical Flash chip-erase and reprogrammability in plastic packaging to AMD's EPROM technology. The device may be packaged in plastic DIP or PLCC and is ideal for use in auto-insertion manufacturing systems. The entire memory content may be erased and reprogrammed using AMD's Flasherase™ and Flashrite™ programming algorithms respectively in a standard PROM programmer. Electrical erasure increases the memory's flexibility, while providing time savings over traditional UV erasing.

## CONNECTION DIAGRAMS



## LOGIC SYMBOL



11558-004A

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## FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming increases flash memory's flexibility over EPROM. Standard PROM programmers may be used for erasing and programming. A command register in the windowless EPROM manages these functions. The command register allows for fixed power supplies during the erase and programming functions, does not require high voltage on control pins, and provides maximum EPROM compatibility.

### Read Mode

The windowless EPROM device functions as a read only memory when high voltage is not applied to the  $V_{pp}$  pin. In this mode the external memory control signals produce the standard EPROM read, standby, output disable, and Auto-select modes.

### Programming/Read Mode

High voltage on the  $V_{pp}$  pin enables the erase and programming functions of the device. The same EPROM read, standby, and output disable functions are available to the system when high voltage is applied to the  $V_{pp}$  pin. All functions associated with altering memory contents: erase, erase-verify, program, and program-verify—are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes.

The command register is alterable only when high voltage is applied to  $V_{pp}$ . When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory.

### Performance

AMD's windowless EPROMs offer access times as fast as 100ns which allows operation of high-speed microprocessors and microcontrollers without wait-states. The windowless EPROM architecture supports separate chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) controls in order to eliminate bus contention.

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## OPERATING RANGES

### Commercial (C) Devices

Case Temperature ( $T_c$ ) 0°C to +70°C

### Industrial (I) Devices

Case Temperature ( $T_c$ ) -40°C to +85°C

### Extended (E) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

### Military (M) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

### Supply Read Voltages:

$V_{cc}$  for Am27F512 +4.50V to +5.50V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*



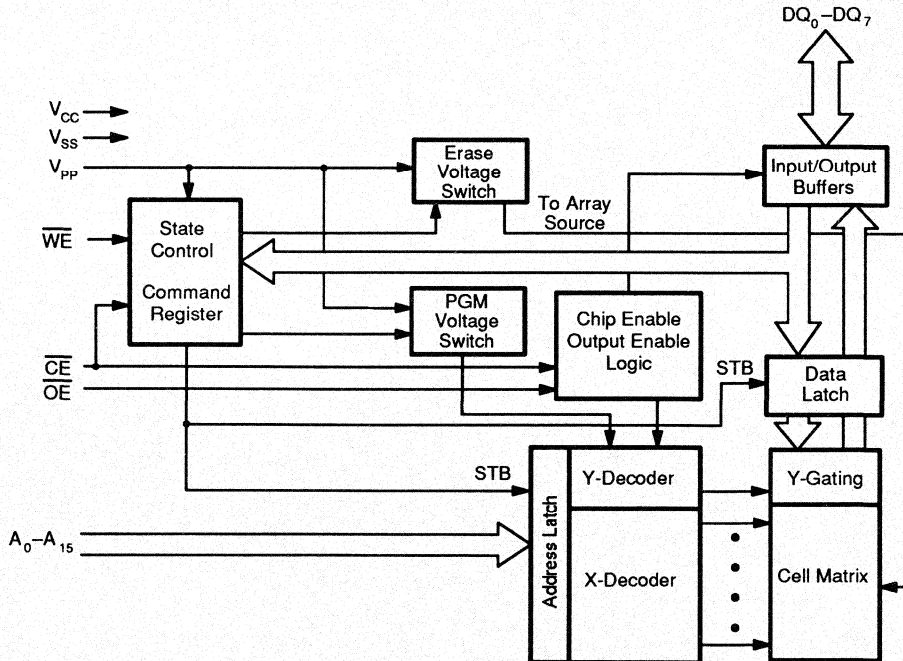
# Am28F512

65,536 x 8-Bit CMOS Flash E<sup>2</sup>PROM

## DISTINCTIVE CHARACTERISTICS

- **Flasherase™ Electrical Bulk Chip-Erase**
  - One Second Typical Chip-Erase
- **Compatible with JEDEC Standard Byte Wide 32-pin EEPROM Pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **Flashrite™ Programming**
  - 10μS Typical Byte-Program
  - Less than 1 Second Typical Chip Program
- **Program and Erase Voltage**
  - 12.0V ± 5% V<sub>pp</sub>
- **Advanced CMOS Technology**
  - EPROM Compatible Process
  - Extensive Manufacturing Experience
- **Low Power Consumption**
  - 30mA Maximum Active Current
  - 100 μA Maximum Standby Current
- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**
- **10,000 Program/Erase Cycles**
- **Provides On-Board Functionality for In-System-Write**
- **High Performance**
  - 100nS Maximum Access Time
- **On Board Address and Data Latches**
- **5V ±10% Single Power Supply**

## BLOCK DIAGRAM



11561-001A

## GENERAL DESCRIPTION

This device is an alternative to the full-featured EEPROM.

The 28F512 is targeted for high density in-system alterable code- or data-storage applications where full-feature EEPROM functionality is either not required or not cost effective. The Am28F512 CMOS Flash memory provides the highest performance and most cost-effective alternative for rewritable non-volatile memory. Flash memory adds electrical chip-erase and reprogramming to AMD's EPROM technology. The entire memory content may be Flash erased and reprogrammed in a PROM programmer or test socket, on board during subassembly test, in-system during final test or after sale. In-system electrical erasure increases the memory's flexibility, while providing time and cost savings.

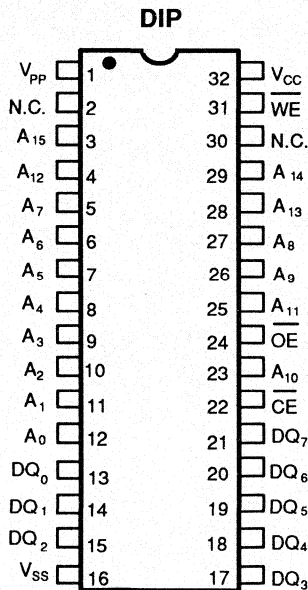
The device may be packaged in plastic DIP or PLCC and is ideal for use in auto-insertion manufacturing systems. The entire memory array may be erased and

reprogrammed on-board using AMD's Flasherase™ and Flashrite™ programming algorithms respectively.

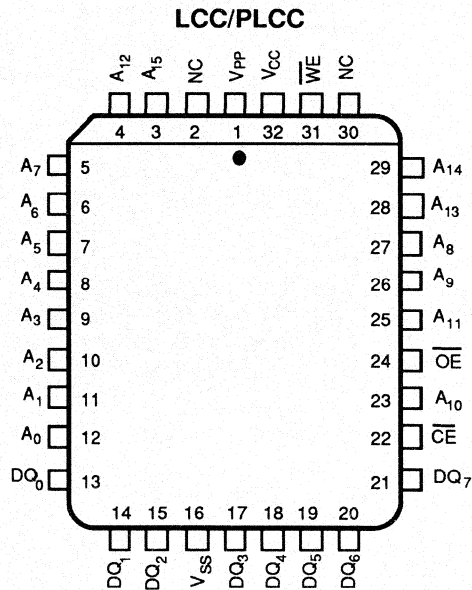
## Typical Applications

Flash memory is ideal for storing code or data-tables in embedded control applications where periodic updates or data down-loading is required. Code updates may occur throughout the entire life of a system. Beginning with prototyping, code updates may also be necessary during subassembly or even in after-sale service. Electrical chip erasure eliminates the 15 to 20 minute ultraviolet erase and streamlines code updates. In addition both DIP or PLCC Flash devices may be soldered to the circuit board during subassembly. Test codes may be programmed into the device on board. Prior to shipment final code is downloaded to the device. Thus, Flash technology eliminates unnecessary handling and less reliable socketed connections, saves board space, and adds increased manufacturing flexibility. After-sale code updates are performed locally via an edge-connector, or remotely over a serial communication link.

## CONNECTION DIAGRAMS

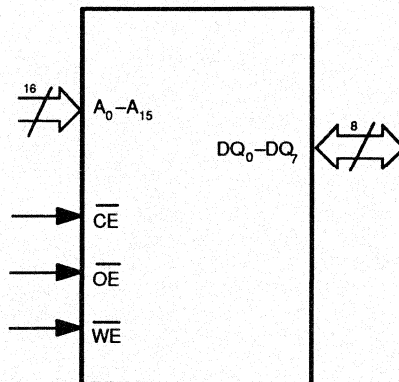


11561-002A



11561-003A

## LOGIC SYMBOL



11561-004A

## FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming gives flash memory the flexibility of EEPROM. A command register in the Flash device manages the electrical erasure and reprogramming. The command register architecture allows for fixed power supplies during erasure and programming and does not require high voltage on control pins.

### Read Mode

The Flash device functions as a read only memory when high voltage is not applied to the  $V_{pp}$  pin. In this mode the external memory control signals produce the standard EPROM read, standby, output disable, and Auto-select modes.

### Programming / Read Mode

High voltage on the  $V_{pp}$  pin enables the erase and programming functions of the device. The same EPROM read, standby, and output disable functions are available to the system when high voltage is applied to the  $V_{pp}$  pin. All functions associated with altering memory contents (erase, erase-verify, program, and program-verify) are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as

input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes. As with EEPROM devices, the 28F512 uses a dedicated WE control pin for command execution.

The command register is alterable only when high voltage is applied to  $V_{pp}$ . When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory.  $V_{pp}$  may be controlled with system hardware to provide secure write protect.

### Performance

AMD's Flash memories offer access times as fast as 100ns. This high performance allows operation of high-speed microprocessors and microcontrollers without wait-states. The Flash architecture supports separate chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) controls in order to eliminate bus contention.

## OPERATING RANGES

### Commercial (C) Devices

Case Temperature ( $T_c$ ) 0°C to +70°C

### Industrial (I) Devices

Case Temperature ( $T_c$ ) -40°C to +85°C

### Extended (E) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

### Military (M) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

*Operating ranges define those limits between which the functionality of the device is guaranteed.*



# Am27F010

131,072 x 8—Bit CMOS Windowless EPROM

## DISTINCTIVE CHARACTERISTICS

- **Flasherace™ Electrical Bulk Chip-Erase**
  - One Second Typical Chip-Erase
- **Compatible with JEDEC Standard Byte Wide EPROM Pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **Flashrite™ Programming**
  - 10μS Typical Byte-Program
  - Less than 2 Second Typical Chip Program
- **Advanced CMOS Technology**
  - EPROM Compatible Process
  - Extensive Manufacturing Experience
- **100 Program/Erase Cycles**
- **Low Power Consumption**
  - 30mA Maximum Active Current
  - 100μA Maximum Standby Current
- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**
- **Program and Erase Voltage**  
12.75V ± 0.25V V<sub>PP</sub>
- **High Performance**
  - 120nS Maximum Access Time
- **Allows for Auto-insertion**
- **5V ±10% Single Power Supply**

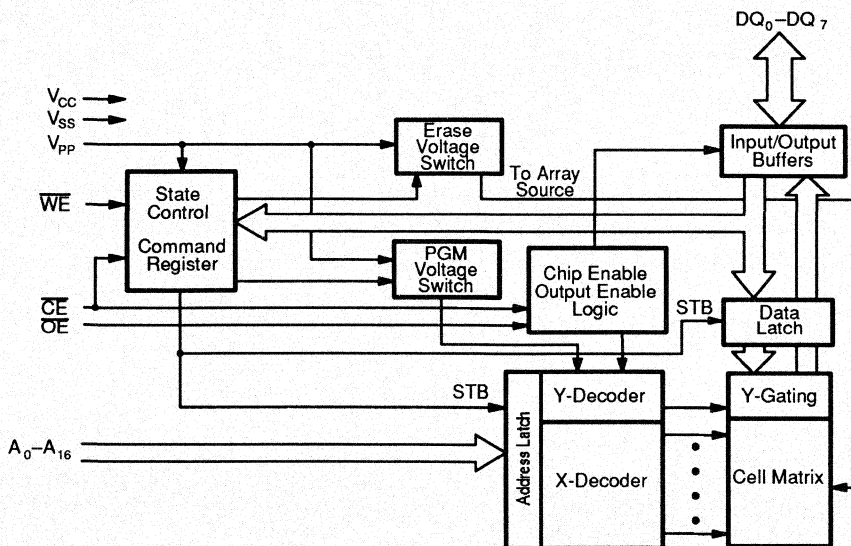
## GENERAL DESCRIPTION

The Am27F010 CMOS windowless EPROM provides the industry's highest performance and most cost-effective alternative for reprogrammable non-volatile memory. It is organized as 128K bytes of 8 bits each. The Am27F010 is pin compatible with the 32 pin byte-wide JEDEC 1MEG EPROM. The 27F010 is targeted for alterable code- or data-storage applications where ultraviolet erasure is impractical or time consuming. The windowless EPROM adds electrical Flash chip-erasure

and reprogramming to AMD's EPROM technology. The device may be packaged in plastic and is ideal for use in auto-insertion manufacturing systems. The entire memory content may be erased and reprogrammed using AMD's Flasherace™ and Flashrite™ programming algorithm respectively in a standard PROM programmer. Electrical erasure increases the memory's flexibility, while providing time savings over traditional UV erasing.

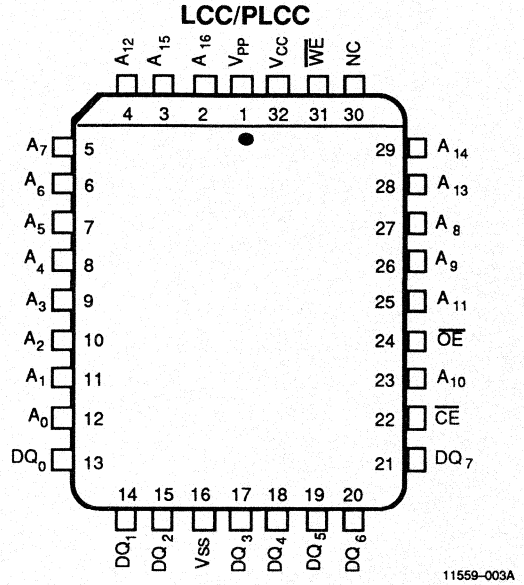
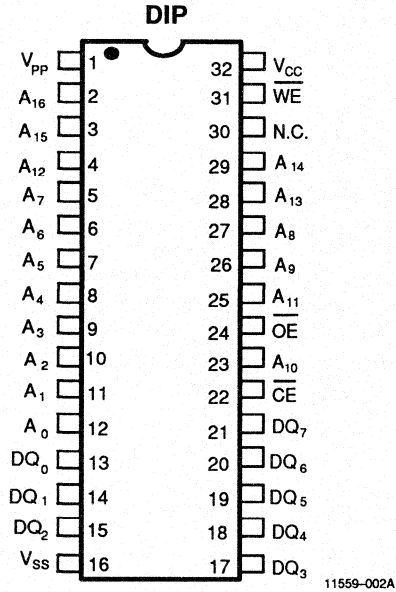
3

## BLOCK DIAGRAM

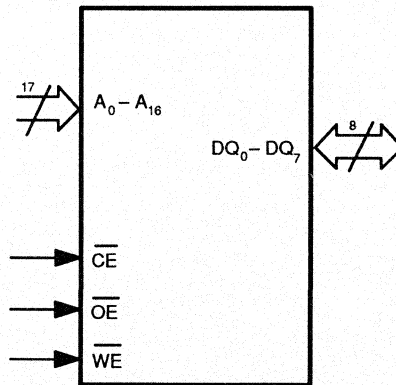


11559-001A

## CONNECTION DIAGRAMS



## LOGIC SYMBOL





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## FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming increases flash memory's flexibility over EPROM. Standard PROM programmers may be used for erasing and programming. A command register in the windowless EPROM manages the electrical erasure and reprogramming. The command register architecture allows for fixed power supplies during erasure and programming, does not require high voltage on control pins, and provides maximum EPROM compatibility.

### Read Mode

The windowless EPROM device functions as a read only memory when high voltage is not applied to the  $V_{pp}$  pin. In this mode the external memory control pins produce the standard EPROM read, standby, output disable, and Auto-select modes.

### Programming/Read Mode

High voltage on the  $V_{pp}$  pin enables erasure and programming of the device. The same EPROM read, standby, and output disable functions are available when high voltage is applied to the  $V_{pp}$  pin. All functions associated with altering memory contents (erase, erase-verify, program, and program-verify) are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes.

The command register is alterable only when high voltage is applied to  $V_{pp}$ . When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory.

### Performance

AMD's windowless EPROMs offer access times of 120ns which allows operation of high-speed microprocessors and microcontrollers without wait-states. The windowless EPROM architecture supports separate chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) controls in order to eliminate bus contention.

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## OPERATING RANGES

### Commercial (C) Devices

Case Temperature ( $T_c$ ) 0°C to +70°C

### Industrial (I) Devices

Case Temperature ( $T_c$ ) -40°C to +85°C

### Extended Commercial (E) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

### Military (M) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

*Operating ranges define those limits between which the functionality of the device is guaranteed.*



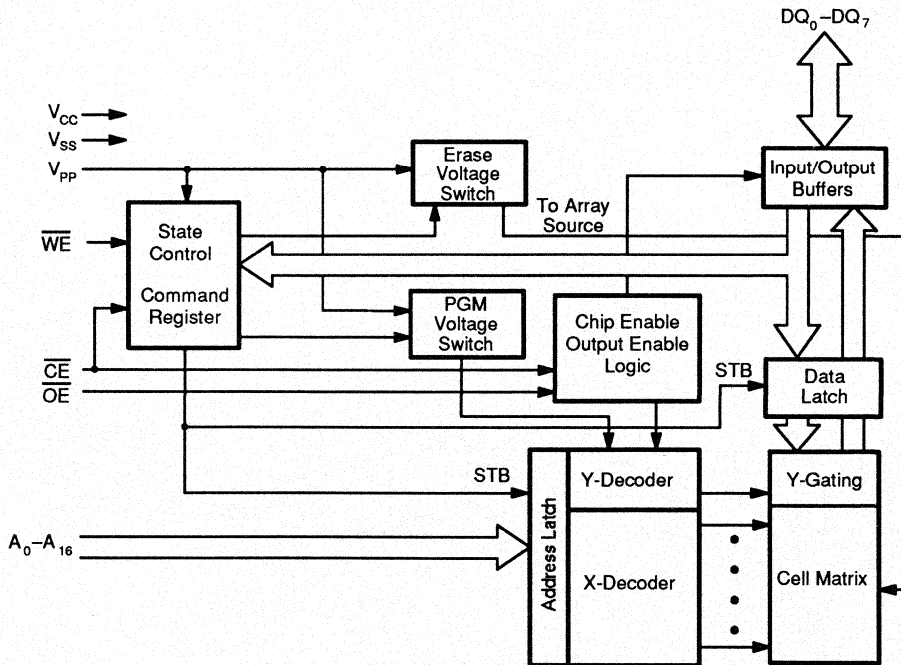
# Am28F010

131,072 x 8-Bit CMOS Flash E<sup>2</sup>PROM

## DISTINCTIVE CHARACTERISTICS

- **Flasherase™ Electrical Bulk Chip-Erase**
  - One Second Typical Chip-Erase
- **Compatible with JEDEC Standard Byte Wide 32-pin EEPROM Pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **Flashrite™ Programming**
  - 10μS Typical Byte-Program
  - Less than 2 Second Typical Chip Program
- **Program and Erase Voltage**
  - 12.0V ±5% V<sub>pp</sub>
- **Advanced CMOS Technology**
  - EPROM Compatible Process
  - Extensive Manufacturing Experience
- **Low Power Consumption**
  - 30mA Maximum Active Current
  - 100 μA Maximum Standby Current
- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**
- **10,000 Program/Erase Cycles**
- **Provides On-Board Functionality for In-System-Write**
- **High Performance**
  - 120nS Maximum Access Time
- **On Board Address and Data Latches**
- **5V±10% Single Power Supply**

## BLOCK DIAGRAM



11559-001A

## GENERAL DESCRIPTION

This device is an alternative to the full-featured EEPROM.

The 28F010 is targeted for in-system alterable code- or data-storage applications where full-feature EEPROM functionality is either not required or not cost effective. The Am28F010 CMOS Flash memory provides the highest performance and most cost-effective alternative for high density rewritable non-volatile memory. Flash memory adds electrical chip-erase and reprogramming to AMD's EPROM technology. The entire memory content may be Flash erased and reprogrammed in a PROM programmer or test socket, on board during sub-assembly test, in-system during final test or after sale. In-system electrical erasure increases the memory's flexibility, while providing time and cost savings.

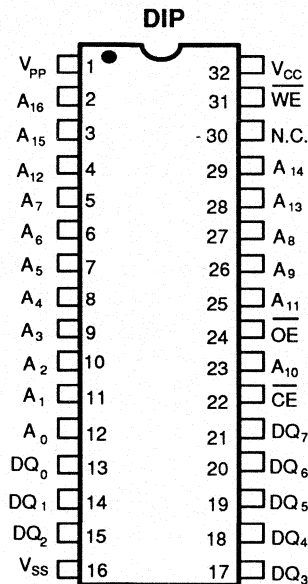
The device may be packaged in plastic DIP or PLCC and is ideal for use in auto-insertion manufacturing systems. The entire memory array may be erased and reprogrammed on-board using AMD's

Flasherase™ and Flashrite™ programming algorithms respectively.

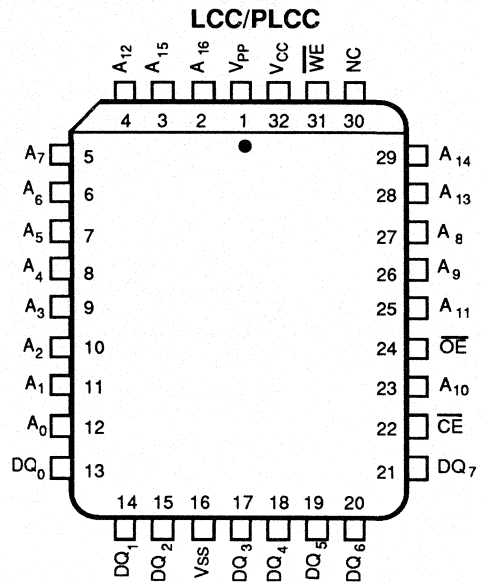
## Typical Applications

Flash memory is ideal for storing code or data-tables in embedded control applications where periodic updates or data down-loading is required. Code updates may occur throughout the entire life of a system. Beginning with prototyping, code updates may also be necessary during subassembly or even in after-sale service. Electrical chip erasure eliminates the 15 to 20 minute ultraviolet erase and streamlines code updates. In addition both DIP or PLCC Flash devices may be soldered to the circuit board during subassembly. Test codes may be programmed into the device on board. Prior to shipment final code is downloaded to the device. Thus, Flash technology eliminates unnecessary handling and less reliable socketed connections, saves board space, and adds increased manufacturing flexibility. After-sale code updates are performed locally via an edge-connector, or remotely over a serial communication link.

## CONNECTION DIAGRAMS

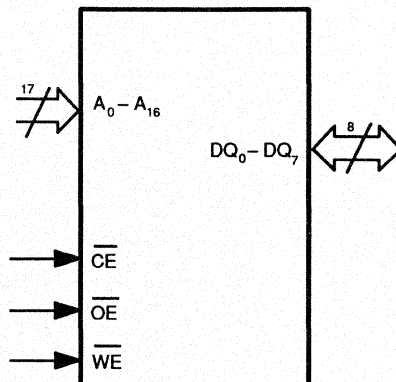


11559-002A



11559-003A

## LOGIC SYMBOL



11559-004A

## FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming gives flash memory the flexibility of EEPROM. A command register in the Flash device manages the electrical erase and reprogramming. The command register architecture allows for fixed power supplies during erasure and programming and does not require high voltage on control pins.

### Read Mode

The Flash device functions as a read only memory when high voltage is not applied to the  $V_{pp}$  pin. In this mode the external memory control signals produce the standard EPROM read, standby, output disable, and Auto-select modes.

### Programming/Read Mode

High voltage on the  $V_{pp}$  pin enables the erase and programming functions of the device. The same EPROM read, standby, and output disable functions are available to the system when high voltage is applied to the  $V_{pp}$  pin. All functions associated with altering memory contents (erase, erase-verify, program, and program-verify) are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as

input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes. As with EEPROM devices, the 28F010 uses a dedicated  $\overline{WE}$  control pin for command execution.

The command register is alterable only when high voltage is applied to  $V_{pp}$ . When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory.  $V_{pp}$  may be controlled with system hardware to provide secure write protect.

### Performance

AMD's Flash memories offer access times as fast as 120ns. This high performance allows operation of high-speed microprocessors and microcontrollers without wait-states. The Flash architecture supports separate chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) controls in order to eliminate bus contention.

## OPERATING RANGES

### Commercial (C) Devices

Case Temperature ( $T_c$ ) 0°C to +70°C

### Industrial (I) Devices

Case Temperature ( $T_c$ ) -40°C to +85°C

### Extended (E) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

### Military (M) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

*Operating ranges define those limits between which the functionality of the device is guaranteed.*



# Am27X64

8,192 x 8-Bit CMOS ExpressROM™ Device

## DISTINCTIVE CHARACTERISTICS

- OTP EPROM alternative:
  - Factory programmed
  - Fully tested and guaranteed to customer code
  - Low cost
- Mask ROM alternative:
  - Shorter leadtime
  - Lower volume per code
- Compatible with JEDEC-approved EPROM pinout
- High performance CMOS technology
  - Fast access time - 100 ns
  - Low power dissipation -
    - 100  $\mu$ A maximum standby current
- Available in plastic DIP and plastic leaded chip carrier

## GENERAL DESCRIPTION

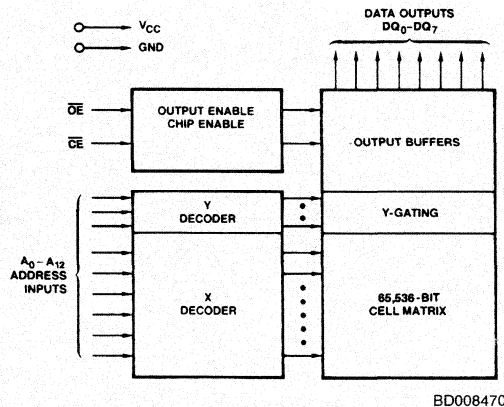
The Am27X64 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 8,192 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufactures a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors

without any WAIT states. The Am27X64 offers separate Output Enable (OE) and Chip Enable (CE) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

## BLOCK DIAGRAM



3

## PRODUCT SELECTOR GUIDE

Family Part No.	Am27X64					
Ordering Part No:						
$\pm 5\%$ $V_{CC}$ Tolerance	-105	-125	-155	-205	-255	-305
$\pm 10\%$ $V_{CC}$ Tolerance	-	-120	-150	-200	-250	-300
Max. Access Time (ns)	100	120	150	200	250	300
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	100	120	150	200	250	300
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	40	50	65	75	100	120



# Am27X128

16,384 x 8-Bit CMOS ExpressROM™ Device

## DISTINCTIVE CHARACTERISTICS

- OTP EPROM alternative:
  - Factory programmed
  - Fully tested and guaranteed to customer code
  - Low cost
- Mask ROM alternative:
  - Shorter leadtime
  - Lower volume per code
- Compatible with JEDEC-approved EPROM pinout
- High performance CMOS technology
  - Fast access time - 100 ns
  - Low power dissipation -
    - 100  $\mu$ A maximum standby current
- Available in plastic DIP and plastic leaded chip carrier

## GENERAL DESCRIPTION

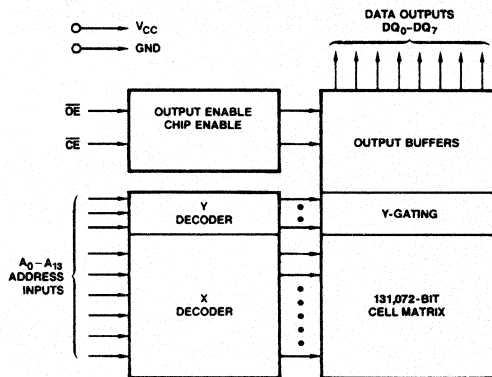
The Am27X128 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 16,384 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors

without any WAIT states. The Am27X128 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

## BLOCK DIAGRAM



BD008480

## PRODUCT SELECTOR GUIDE

Family Part No.	Am27X128					
Ordering Part No:						
$\pm 5\%$ $V_{CC}$ Tolerance	-105	-125	-155	-205	-255	-305
$\pm 10\%$ $V_{CC}$ Tolerance	-	-120	-150	-200	-250	-300
Max. Access Time (ns)	100	120	150	200	250	300
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	100	120	150	200	250	300
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	40	50	65	75	100	120



# Am27X256

32,768 x 8-Bit CMOS ExpressROM™ Device

## DISTINCTIVE CHARACTERISTICS

- OTP EPROM alternative:
  - Factory programmed
  - Fully tested and guaranteed to customer code
  - Low cost
- Mask ROM alternative:
  - Shorter leadtime
  - Lower volume per code
- Compatible with JEDEC-approved EPROM pinout
- High performance CMOS technology
  - Fast access time - 100 ns
  - Low power dissipation - 100  $\mu$ A maximum standby current
- Available in plastic DIP and plastic leaded chip carrier

## GENERAL DESCRIPTION

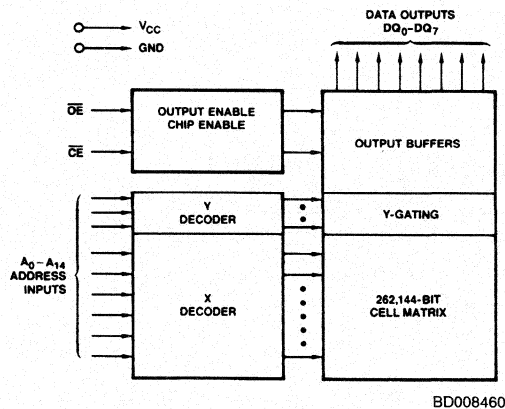
The Am27X256 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 32,768 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufactures a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors

without any WAIT states. The Am27X256 offers separate Output Enable (OE) and Chip Enable (CE) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

## BLOCK DIAGRAM



## PRODUCT SELECTOR GUIDE

Family Part No.	Am27X256						
Ordering Part No:							
±5% V <sub>CC</sub> Tolerance	-105	-125	-155	-175	-205	-255	-305
±10% V <sub>CC</sub> Tolerance	-	-120	-150	-170	-200	-250	-300
Max. Access Time (ns)	100	120	150	170	200	250	300
CE (E) Access (ns)	100	120	150	170	200	250	300
OE (G) Access (ns)	40	50	65	70	75	100	120



# Am27X512

65,536 x 8-Bit CMOS ExpressROM™ Device

## DISTINCTIVE CHARACTERISTICS

- OTP EPROM alternative:  
Factory programmed  
Fully tested and guaranteed to customer code  
Low cost
- Mask ROM alternative:  
Shorter leadtime  
Lower volume per code
- Compatible with JEDEC-approved EPROM pinout
- High performance CMOS technology  
Fast access time - 150 ns  
Low power dissipation -  
100  $\mu$ A maximum standby current
- Available in plastic DIP and plastic leaded chip carrier

## GENERAL DESCRIPTION

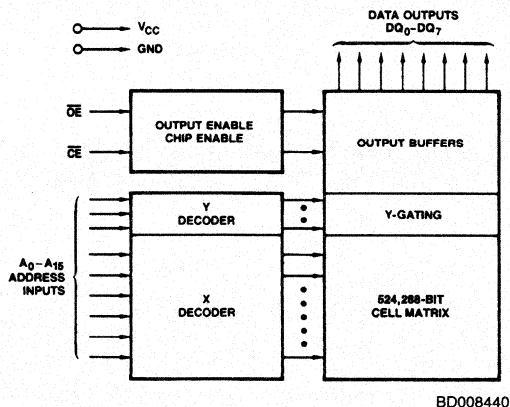
The Am27X512 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 65,536 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufactures a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Typically, any byte can be accessed in less than 150 ns, allowing operation with high-performance microprocessors

with reduced WAIT states. The Am27X512 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

## BLOCK DIAGRAM



## PRODUCT SELECTOR GUIDE

Family Part No.	Am27X512				
Ordering Part No:					
$\pm 5\%$ $V_{CC}$ Tolerance	-155	-175	-205	-255	-305
$\pm 10\%$ $V_{CC}$ Tolerance	-	-170	-200	-250	-300
Max. Access Time (ns)	150	170	200	250	300
$\overline{CE}$ (E) Access (ns)	150	170	200	250	300
$\overline{OE}$ (G) Access (ns)	50	50	75	100	100



# Am27X010

1 Megabit (131,072 x 8-Bit) CMOS ExpressROM™ Device



## DISTINCTIVE CHARACTERISTICS

- OTP EPROM alternative:  
Factory programmed  
Fully tested and guaranteed to customer code  
Low cost
- Mask ROM alternative:  
Shorter leadtime  
Lower volume per code
- Compatible with JEDEC-approved EPROM pinout
- High performance CMOS technology  
Fast access time - 170 ns  
Low power dissipation -  
100  $\mu$ A maximum standby current
- Available in plastic DIP and plastic leaded chip carrier

## GENERAL DESCRIPTION

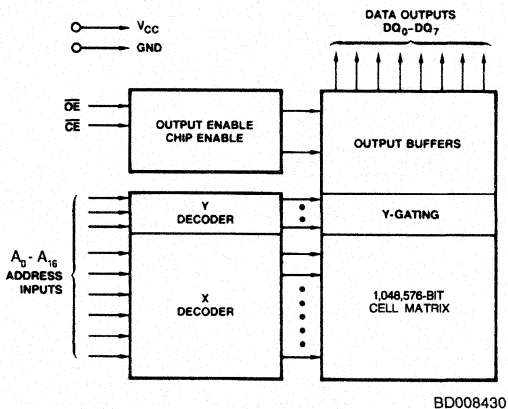
The Am27X010 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 131,072 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Typically, any byte can be accessed in less than 170 ns, allowing operation with high-performance microprocessors

with reduced WAIT states. The Am27X010 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

## BLOCK DIAGRAM



3

## PRODUCT SELECTOR GUIDE

Family Part No.	Am27X010			
Ordering Part No:				
±5% V <sub>CC</sub> Tolerance	-175	-205	-255	-305
±10% V <sub>CC</sub> Tolerance	-	-200	-250	-300
Max. Access Time (ns)	170	200	250	300
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	170	200	250	300
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	65	75	100	120



# Am27X1024

1 Megabit (65,536 x 16-Bit) CMOS ExpressROM™ Device

## DISTINCTIVE CHARACTERISTICS

- OTP EPROM alternative:
  - Factory programmed
  - Fully tested and guaranteed to customer code
  - Low cost
- Mask ROM alternative:
  - Shorter leadtime
  - Lower volume per code
- Compatible with JEDEC-approved EPROM pinout
- High performance CMOS technology
  - Fast access time - 170 ns
  - Low power dissipation - 100  $\mu$ A maximum standby current
- Available in plastic DIP and plastic leaded chip carrier

## GENERAL DESCRIPTION

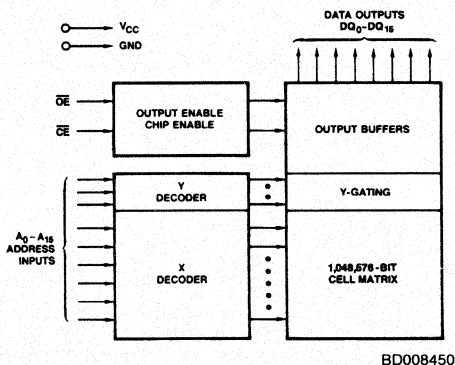
The Am27X1024 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 65,536 by 16 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufactures a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Typically, any byte can be accessed in less than 170 ns, allowing operation with high-performance microprocessors

with reduced WAIT states. The Am27X1024 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250  $\mu$ W in standby mode.

## BLOCK DIAGRAM

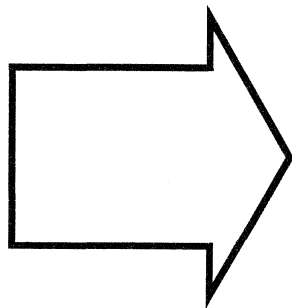


## PRODUCT SELECTOR GUIDE

Family Part No.	Am27X1024			
Ordering Part No:				
$\pm 5\%$ $V_{CC}$ Tolerance	-175	-205	-255	-305
$\pm 10\%$ $V_{CC}$ Tolerance	-	-200	-250	-300
Max. Access Time (ns)	170	200	250	300
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	170	200	250	300
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	65	75	100	120



Advanced  
Micro  
Devices



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# Am9122/Am91L22

256x4 Static RAM



## DISTINCTIVE CHARACTERISTICS

- High-performance replacement for 93422/93L422
- Fast access times — as low as 25 ns
- Low-power dissipation
  - Low power: 440 mW (Commercial)
  - 495 mW (Military)
- Single 5-volt power supply —  $\pm 10\%$  tolerance both Commercial and Military

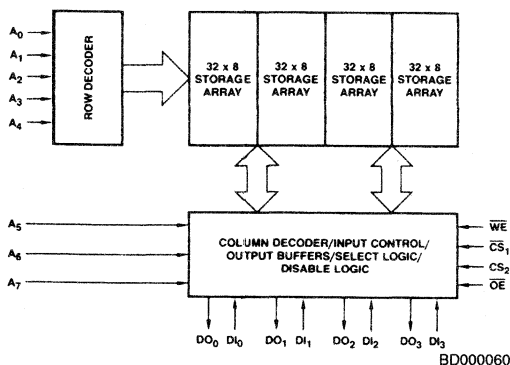
## GENERAL DESCRIPTION

The Am9122/Am91L22 Series is a MOS pin-for-pin and functional replacement for the 93422/93L422 bipolar memories. These devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 25 ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient

design of small memory systems and allows finer resolution of incremental memory depth.

The Am9122/91L22 employs an output enable and two chip enable inputs to give the user better data control. High noise immunity, high output drive (4 TTL loads) and TTL logic voltage levels allow easy conversion from bipolar to MOS. 10% power supply tolerances give better margins in the memory system.

## BLOCK DIAGRAM



## MODE SELECT TABLE

Inputs					Outputs	Mode
OE	CS <sub>1</sub>	CS <sub>2</sub>	WE	D <sub>0</sub> -D <sub>3</sub>		
X	H	X	X	X	Hi-Z	Not Selected
X	X	L	X	X	Hi-Z	Not Selected
L	L	H	H	X	O <sub>0</sub> -O <sub>3</sub>	Read Stored Data
X	L	H	L	L	Hi-Z	Write "0"
X	L	H	L	H	Hi-Z	Write "1"
H	L	H	H	X	Hi-Z	Output Disabled
H	L	H	L	L	Hi-Z	Write "0" (Output Disabled)
H	L	H	L	H	Hi-Z	Write "1" (Output Disabled)

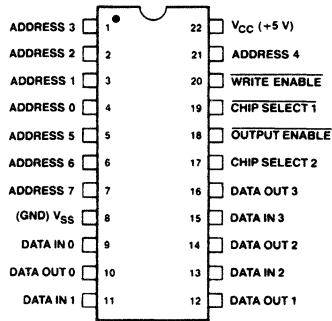
H = HIGH Voltage  
 L = LOW Voltage  
 X = Don't Care (HIGH or LOW)  
 Hi-Z = High Impedance

4

## PRODUCT SELECTOR GUIDE

Part Number	Am9122-25	Am9122-35	Am91L22-35	Am91L22-45
Maximum Access Time (ns)	25	35	35	45
Maximum Operating Current (mA)	0° to +70°C	120	120	80
	-55° to +125°C	N/A	135	N/A

**CONNECTION DIAGRAM**  
**Top View**  
**DIPs**

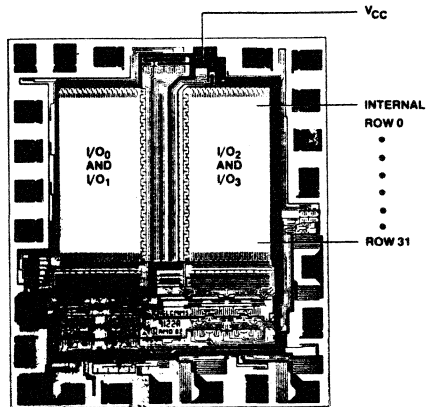


CD000111

Note: Pin 1 is marked for orientation.

**METALLIZATION AND PAD LAYOUT**

<b>Address Designators</b>	
<b>External</b>	<b>Internal</b>
A <sub>0</sub>	A <sub>0</sub>
A <sub>1</sub>	A <sub>1</sub>
A <sub>2</sub>	A <sub>2</sub>
A <sub>3</sub>	A <sub>3</sub>
A <sub>4</sub>	A <sub>4</sub>
A <sub>5</sub>	A <sub>5</sub>
A <sub>6</sub>	A <sub>6</sub>
A <sub>7</sub>	A <sub>7</sub>

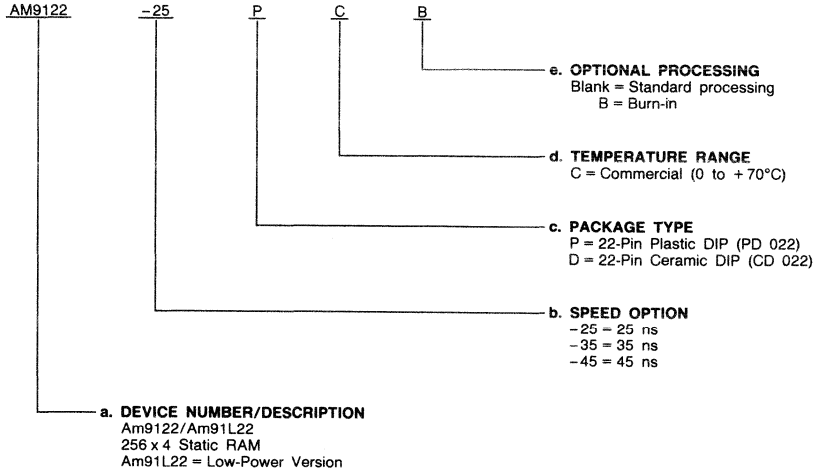


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM9122-25	DC, DCB, PC, PCB
AM91L22-35	
AM9122-35	
AM91L22-45	

#### Valid Combinations

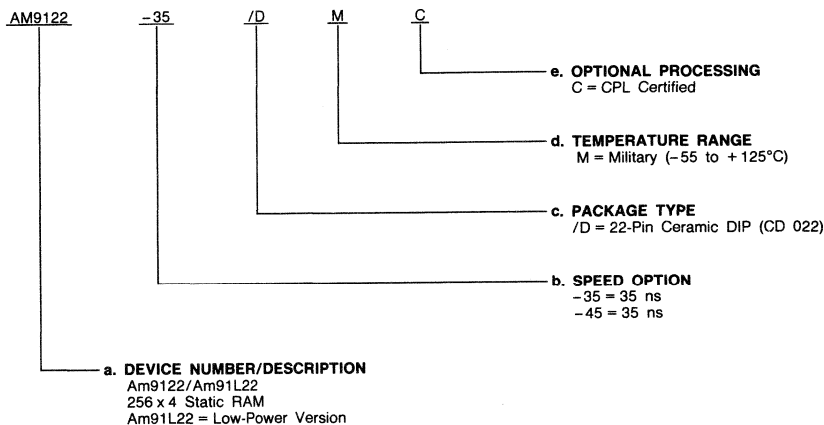
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of packages, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM9122-35	/DMC
AM91L22-45	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>7</sub> Address (Input)

The 8 address inputs select one of the 256 4-bit words in the RAM.

### $\overline{CS}_1$ Chip Select 1 (Input)

### CS<sub>2</sub> Chip Select 2 (Input)

$\overline{CS}_1$  is active LOW and CS<sub>2</sub> is active HIGH. The device can be accessed only when both Chip Selects are active. If either Chip Select is not active, the device is deselected and the outputs will be in a high-impedance state.

### $\overline{WE}$ Write Enable Input

$\overline{WE}$  controls read and write operations. When  $\overline{WE}$  is HIGH and  $\overline{OE}$  is LOW, data will be present at the data outputs. When  $\overline{WE}$  is LOW, data present on the data inputs will be

written into the selected memory location. The data outputs will be in a high-impedance state.

### $\overline{OE}$ Output Enable (Input)

$\overline{OE}$  controls the state of the data outputs in conjunction with Chip Select and  $\overline{WE}$ .

### DI<sub>0</sub> - DI<sub>3</sub> Data IN (Input)

Data inputs to the RAM.

### DO<sub>0</sub> - DO<sub>3</sub> Data Out (Output)

Data output from the RAM. The data output will be in a high-impedance state when either Chip Select is not active or  $\overline{OE}$  is HIGH or  $\overline{WE}$  is LOW.

### V<sub>CC</sub> Power Supply +5 Volts

### V<sub>SS</sub> Ground



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs .....	-0.5 V to +7.0 V
DC Input Voltage .....	-0.5 V to +7.0 V
Power Dissipation .....	1.0 W
DC Output Current .....	20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES (Note 2)

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +70°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V
Military (M) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for CPL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Am91L22-35 Am91L22-45			Am9122-25 Am9122-35			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min.	I <sub>OH</sub> = -5.2 mA	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min.	I <sub>OL</sub> = 8.0 mA			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.1		V <sub>CC</sub>	2.1		V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage			-2.5		0.8	-2.5		0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND		-10			-10			μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>				10			10	μA
V <sub>CD</sub>	Input Diode Clamp Voltage					Note 3			Note 3	V
I <sub>OFF</sub>	Output Current (Hi-Z)	V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub> Output Disabled	T <sub>A</sub> = Max.	-10		10	-10		10	μA
I <sub>OS</sub>	Output Short Circuit Current (Note 4)	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND	COM'L			-85			-85	mA
			MIL			-100			-100	
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA	T <sub>A</sub> = 0°C			80			120	mA
			T <sub>A</sub> = -55°C			90			135	
C <sub>IN</sub>	Input Capacitance V <sub>IN</sub> = 0 V	T <sub>A</sub> = 25°C, f = 1 MHz			3	5		3	5	pF
C <sub>OUT</sub>	Output Capacitance V <sub>OUT</sub> = 0 V	V <sub>CC</sub> = 4.5 V (Note 5)			5	8		5	8	

- Notes: 1. Absolute Maximum Rating are intended for user guidelines and are not tested.  
 2. For test and correlation purposes, ambient temperature is defined as the "instant-ON" case temperature.  
 3. The NMOS process does not provide a clamp diode. However, the Am9122/91L22 is insensitive to -3 V DC input levels and -5 V undershoot pulses of less than 10 ns (measured at 50% point).  
 4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.  
 5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.  
 6. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance as in A under Switching Test Circuits.  
 7. Transition is measured at 1.5 V on the input to V<sub>OH</sub> - 500 mV and V<sub>OL</sub> + 500 mV on the outputs using the load shown in B. C<sub>L</sub> = 5 pF.  
 8. t<sub>w</sub> measured at t<sub>wsa</sub> = Min.; t<sub>wsa</sub> measured at t<sub>w</sub> = Min.

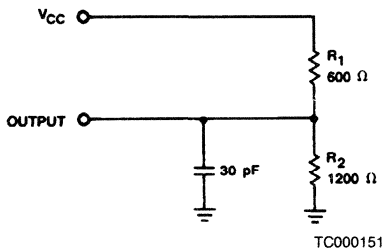
4

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for CPL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Notes 6, 7, 8)

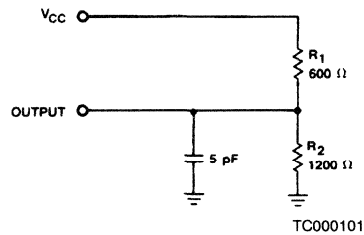
No.	Parameter Symbol	Parameter Description	Am9122-25		Am91L22-35 Am9122-35		Am91L22-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	tACS	Chip Select Time		15		25		30	ns
2	tzRCS	Chip Select to Hi-Z (Note 5 & 7)		20		30		30	ns
3	tAOS	Output Enable Time		15		25		30	ns
4	tzROS	Output Enable to Hi-Z (Note 5 & 7)		20		30		30	ns
5	tAA	Address Access Time		25		35		45	ns
6	tzWS	Write Disable to Hi-Z (Note 5 & 7)		20		30		35	ns
7	tWR	Write Recovery Time		20		25		40	ns
8	tW	Write Pulse Width (Note 8)	15		25		30		ns
9	tWSD	Data Setup Time Prior to Write	5		5		5		ns
10	tWHD	Data Hold Time After Write	5		5		5		ns
11	tWSA	Address Setup Time (Note 8)	5		5		10		ns
12	tWHA	Address Hold Time	5		5		5		ns
13	tWSCS	Chip Select Setup Time	5		5		5		ns
14	tWHCS	Chip Select Hold Time	5		5		5		ns

Notes: See notes following DC Characteristics table.

### SWITCHING TEST CIRCUITS

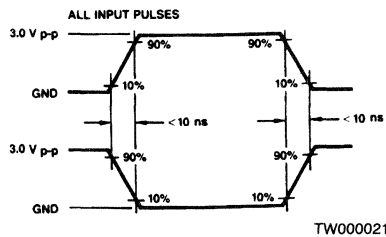


A



B

### SWITCHING TEST WAVEFORM

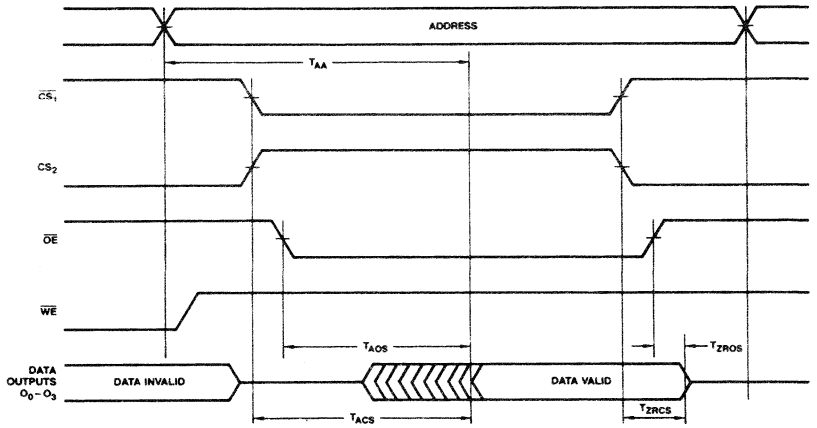


# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

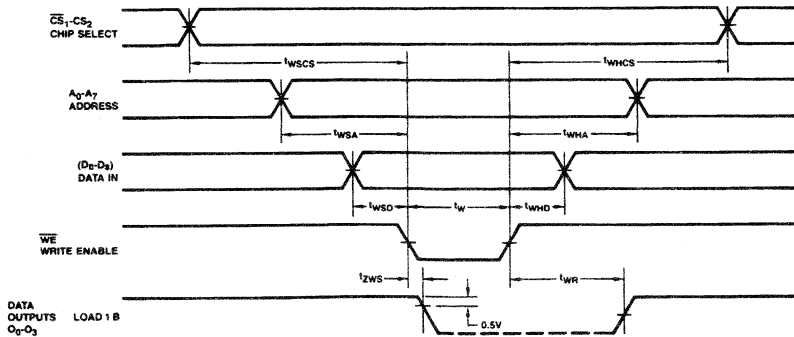
WAVEFORM	INPUTS	OUTPUTS
—	MUST BE STEADY	WILL BE STEADY
▨▨▨▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▧▧▧▧	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▩▩▩▩	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
▧▩▩▩	DOES NOT APPLY	CENTER LINE IS HIGH IMPLICANCE "OFF" STATE

KS000010



WF000660

**Read Mode**



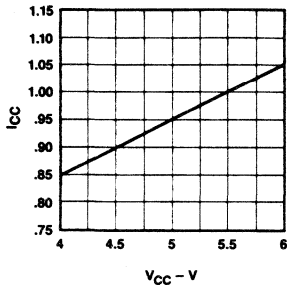
WF022050

**Write Mode**

(All above measurements implemented to 1.5 V unless otherwise stated.)  
 Note: Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst-case limits are not violated.

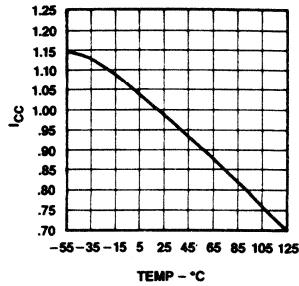
## TYPICAL PERFORMANCE CURVES

**Normalized  $I_{CC}$  versus Supply Voltage**



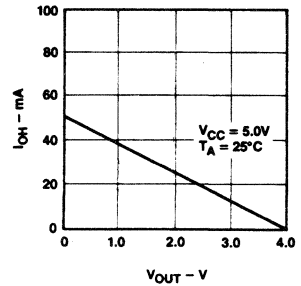
OP000120

**Normalized  $I_{CC}$  versus Ambient Temperature**



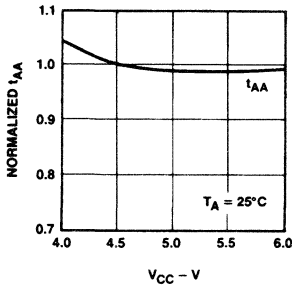
OP000130

**Output Source Current versus Output Voltage**



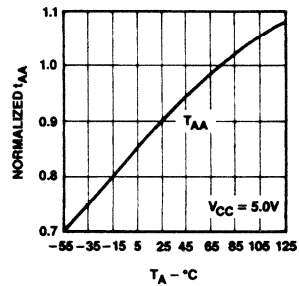
OP000140

**Normalized Access Time versus Supply Voltage**



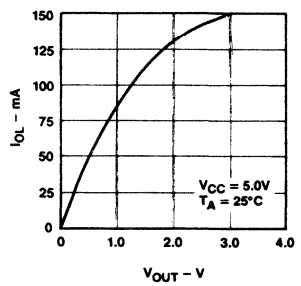
OP000150

**Normalized Access Time versus Ambient Temperature**



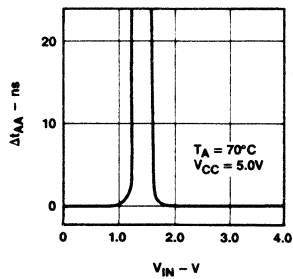
OP000160

**Output Sink Current versus Output Voltage**



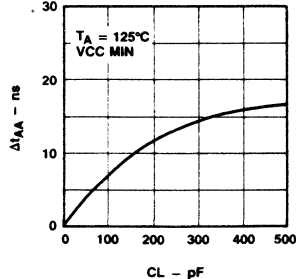
OP000170

**Access Time Change versus Input Voltage**



OP000180

**Access Time Change versus Output Loading**



OP000190

## DISTINCTIVE CHARACTERISTICS

- Fully static storage and interface circuitry
- Automatic power-down when deselected
- Low power dissipation
  - Am21L41; 220 mW active, 27.5 mW power down
- High output drive
- TTL compatible interface levels
- No power-on current surge

## GENERAL DESCRIPTION

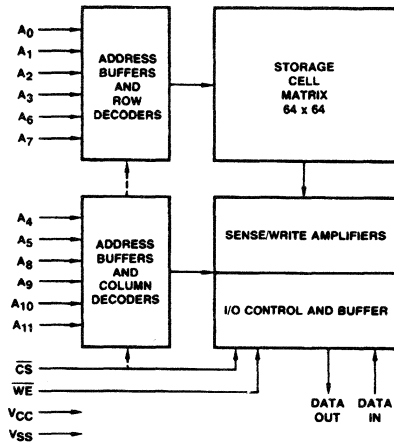
The Am21L41 is a high-performance, 4096-bit, static, read/write, random-access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard Schottky TTL loads or up to six standard TTL loads.

Only a single +5-volt power supply is required. When deselected ( $\overline{CS} \geq V_{IH}$ ), the Am21L41 automatically enters

a power-down mode which reduces power dissipation by as much as 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a three-state signal allowing wired-OR operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

## BLOCK DIAGRAM

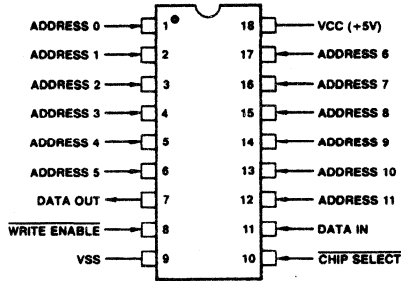


BD000111

## PRODUCT SELECTOR GUIDE

Part Number	Am21L41-12	Am21L41-15	Am21L41-20	Am21L41-25
Maximum Access Time (ns)	120	150	200	250
Maximum Active Current (mA)	55	40	40	40
Maximum Standby Current (mA)	10	5	5	5

## CONNECTION DIAGRAM Top View

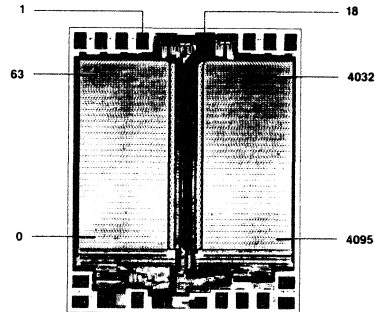


CD000161

Note: Pin 1 is marked for orientation.

## METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A <sub>0</sub>	A <sub>2</sub>
A <sub>1</sub>	A <sub>5</sub>
A <sub>2</sub>	A <sub>4</sub>
A <sub>3</sub>	A <sub>3</sub>
A <sub>4</sub>	A <sub>8</sub>
A <sub>5</sub>	A <sub>7</sub>
A <sub>6</sub>	A <sub>1</sub>
A <sub>7</sub>	A <sub>0</sub>
A <sub>8</sub>	A <sub>11</sub>
A <sub>9</sub>	A <sub>9</sub>
A <sub>10</sub>	A <sub>10</sub>
A <sub>11</sub>	A <sub>6</sub>



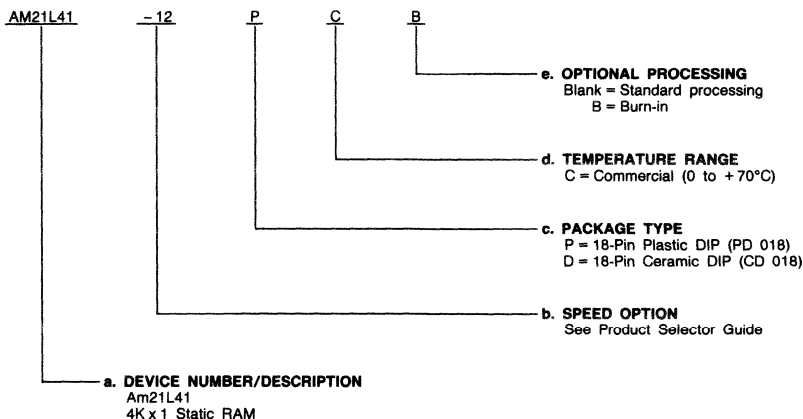
Die Size: 0.130" x 0.106"

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM21L41-12	PC, PCB, DC, DCB
AM21L41-15	
AM21L41-20	
AM21L41-25	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

4

## PIN DESCRIPTION

#### **A<sub>0</sub> - A<sub>11</sub> Address (Inputs)**

The address input lines select memory location from which to read or write.

#### **CS Chip Select (Input, Active LOW)**

The Chip Select line selects the memory device for active operation.

#### **WE Write Enable (Input, Active LOW)**

When both CS and WE are LOW, data on the input lines is written to the location presented on the address input lines.

#### **D<sub>IN</sub> Data In (Input)**

This pin is used to enter data during write operations.

#### **D<sub>OUT</sub> Data Out (Output, Three-State)**

The content of the selected memory location is presented on the Data Output line during read operations (CS LOW, WE HIGH). The line goes three-state during write operations.

#### **V<sub>CC</sub> Power Supply**

#### **V<sub>SS</sub> Ground**

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .....	- 65 to +150°C
Ambient Temperature with Power Applied .....	0 to +70°C
Supply Voltage .....	-0.5 V to +7.0 V
All Signal Voltage with Respect to Ground.....	- 1.5 V to +7.0 V
Power Dissipation .....	1.2 W
DC Output Current.....	20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES (Note 2)

Commercial (C) Devices	
Temperature (T <sub>A</sub> ) .....	0 to +70°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating ranges unless otherwise specified

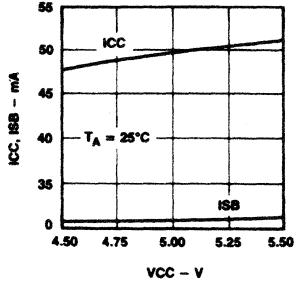
Parameter Symbol	Parameter Description	Test Conditions		Am21L41-12		Am21L41-15, Am21L41-20, Am21L41-25		Units
				Min.	Max.	Min.	Max.	
I <sub>OH</sub>	Output HIGH Current	V <sub>OH</sub> = 2.4 V	V <sub>CC</sub> = 4.5 V	-4		-4		mA
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4 V	T <sub>A</sub> = 70°C	8		8		mA
V <sub>IH</sub>	Input HIGH Voltage			2.0	6.0	2.0	6.0	V
V <sub>IL</sub>	Input LOW Voltage			-2.5	0.8	-2.5	0.8	V
I <sub>Ix</sub>	Input Load Current	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>			10		10	μA
I <sub>OZ</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled	T <sub>A</sub> = 70°C	-10	10	-10	10	μA
I <sub>OS</sub>	Output Short-Circuit Current	V <sub>SS</sub> ≤ V <sub>O</sub> ≤ V <sub>CC</sub> (Note 3)	0 to +70°C	-120	120	-120	120	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	Max. V <sub>CC</sub> , $\overline{CS} \leq V_{IL}$	T <sub>A</sub> = 0°C		55		40	mA
I <sub>SB</sub>	Automatic $\overline{CS}$ Power Down Current	Max. V <sub>CC</sub> , ( $\overline{CS} \geq V_{IH}$ ) (Note 5)			10		5.0	mA
C <sub>I</sub>	Input Capacitance (Note 13)	Test Frequency = 1.0 MHz T <sub>A</sub> = 25°C, All pins at 0 V			5.0		5.0	pF
C <sub>O</sub>	Output Capacitance (Note 13)				6.0		6.0	

- Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
  2. For test and correlation purpose, operating temperature is defined as the "instant-ON" case temperature.
  3. Short-circuit test duration should not exceed 30 seconds. Actual testing is performed for only 5 ms.
  4. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.5 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and C<sub>L</sub> = 30 pF load capacitance (reference A. under Switching Test Circuit.).
  5. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
  6. A pull-up resistor to V<sub>CC</sub> on the  $\overline{CS}$  input is required to keep the device deselected during V<sub>CC</sub> power up, otherwise I<sub>SB</sub> will exceed values given.
  7. Chip deselected greater than 55 ns prior to selection.
  8. Chip deselected less than 55 ns prior to selection.
  9. Transition is measured at V<sub>OH</sub> - 500 mV and V<sub>OL</sub> + 500 mV levels on the output from 1.5 V level on the input with load shown in Figure A using C<sub>L</sub> = 5 pF (under switching test circuit).
  10.  $\overline{WE}$  is HIGH for read cycle.
  11. Device is continuously selected,  $\overline{CS} = V_{IL}$ .
  12. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
  13. These parameters are not 100% tested, but are evaluated at initial characterization and at anytime the design is modified where capacitance may be affected.



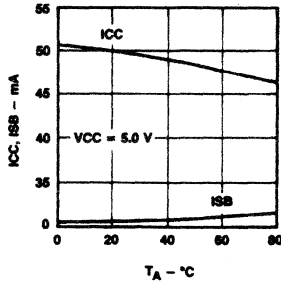
# TYPICAL DC and AC CHARACTERISTICS

Supply Current  
Versus Supply Voltage



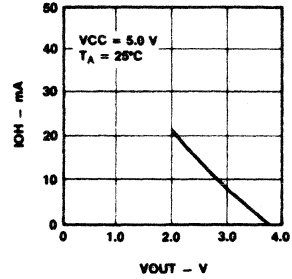
OP000820

Supply Current  
Versus Ambient Temperature



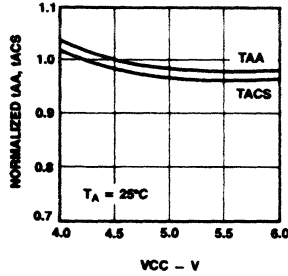
OP000831

Output Source Current  
Versus Output Voltage



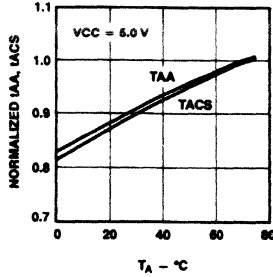
OP000841

Normalized Access Time  
Versus Supply Voltage



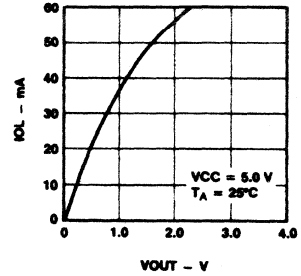
OP000760

Normalized Access Time  
Versus Ambient Temperature



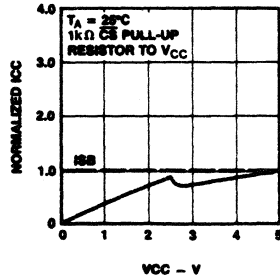
OP000851

Output Sink Current  
Versus Output Voltage



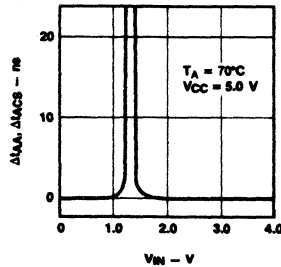
OP000861

Typical Power-On Current  
Versus Power Supply



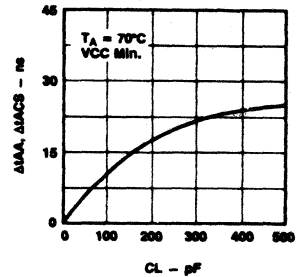
OP000871

Access Time Change  
Versus Input Voltage



OP000801

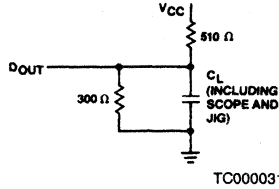
Access Time Change  
Versus Output Loading



OP000881



## SWITCHING TEST CIRCUIT



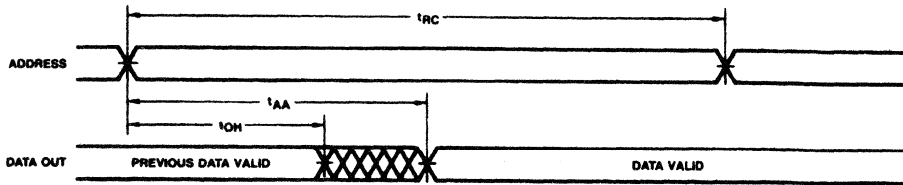
### A. Output Load

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (See Notes 4-12)

No.	Parameter Symbol	Parameter Description	Am21L41-12		Am21L41-15		Am21L41-20		Am21L41-25		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>											
1	$t_{RC}$	Address Valid to Address Do Not Care Time (Read Cycle Time)	120		150		200		250		ns
2	$t_{AA}$	Address Valid to Data Out Valid Delay (Address Access Time)		120		150		200		250	ns
3	$t_{ASC1}$	Chip Select LOW to Data Out Valid		120		150		200		250	ns
4	$t_{ASC2}$	Chip Select LOW to Data Out On (Note 9, 13)	10		10		10		10		ns
5	$t_{HZ}$	Chip Select HIGH to Data Out Off (Note 9, 13)	0	60	0	60	0	60	0	60	ns
6	$t_{OH}$	Output hold after address change	10		10		10		10		ns
7	$t_{PD}$	Chip Select HIGH to Power LOW Delay (Note 13)		60		60		60		60	ns
8	$t_{PU}$	Chip Select LOW to Power HIGH Delay (Note 13)	0		0		0		0		ns
<b>Write Cycle</b>											
10	$t_{WC}$	Address Valid to Address Do Not Care Time (Write Cycle Time)	120		150		200		250		ns
11	$t_{WP}$	Write Enable LOW to Write Enable HIGH Time (Note 5)	60		60		60		75		ns
12	$t_{WR}$	Write Enable HIGH to Address Do Not Care Time	10		15		20		20		ns
13	$t_{WZ}$	Write Enable LOW to Data Out Off Delay (Notes 9, 13)	0	70	0	80	0	80	0	80	ns
14	$t_{DW}$	Data in Valid to Write Enable HIGH Time	50		60		60		75		ns
15	$t_{DH}$	Write Enable HIGH to Data In Do Not Care Time	10		10		10		10		ns
16	$t_{AS}$	Address Valid to Write Enable LOW Time	0		0		0		0		ns
17	$t_{CW}$	Chip Select LOW to Write Enable HIGH Time (Note 5)	110		135		180		230		ns
18	$t_{OW}$	Write Enable HIGH to Output Turn On (Notes 9, 13)	0		0		0		0		ns
19	$t_{AW}$	Address Valid to End of Write	110		135		180		230		ns

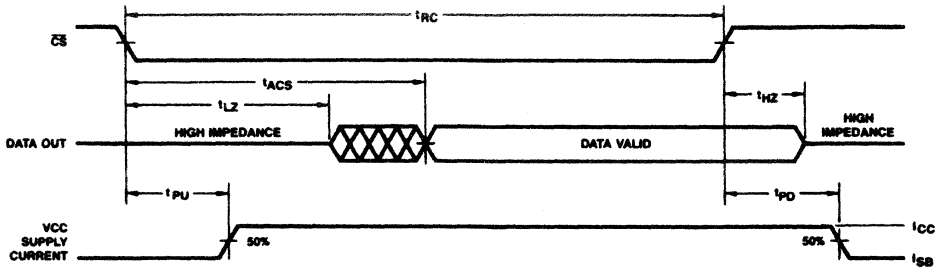
Notes: See notes following DC Characteristics table.

**SWITCHING WAVEFORMS (Cont'd.)**



WF000231

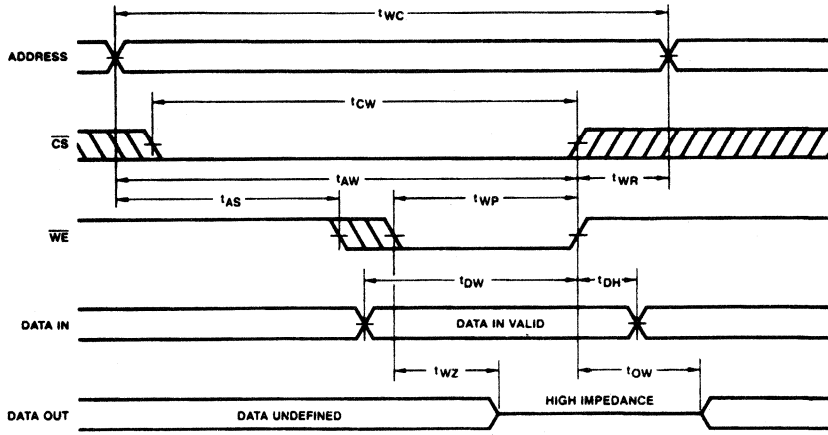
**Read Cycle No. 1 (Notes 10 & 11)**



WF000241

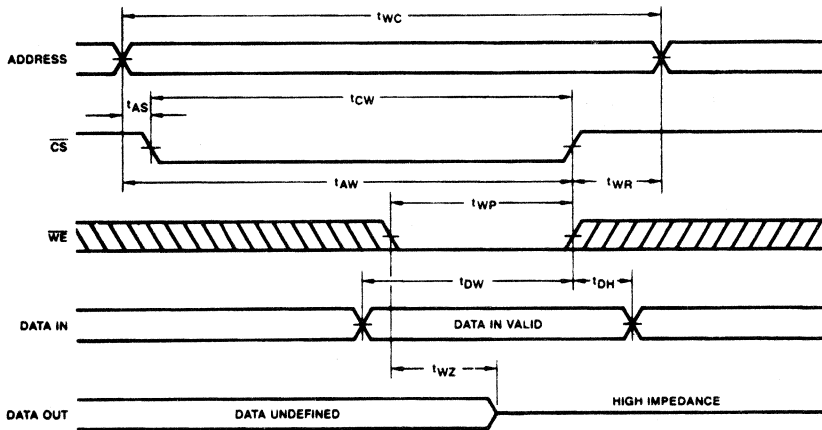
**Read Cycle No. 2 (Notes 10 & 12)**

## SWITCHING WAVEFORMS



WF000211

**Write Cycle No. 1 ( $\overline{WE}$  Controlled)**



WF000221

**Write Cycle No. 2 ( $\overline{CS}$  Controlled)**

Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

# Am9044/AM90L44

4096x1 Static RAM



## DISTINCTIVE CHARACTERISTICS

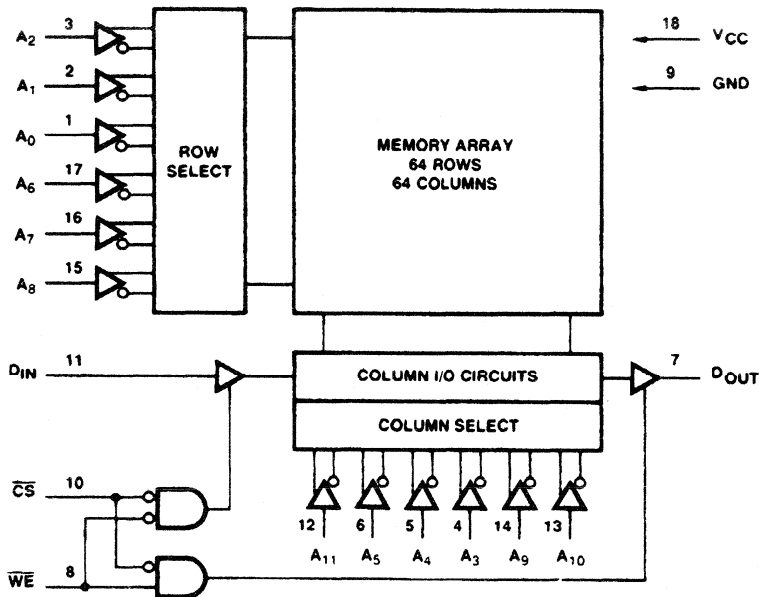
- Low operating and standby power
- Access times down to 200 ns
- Am9044 is a direct plug-in replacement for 4044
- High output drive — 4.0 mA sink current @ 0.4 V
- TTL identical interface logic levels

## GENERAL DESCRIPTION

The Am9044/Am90L44 Series are high-performance, static, N-Channel, read/write, random-access memories organized as 4096 x 1. Operation is from a single 5 V supply, and all input/output levels are identical to standard TTL specifications. A Low-power version is available with power savings of about 30%.

Data readout is not destructive and the same polarity as data input.  $\overline{CS}$  provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0 mA Am9044 provide increased short-circuit current for improved drive.

## BLOCK DIAGRAM



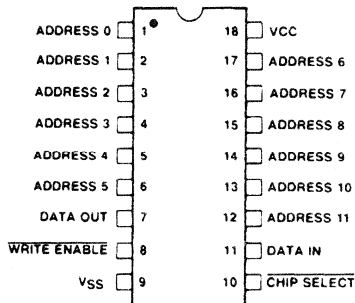
BD000091

Publication # Rev. Amendment  
03254 E /0  
Issue Date: January 1989

## PRODUCT SELECTOR GUIDE

Part Number			Am9044/Am90L44			
Speed Indicator			B	C	D	E
Maximum Access Time (ns)			450	300	250	200
0 to +70°C	I <sub>CC</sub> (mA)	Standard	70	70	70	70
		Low-Power	50	50	70	-

### CONNECTION DIAGRAM Top View DIPs

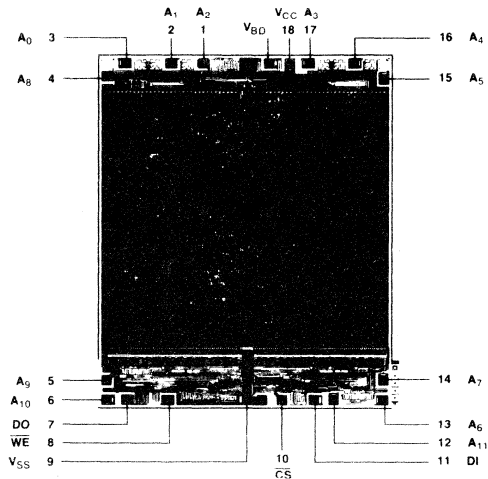


CD000142

Note: Pin 1 is marked for orientation.

### METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A <sub>0</sub>	A <sub>2</sub>
A <sub>1</sub>	A <sub>1</sub>
A <sub>2</sub>	A <sub>0</sub>
A <sub>3</sub>	A <sub>8</sub>
A <sub>4</sub>	A <sub>9</sub>
A <sub>5</sub>	A <sub>10</sub>
A <sub>6</sub>	A <sub>3</sub>
A <sub>7</sub>	A <sub>4</sub>
A <sub>8</sub>	A <sub>5</sub>
A <sub>9</sub>	A <sub>7</sub>
A <sub>10</sub>	A <sub>6</sub>
A <sub>11</sub>	A <sub>11</sub>



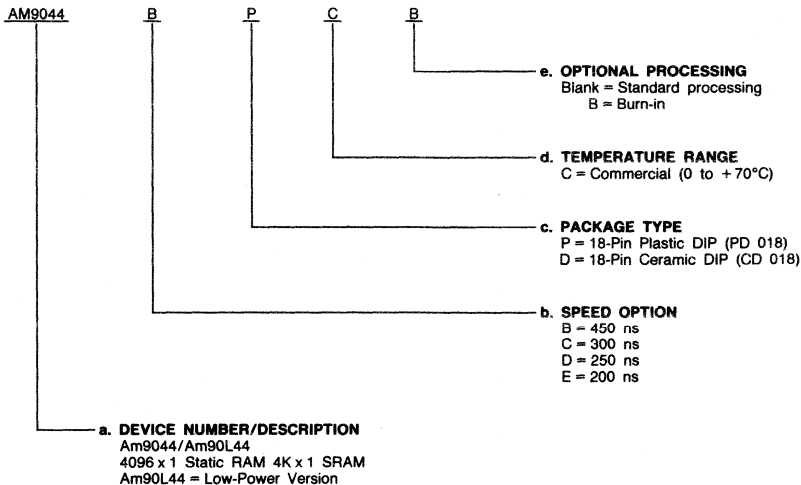
Die Size 0.137" x 0.167"

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- e. Temperature Range
- e. Optional Processing



Valid Combinations	
AM9044B	PC, PCB, DC, DCB
AM90L44B	
AM9044C	
AM90L44C	
AM9044D	
AM90L44D	
AM9044E	
AM90L44E	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## PIN DESCRIPTION

### **A<sub>0</sub> - A<sub>11</sub> Address Inputs (Inputs)**

The address input lines select the memory location from which to read or write.

### **CS Chip Select (Input, Active LOW)**

The CS line selects the memory device for active operation.

### **WE Write Enable (Input, Active LOW)**

When both CS and WE are LOW, data on the input lines is written to the location presented on the address input lines.

### **D<sub>IN</sub> Data In (Input)**

This pin is used to enter data during write operations.

### **D<sub>OUT</sub> Data Out (Output, Three-State)**

The content of the selected memory location is presented on the Data Output line during read operations (CS LOW, WE HIGH). The line goes three-state during write operations.

### **V<sub>CC</sub> Power Supply**

### **V<sub>SS</sub> Ground**

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	0 to 70°C
Supply Voltage .....	-0.5 V to +7.0 V
All Signal Voltage with Respect to Ground .....	-0.5 V to +7.0 V
Power Dissipation .....	1.0 W
DC Output Current .....	10 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGES (Note 2)

Commercial (C) Devices Ambient Temperature ( $T_A$ ) .....	0 to +70°C
Supply Voltage ( $V_{CC}$ ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
$I_{OH}$	Output HIGH Current	$V_{OH} = 2.4\text{ V}$ $V_{CC} = 4.5\text{ V}$	$T_A = 70^\circ\text{C}$	-1.0		mA
$I_{OL}$	Output LOW Current	$V_{OL} = 0.4\text{ V}$	$T_A = 70^\circ\text{C}$	4.0		mA
$V_{IH}$	Input HIGH Voltage			2.0	$V_{CC}$	V
$V_{IL}$	Input LOW Voltage			-0.5	0.8	V
$I_{IX}$	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$			10	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$0.4\text{ V} \leq V_O \leq V_{CC}$ , Output Disabled	$T_A = +70^\circ\text{C}$	-50	50	$\mu\text{A}$
$I_{CC}$	Operating Supply Current	$V_{CC} = \text{Max.}$ $\overline{CS} \leq V_{IL}$	$T_A = 0^\circ\text{C}$		70	mA
					50	
$C_I$	Input Capacitance (Note 6)	Test Frequency = 1.0 MHz			7.0	pF
$C_O$	Output Capacitance (Note 6)	$T_A = 25^\circ\text{C}$ , All pins at 0 V			7.0	

- Notes: 1. Absolute Maximum Ratings are intended for user guidelines and are not tested.  
2. For test and correlation purposes, ambient temperature is defined as the "instant-on" case temperature.  
3. Test conditions assume signal transition time of 10 ns or less, timing reference levels of 1.5 V, and output loading of the specified  $I_{OL}/I_{OH}$  plus 100 pF or 5 pF for  $T_{CX}$ ,  $T_{OTD}$ ,  $T_{OTW}$  and  $T_{WO}$ .  
4. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.  
5. The specified address access time will be valid only when  $\overline{CS}$  is LOW soon enough for  $t_{CO}$  to elapse.  
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.  
7. Transition is measured from 1.5 V on the input to ( $V_{OH} - 500\text{ mV}$ ) and ( $V_{OL} + 500\text{ mV}$ ) on the output using  $C_L = 5\text{ pF}$ .



**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Notes 3 – 6)

No.	Parameter Symbol	Parameter Description	B Devices		C Devices		D Devices		E Devices		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>											
1	t <sub>RC</sub>	Address Valid to Address Do Not Care Time (Read Cycle Time)	450		300		250		200		
2	t <sub>A</sub>	Address Valid to Data Out Valid Delay (Address Access Time)		450		300		250		200	
3	t <sub>CO</sub>	Chip Select LOW to Data Out Valid (Note 5)		100		100		70		70	
4	t <sub>CX</sub>	Chip Select LOW to Data Out On (Note 6, 7)	10		10		10		10		
5	t <sub>OTD</sub>	Chip Select HIGH to Data Out Off (Note 6, 7)		100		80		60		60	
6	t <sub>OHA</sub>	Output hold time after address change	20		20		20		20		
<b>WRITE CYCLE</b>											
7	t <sub>WC</sub>	Address Valid to Address Do Not Care Time (Write Cycle Time)	450		300		250		200		
8	t <sub>W</sub>	Write Enable LOW to Write Enable HIGH Time (Note 4)	200		150		100		100		
9	t <sub>WR</sub>	Write Enable HIGH to Address Do Not Care Time	0		0		0		0		
10	t <sub>OTW</sub>	Write Enable LOW to Data Out Off Delay (Note 6, 7)		100		80		60		60	
11	t <sub>DW</sub>	Data In Valid to Write Enable HIGH Time	200		150		100		100		
12	t <sub>DH</sub>	Write Enable HIGH to Data In Do Not Care Time	0		0		0		0		ns
13	t <sub>AW</sub>	Address Valid to Write Enable LOW Time	0		0		0		0		
14	t <sub>CW</sub>	Chip Select LOW to Write Enable HIGH Time (Note 4)	200		150		100		100		
15	t <sub>WO</sub>	Write Enable HIGH To Output Turn On (Note 6, 7)	0	100	0	100	0	70	0	70	

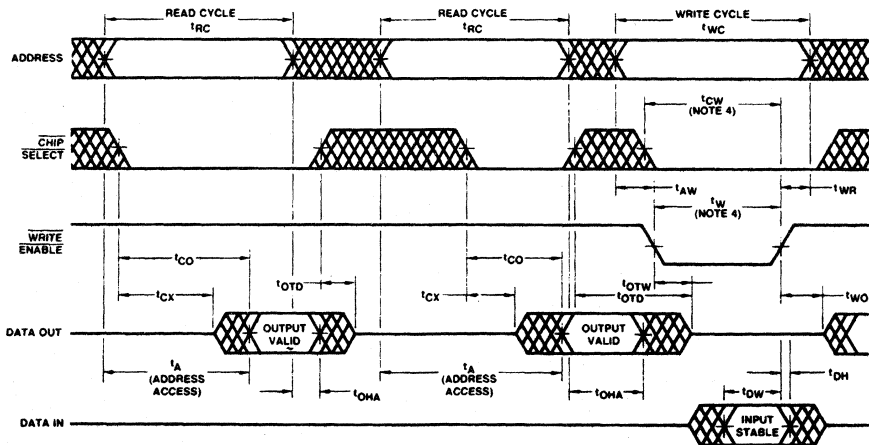
Notes: See notes following DC Characteristics table.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

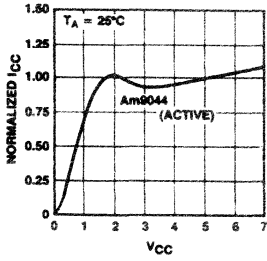


WF000191

Notes: See notes following DC Characteristics table.

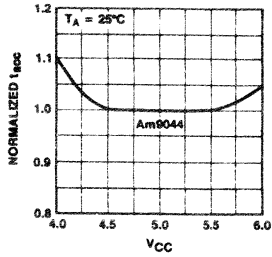
## TYPICAL PERFORMANCE CURVES

Normalized Supply Current Versus Supply Voltage



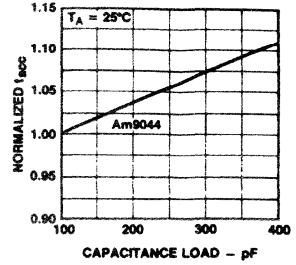
OP000892

Normalized Access Time Versus Supply Voltage



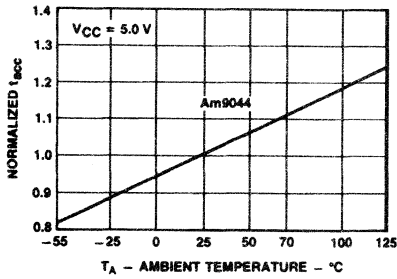
OP000902

Normalized Access Time Versus Output Loading



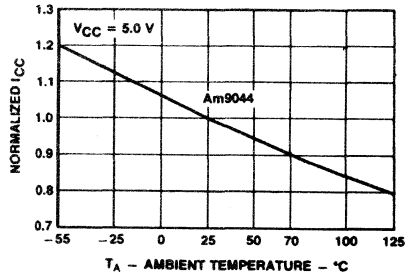
OP000912

Normalized Access Time Versus Ambient Temperature



OP000922

Normalized Supply Current Versus Ambient Temperature



OP000932



# Am9114/Am91L14

1024x4 Static RAM

## DISTINCTIVE CHARACTERISTICS

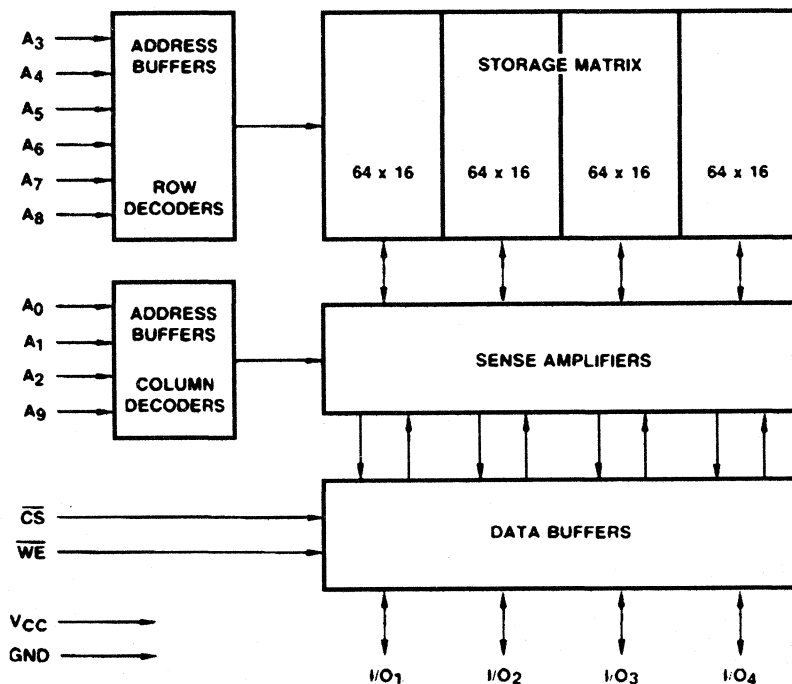
- Low operating and standby power
- Access times down to 200 ns
- Am9114 is a direct plug-in replacement for 2114
- High output drive: 3.2-mA sink current @ 0.4 V
- TTL-identical input/output levels

## GENERAL DESCRIPTION

The Am9114/Am91L14 Series are high-performance, static, N-Channel, read/write, random-access memories organized as 1024 x 4. Operation is from a single 5-V supply, and all input/output levels are identical to standard TTL specifications. Low-power version is available with power savings of over 30%.

Data readout is not destructive and the same polarity as data input.  $\overline{CS}$  provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 3.2 mA for Am9114 provides increased short-circuit current for improved capacitive drive.

## BLOCK DIAGRAM



BD000082

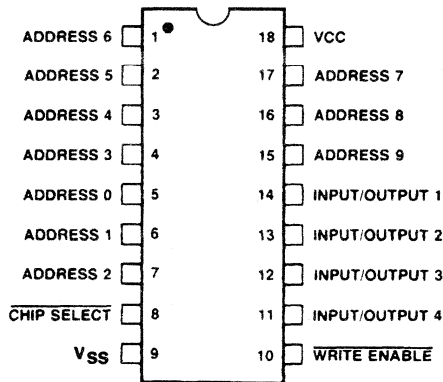
## PRODUCT SELECTOR GUIDE

Part Number			Am9114/91L14		Am9114/91L14
Speed Indicator			B	C	E
Maximum Access Time (ns)			450	300	200
0 to +70°C	I <sub>CC</sub> (mA)	Standard	70	70	70
		Low-Power	50	50	50
-55 to +125°C	I <sub>CC</sub> (mA)	Standard	80	80	80
		Low-Power	60	60	60

## CONNECTION DIAGRAM

Top View

DIPs



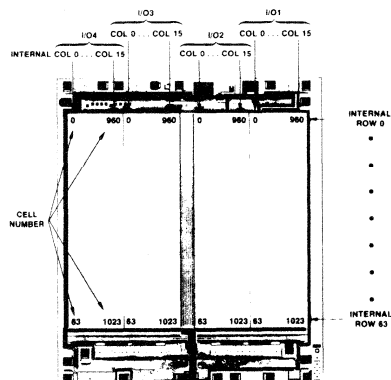
CD000132

Note: Pin 1 is marked for orientation.

4

## METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A <sub>0</sub>	A <sub>9</sub>
A <sub>1</sub>	A <sub>8</sub>
A <sub>2</sub>	A <sub>7</sub>
A <sub>3</sub>	A <sub>0</sub>
A <sub>4</sub>	A <sub>1</sub>
A <sub>5</sub>	A <sub>2</sub>
A <sub>6</sub>	A <sub>3</sub>
A <sub>7</sub>	A <sub>4</sub>
A <sub>8</sub>	A <sub>5</sub>
A <sub>9</sub>	A <sub>6</sub>

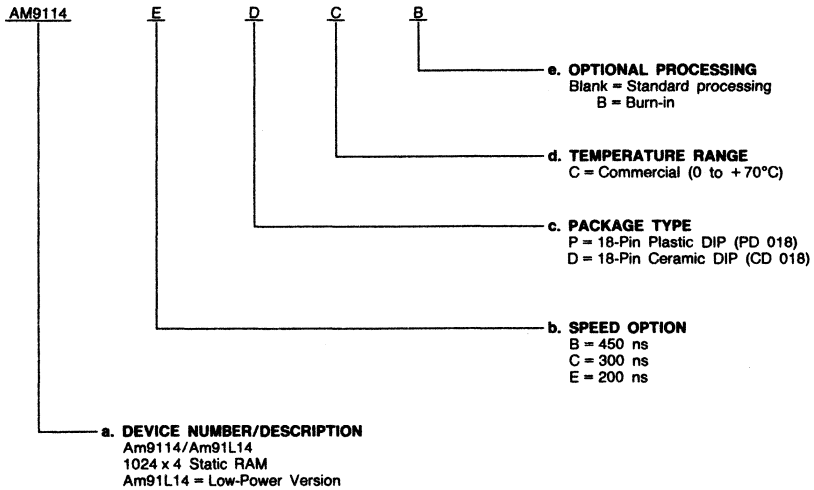


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM9114B	PC, PCB, DC, DCB
AM91L14B	
AM9114C	
AM91L14C	
AM9114E	
AM91L14E	

### Valid Combinations

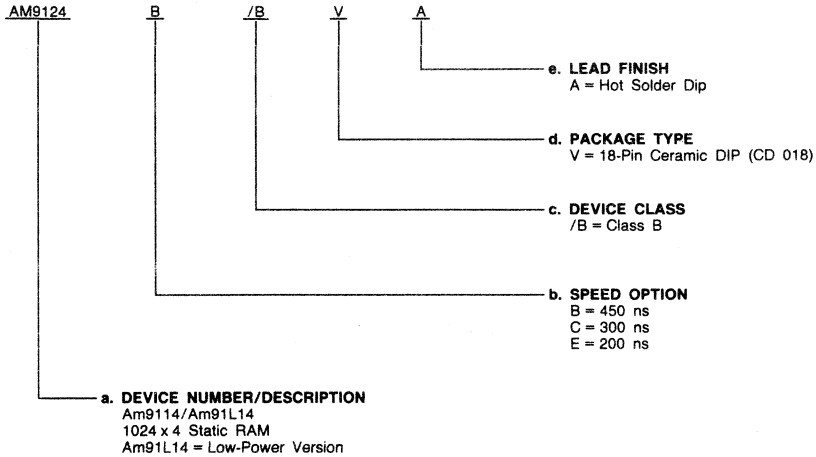
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM9114B	/BVA
AM91L14B	
AM9114C	
AM91L14C	
AM9114E	
AM91L14E	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups  
 1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

**A<sub>0</sub> - A<sub>9</sub> Address Inputs**

The address input lines select the memory location from which to read or write.

**$\overline{\text{CS}}$  Chip Select (Input, Active LOW)**

The  $\overline{\text{CS}}$  line selects the memory device for active operation.

**$\overline{\text{WE}}$  Write Enable (Input, Active LOW)**

When both  $\overline{\text{CS}}$  and  $\overline{\text{WE}}$  are LOW, data on the input lines is written to the location presented on the address input lines.

**I/O<sub>1</sub> - I/O<sub>4</sub> Data In/Out Bus (Bidirectional)**

These lines provide the path for data to be written to or read from the selected memory location.

**V<sub>CC</sub> Power Supply**

**V<sub>SS</sub> Ground**

**TABLE 1. SUPPLY CURRENT ADVANTAGE**

		Worst Case Current (mA at 0°C)	
Configuration	Part Number	100% Duty Cycle	50% Duty Cycle
2K x 8	9114	280	280
	91L14	200	200
4K x 12	9114	840	840
	91L14	600	600
8K x 16	9114	2240	2240
	91L14	1600	1600



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
Signal Voltages with Respect to Ground .....	-0.5 V to +7.0 V
Power Dissipation .....	1.0 W
DC Output Current .....	10 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGES (Note 2)

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0°C to +70°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5V to +5.5 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55°C to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military products 100% tested at T<sub>C</sub> = +25°C, +125°C and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I <sub>OH</sub>	Output HIGH Current	V <sub>CC</sub> = +4.5V V <sub>OH</sub> = 2.4V	91(L)14	-1.0		mA
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4V	T <sub>A</sub> = 70°C 91(L)14 T <sub>A</sub> = +125°C 91(L)14	3.2 2.4		
V <sub>IH</sub>	Input HIGH Voltage			2.0	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage			-0.5	0.8	
I <sub>Ix</sub>	Input Load Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>			10	μA
I <sub>OZ</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled	T <sub>A</sub> = 0 to +70°C T <sub>A</sub> = -55 to +125°C	-10 -50	10 50	
I <sub>OS</sub>	Output Short Circuit Current	(Note 3)	91(L)14C 91(L)14M		75 75	mA
I <sub>CC</sub>	Operating Supply Current	V <sub>CC</sub> = Max. CS ≤ V <sub>IL</sub>	T <sub>A</sub> = 0°C T <sub>A</sub> = -55°C		70 50 80 60	
C <sub>IN</sub>	Input Capacitance	(Note 7)	f = 1.0 MHz, T <sub>A</sub> = 25°C, All pins at 0V		7	pF
C <sub>I/O</sub>	I/O Capacitance				7	

- Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
  2. For test and correlation purposes, ambient temperature is defined as the "Instant-ON" case temperature.
  3. For test purposes, not more than one output at a time should be shorted. Short-circuit test duration should not exceed 30 seconds. Actual testing is performed for only 5 ms.
  4. Test conditions assume signal transition time of 10 ns or less, timing reference levels of 1.5 V, output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> plus 100 pF or plus 5 pF for T<sub>CX</sub>, T<sub>OTP</sub> and T<sub>OTW</sub>.
  5. The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
  6. The specified address access time will be valid only when Chip Select is low soon enough for t<sub>CO</sub> to elapse.
  7. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
  8. Transition is measured from 1.5 V on the input to (V<sub>OH</sub> - 500 mV) and (V<sub>OL</sub> + 500 mV) on the output.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Notes 4 – 6)

No.	Parameter Symbol	Parameter Description	B Devices		C Devices		E Devices		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>									
1	t <sub>RC</sub>	Address Valid to Address Do Not Care Time (Read Cycle Time)	450		300		200		ns
2	t <sub>A</sub>	Address Valid to Data Out Valid Delay (Address Access Time)		450		300		200	ns
3	t <sub>CO</sub>	Chip Select LOW to Data Out Valid (Note 6)		120		100		70	ns
4	t <sub>CX</sub>	Chip Select LOW to Data Out On (Notes 7, 8)	10		10		10		ns
5	t <sub>OTD</sub>	Chip Select HIGH to Data Out Off (Notes 7, 8)		100		80		60	ns
6	t <sub>OHA</sub>	Output hold after address change	50		50		50		ns
<b>WRITE CYCLE</b>									
7	t <sub>WC</sub>	Address Valid to Address Do Not Care Time (Write Cycle Time)	450		300		200		ns
8	t <sub>W</sub>	Write Enable LOW to Write Enable HIGH Time (Note 5)	200		150		120		ns
9	t <sub>WR</sub>	Write Enable HIGH to Address Do Not Care Time	0		0		0		ns
10	t <sub>OTW</sub>	Write Enable LOW to Data Out Off Delay (Notes 7, 8)		100		80		60	ns
11	t <sub>DW</sub>	Data In Valid to Write Enable HIGH Time	200		150		120		ns
12	t <sub>DH</sub>	Write Enable HIGH to Data In Do Not Care Time	0		0		0		ns
13	t <sub>AW</sub>	Address Valid to Write Enable LOW Time	0		0		0		ns
14	t <sub>CW</sub>	Chip Select LOW to Write Enable HIGH Time (Note 5)	200		150		120		90

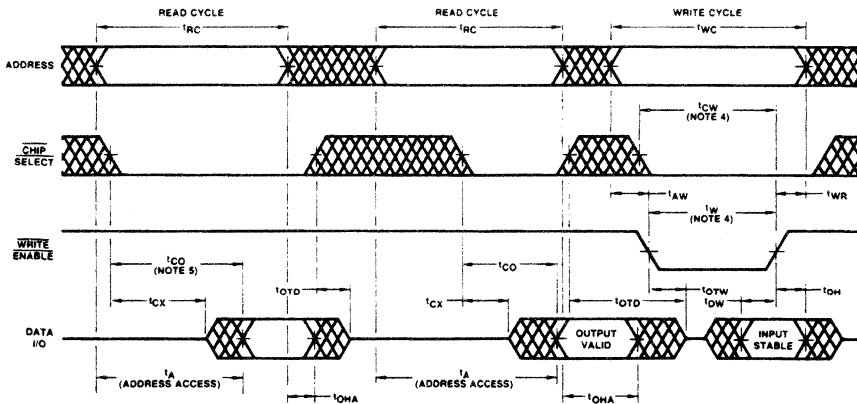
Notes: See notes following DC Characteristics table.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

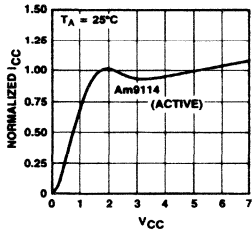


WF000171

Notes: See notes following DC Characteristics table.

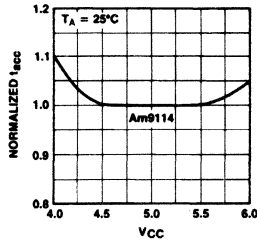
## TYPICAL PERFORMANCE CURVES

**Normalized Supply Current Versus Supply Voltage**



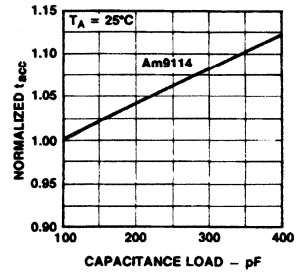
OP000532

**Normalized Access Time Versus Supply Voltage**



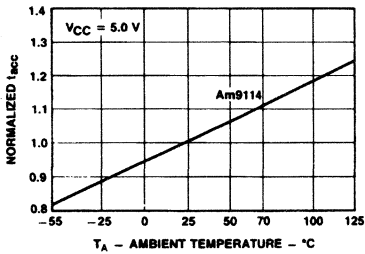
OP000542

**Normalized Access Time Versus Output Loading**



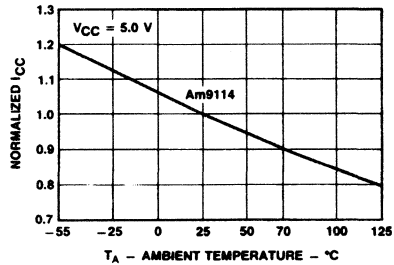
OP000552

**Normalized Access Time Versus Ambient Temperature**



OP000202

**Normalized Supply Current Versus Ambient Temperature**



OP000212

# Am2147/Am21L47

## 4096x1 Static RAM

### DISTINCTIVE CHARACTERISTICS

- High speed — access times down to 35 ns maximum
- Automatic power-down when deselected
- Low power dissipation
- High output drive
- TTL compatible interface levels
- No power-on current surge

### GENERAL DESCRIPTION

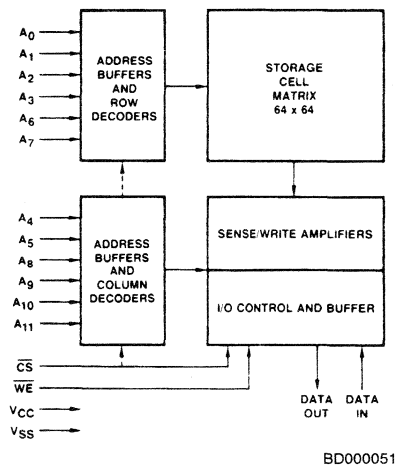
The Am2147/Am21L47 Series are high-performance, 4096 x 1-bit, static, read/write, random-access memories. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard TTL loads or up to six Schottky TTL loads.

Only a single +5-volt power supply is required. When deselected ( $\overline{CS} \geq V_{IH}$ ), the Am2147 automatically enters a

power-down mode which reduces power dissipation by more than 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a three-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

### BLOCK DIAGRAM

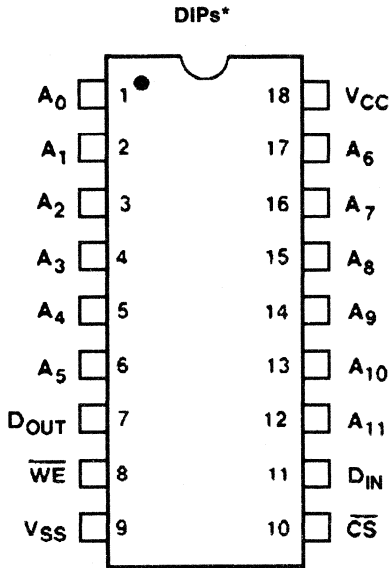


4

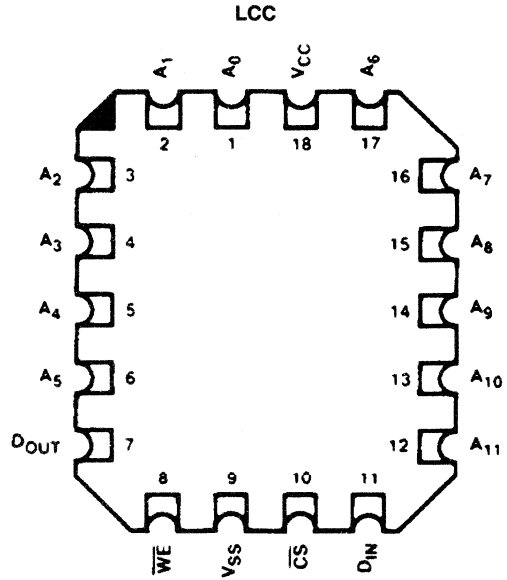
### PRODUCT SELECTOR GUIDE

Part Number	Am2147-35	Am2147-45	Am21L47-45	Am2147-55	Am21L47-55	Am2147-70	Am21L47-70
Maximum Access time (ns)	35	45	45	55	55	70	70
Maximum Active Current (mA)	180	180	125	180	125	160 (180 mil)	125
Maximum Standby Current (mA)	30	30	15	30	15	20 (30 mil)	15
Full Military Operating Range Version		Yes		Yes		Yes	

**CONNECTION DIAGRAMS**  
**Top View**



CD000091



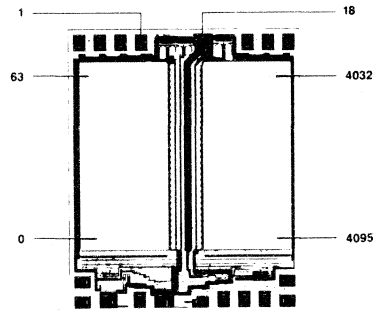
CD000100

\*Also available for military customers in an 18-Pin Ceramic Flatpack. Pinout is identical to DIPs.

Note: Pin 1 is marked for orientation.

**BIT MAP**

Address Designators	
External	Internal
A <sub>0</sub>	A <sub>2</sub>
A <sub>1</sub>	A <sub>5</sub>
A <sub>2</sub>	A <sub>4</sub>
A <sub>3</sub>	A <sub>3</sub>
A <sub>4</sub>	A <sub>8</sub>
A <sub>5</sub>	A <sub>7</sub>
A <sub>6</sub>	A <sub>1</sub>
A <sub>7</sub>	A <sub>0</sub>
A <sub>8</sub>	A <sub>11</sub>
A <sub>9</sub>	A <sub>9</sub>
A <sub>10</sub>	A <sub>10</sub>
A <sub>11</sub>	A <sub>6</sub>



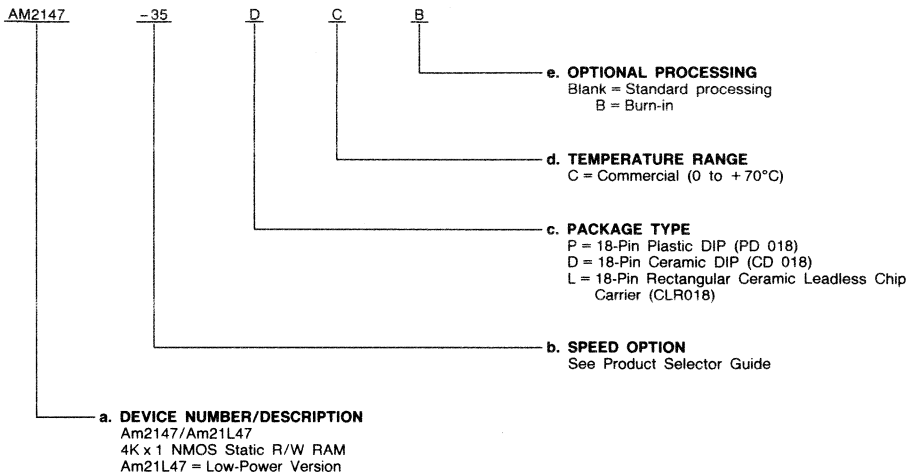
Die Size: 0.130 x 0.106

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM2147-35	PC, PCB, DC, DCB, LC, LCB
AM2147-45	
AM2147-55	
AM2147-70	
AM21L47-45	
AM21L47-55	
AM21L47-70	

### Valid Combinations

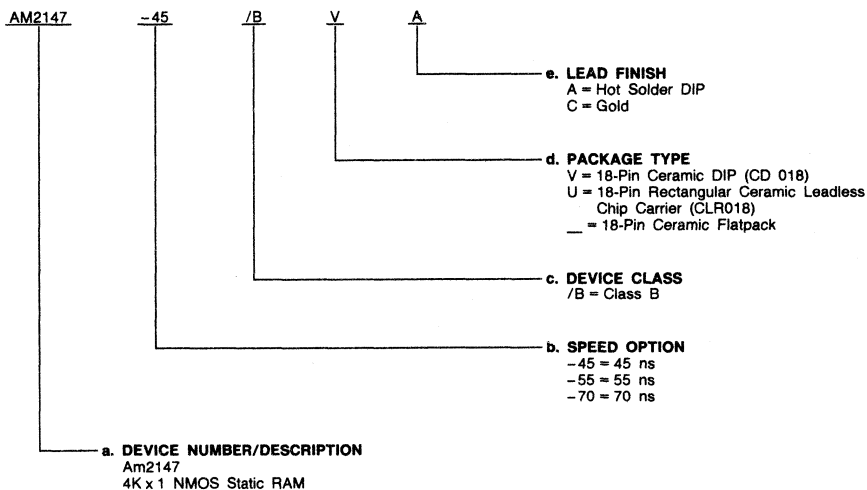
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM2147-45	/BVA
AM2147-55	
AM2147-70	
AM2147-45	/BUC
AM2147-55	
AM2147-70	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

#### **A<sub>0</sub> - A<sub>11</sub> Address Inputs**

The address input lines select the RAM location to be read or written.

#### **CS Chip Select (Input, Active LOW)**

The Chip Select selects the memory device.

#### **WE Write Enable (Input, Active LOW)**

When WE is LOW and CS is also LOW, data is written into the location specified on the address pins.

#### **D<sub>IN</sub> Data In (Input)**

This pin is used for entering data during write operations.

#### **D<sub>OUT</sub> Data Out (Output, Three-State)**

This pin is three state during write operations. It becomes active when CS is LOW and WE is HIGH.

#### **V<sub>CC</sub> Power Supply**

#### **V<sub>SS</sub> Ground**



## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
Signal Voltages with respect to ground .....	-3.5 V to +7.0 V
Power Dissipation .....	1.2 W
DC Output Current .....	20. mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Absolute Maximum Ratings are for system-design reference; parameters given are not 100% tested.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +70°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Military (M) Devices	
Ambient Temperature (T <sub>A</sub> )* .....	-55 to +125°C
Supply Voltage V <sub>CC</sub> .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*T<sub>A</sub> is defined as the "instant on" case temperature.

Parameter Symbol	Parameter Description	Test Conditions	Am2147-35 Am2147-45 Am2147-55		Am21L47-45 Am21L47-55		Am2147-70		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V	V <sub>CC</sub> = 4.5 V		-4	-4	-4	-4	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	T <sub>A</sub> = 70°C		12	12	12		mA	
			T <sub>A</sub> = 125°C		8	N/A	8			
V <sub>IH</sub>	Input High Voltage		2.0	6.0	2.0	6.0	2.0	6.0	V	
V <sub>IL</sub>	Input Low Voltage		-2.5	0.8	-2.5	0.8	-2.5	0.8	V	
I <sub>Ix</sub>	Input Load Current	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	10	-10	10	-10	10	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disables	T <sub>A</sub> = -55 to +125°C		-50	50	-50	50	μA	
C <sub>I</sub>	Input Capacitance	Test Frequency = 1.0 MHz (Note 4)		5		5		5		
C <sub>O</sub>	Output Capacitance	T <sub>A</sub> = 25°C, All pins at 0 V, V <sub>CC</sub> = 5 V		6		6		6		
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	Max. V <sub>CC</sub> CS ≤ V <sub>IL</sub> Output Open	T <sub>A</sub> = 0 to 70°C		180		125		160	
			T <sub>A</sub> = -55 to 125°C		180		N/A		180	
I <sub>SB</sub>	Automatic CS Power Down Current	Max. V <sub>CC</sub> , (CS ≥ V <sub>IH</sub> ) (Note 3)	T <sub>A</sub> = 0 to 70°C		30		15		20	
			T <sub>A</sub> = -55 to +125°C		30		N/A		30	

- Notes: 1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be low to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power up. Otherwise I<sub>SB</sub> will exceed values given.
4. These parameters are not 100% tested, but guaranteed by characterization.
5. Chip deselected greater than 55 ns prior to selection.
6. Chip deselected less than 55 ns prior to selection.
7. Transition is measured at 1.5 V on the input to V<sub>OH</sub> - 500 mV and V<sub>OL</sub> + 500 mV on the outputs using the load shown in Figure B under Switching Test Circuit.
8. WE is HIGH for read cycle.
9. Device is continuously selected, CS = V<sub>IL</sub>.
10. Address valid prior to or coincident with CS transition LOW.



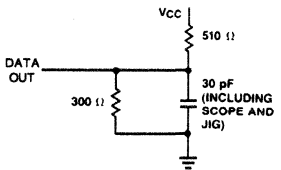
**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (Note 1) (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am2147-35		Am2147-45 Am21L47-45		Am2147-55 Am21L47-55		Am2147-70 Am21L47-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>											
1	t <sub>RC</sub>	Address Valid to Address Do Not Care Time (Read Cycle Time)	35		45		55		70		ns
2	t <sub>AA</sub>	Address Valid to Data Out Valid Delay (Address Access Time)		35		45		55		70	ns
3	t <sub>ACS1</sub>	Chip Select LOW to Data Out Valid		35		45		55		70	ns
4	t <sub>ACS2</sub>	Chip Select LOW to Data Out On (Notes 4 & 7)		35		45		65		80	
5	t <sub>LZ</sub>	Chip Select HIGH to Data Out Off (Notes 4 & 7)	0	30	0	30	0	30	0	40	ns
6	t <sub>HZ</sub>	Output hold after address change	5		5		5		5		ns
7	t <sub>OH</sub>	Chip Select HIGH Power Down Delay (Note 4)		20		20		20		30	ns
8	t <sub>PD</sub>	Chip Select LOW to Power Up Delay (Note 4)	0		0		0		0		ns
9	t <sub>PU</sub>										

<b>WRITE CYCLE</b>											
10	t <sub>WC</sub>	Address Valid to Address Do Not Care (Write Cycle Time)	35		45		55		70		ns
11	t <sub>WP</sub>	Write Enable LOW to Write Enable High (Note 2)	20		25		25		40		ns
12	t <sub>WR</sub>	Write Enable HIGH to Address	0		0		10		15		ns
13	t <sub>WZ</sub>	Write Enable LOW to Output in Hi Z (Notes 4 & 7)	0	20	0	25	0	25	0	35	ns
14	t <sub>DW</sub>	Data In Valid to Write Enable HIGH	20		25		25		30		ns
15	t <sub>DH</sub>	Data Hold Time	10		10		10		10		ns
16	t <sub>AS</sub>	Address Valid to Write Enable LOW	0		0		0		0		ns
17	t <sub>CW</sub>	Chip Select LOW to Write Enable HIGH (Note 2)	35		45		45		55		ns
18	t <sub>OW</sub>	Write Enable HIGH to Output in Low Z (Notes 4 & 7)	0		0		0		0		ns
19	t <sub>AW</sub>	Address Valid to End of Write	35		45		45		55		ns

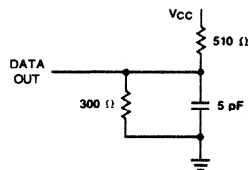
Notes: See notes following DC Characteristics table.

**SWITCHING TEST CIRCUITS**



TC000062

**A. Output Load**



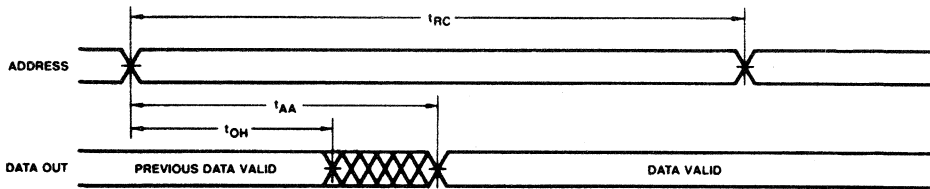
TC000072

**B. Output Load  
for t<sub>HZ</sub>, t<sub>LZ</sub>, t<sub>OW</sub>, t<sub>WZ</sub>**

**SWITCHING WAVEFORMS**  
**KEY TO SWITCHING WAVEFORMS**

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

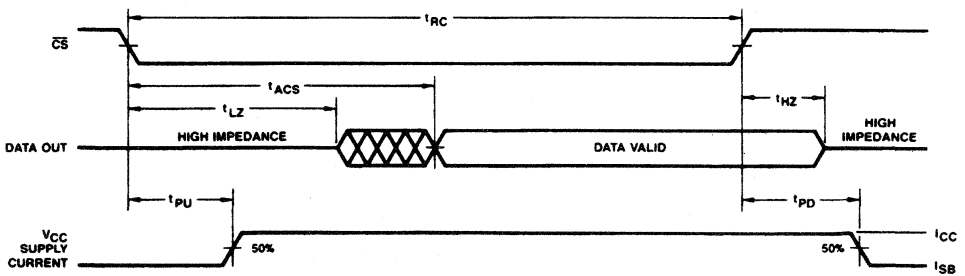
KS000010



WF000461

**Read Cycle No. 1 (Notes 8, 9)**

4

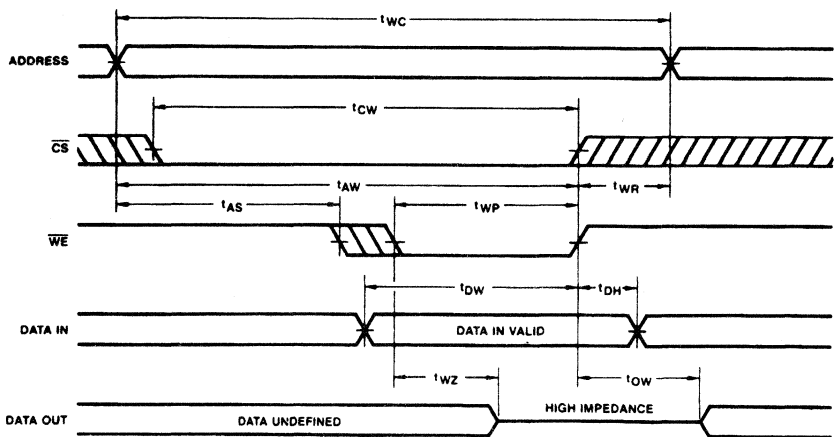


WF000471

**Read Cycle No. 2 (Notes 8, 10)**

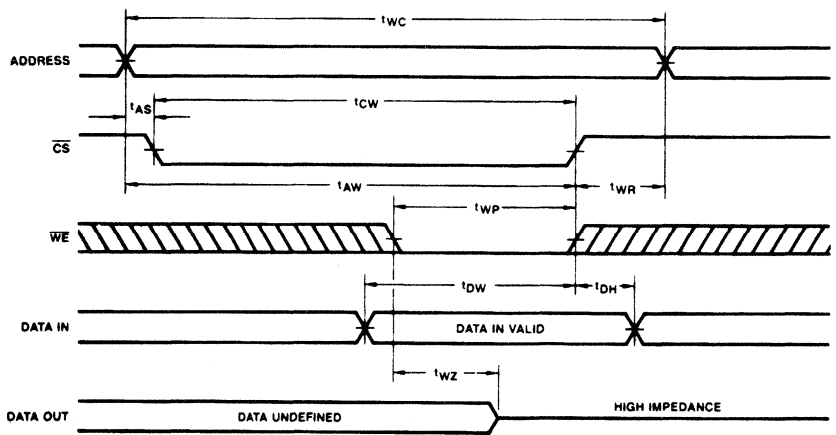
Notes: See notes following DC Characteristics table.

SWITCHING WAVEFORMS (Cont'd.)



WF000211

Write Cycle No. 1 ( $\overline{WE}$  Controlled)



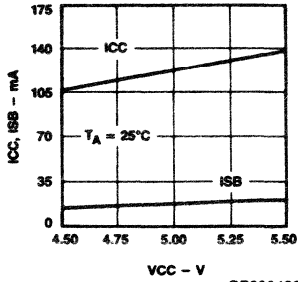
WF000221

Write Cycle No. 2 ( $\overline{CS}$  Controlled)

Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  high, the output remains in a high impedance state.

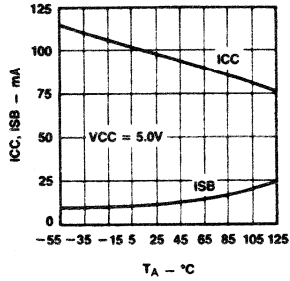
## TYPICAL PERFORMANCE CURVES

**Supply Current  
Versus Supply Voltage**



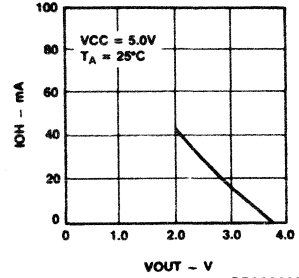
OP000430

**Supply Current  
Versus Ambient Temperature**



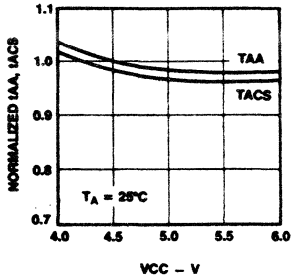
OP000440

**Output Source Current  
Versus Output Voltage**



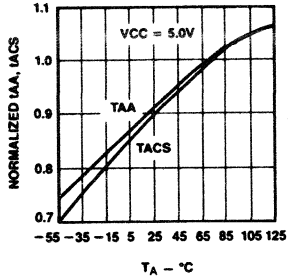
OP000220

**Normalized Access Time  
Versus Supply Voltage**



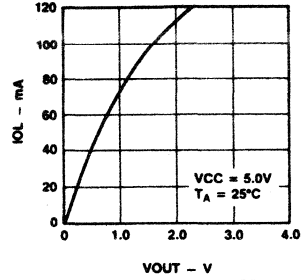
OP000760

**Normalized Access Time  
Versus Ambient Temperature**



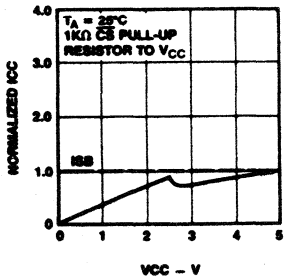
OP000230

**Output Sink Current  
Versus Output Voltage**



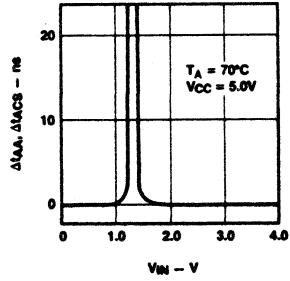
OP000240

**Typical Power-On Current  
Versus Power Supply**



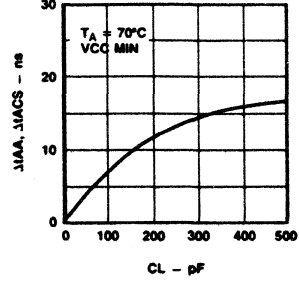
OP000870

**Access Time Change  
Versus Input Voltage**



OP000800

**Access Time Change  
Versus Output Loading**



OP000270



# Am2148/Am2149

## Am21L48/Am21L49

1024x4 Static RAM



### DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 35 ns
- Fully static storage and interface circuitry
- Automatic power-down when deselected (Am2148)
- TTL-compatible interface levels
- Low power dissipation
  - Am2148: 990 mW active, 165 mW power down
  - Am21L48: 688 mW active, 110 mW power down
- High output drive
  - Up to seven standard TTL loads

### GENERAL DESCRIPTION

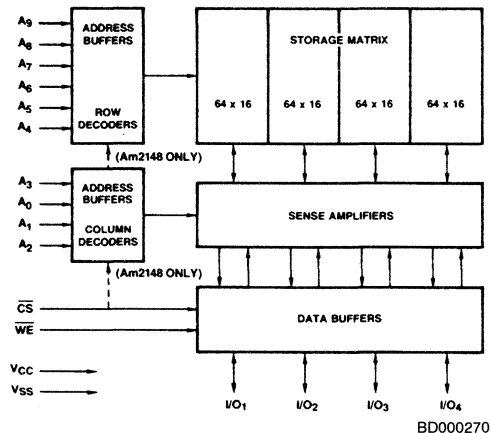
The Am2148 and Am2149 are high-performance, static, N-Channel, read/write, random-access memories, organized as 1024 x 4. Operation is from a single 5-V supply, and all input/output levels are identical to standard TTL specifications. The Am2148 and Am2149 are the same except that the Am2148 offers an automatic  $\overline{CS}$  power-down feature.

The Am2148 remains in a low-power standby mode as long as  $\overline{CS}$  remains HIGH, thus reducing its power requirements.

The Am2148 power decreases from 990 mW to 165 mW in the standby mode. The  $\overline{CS}$  input does not affect the power dissipation of the Am2149.

Data readout is non-destructive and has the same polarity as data input.  $\overline{CS}$  provides for easy selection of an individual package when the outputs are OR-tied.

### BLOCK DIAGRAM

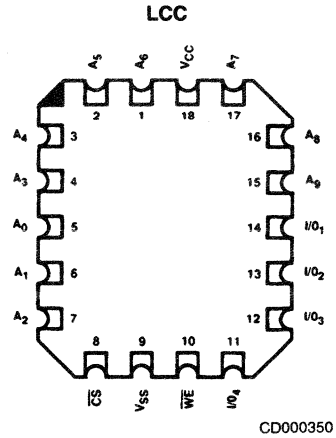
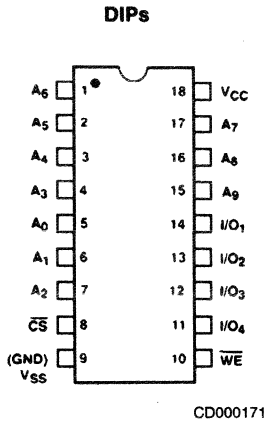


### PRODUCT SELECTOR GUIDE

Part Number	Am2148/9 -35	Am2148/9 -45	Am21L48/9 -45	Am2148/9 -55	Am21L48/9 -55	Am2148/9 -70	Am21L48/9 -70
Maximum Access Time (ns)	35	45	45	55	55	70	70
$I_{CC}$ Max. (mA)	0 to +70°C		125	180	125	180	125
$I_{SB}^*$ Max. (mA)	+70°C		20	30	20	30	20
$I_{CC}$ Max. (mA)	-55 to +125°C		N/A	180	N/A	180	N/A
$I_{SB}^*$ Max. (mA)	+125°C		N/A	30	N/A	30	N/A

\*Am2148 and Am21L48 only.

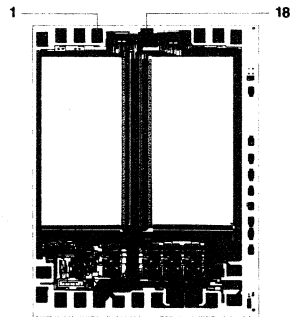
## CONNECTION DIAGRAMS Top View



Note: Pin 1 is marked for orientation.

## METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A <sub>0</sub>	A <sub>7</sub>
A <sub>1</sub>	A <sub>8</sub>
A <sub>2</sub>	A <sub>9</sub>
A <sub>3</sub>	A <sub>6</sub>
A <sub>4</sub>	A <sub>5</sub>
A <sub>5</sub>	A <sub>4</sub>
A <sub>6</sub>	A <sub>3</sub>
A <sub>7</sub>	A <sub>2</sub>
A <sub>8</sub>	A <sub>1</sub>
A <sub>9</sub>	A <sub>0</sub>



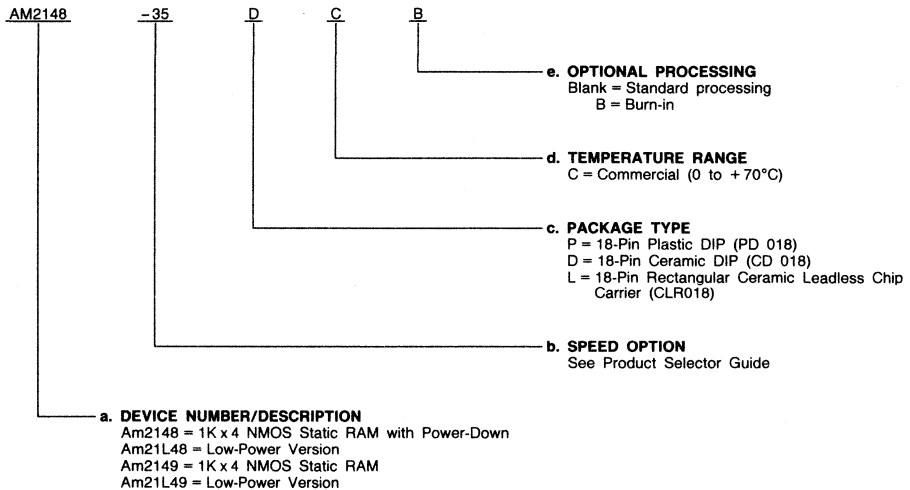
Die Size: 0.107" x 0.145"

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM2148-35	PC, PCB, DC, DCB, LC, LCB
AM2149-35	
AM21L48-45	
AM21L49-45	
AM21L48-55	
AM21L49-55	
AM21L48-70	PC, PCB, DC, DCB, LC, LCB
AM21L49-70	
AM2148-45	
AM2149-45	
AM2148-55	
AM2149-55	
AM2148-70	
AM2149-70	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

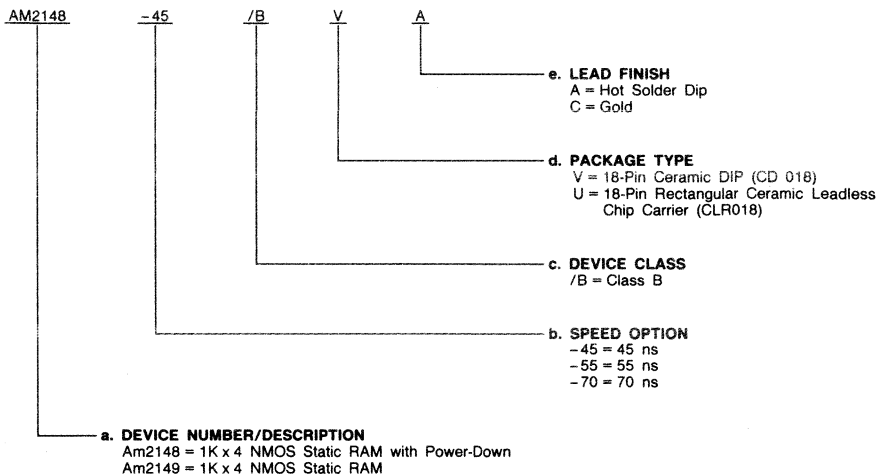


## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM2148-45	/BVA
AM2149-45	
AM2148-55	
AM2149-55	
AM2148-70	
AM2149-70	
AM2148-45	/BUC
AM2149-45	
AM2148-55	
AM2149-55	
AM2148-70	
AM2149-70	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A Tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

4

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>9</sub> Address Inputs

The address input lines select the RAM location to be read or written.

### CS Chip Select (Input, Active LOW)

The Chip Select selects the memory device.

### WE Write Enable (Input, Active LOW)

When WE is LOW and CS is also LOW, data is written into the location specified on the address pins.

### I/O<sub>1</sub> - I/O<sub>4</sub> Data In/Out Bus (Bidirectional, Active HIGH)

These I/O lines provide the path for data to be read from or written to the selected memory location.

### V<sub>CC</sub> Power Supply

### V<sub>SS</sub> Ground

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
Signal Voltages with Respect to Ground .....	-3.5 V to +7.0 V
Power Dissipation .....	1.2 W
DC Output Current .....	20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Absolute Maximum Ratings are for system-design reference; parameters given are not 100% tested.

## OPERATING RANGES

Commercial (C) Devices	Ambient Temperature (T <sub>A</sub> ) .....	0 to +70°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V
Military (M) Devices	Ambient Temperature (T <sub>A</sub> *) .....	-55 to +125°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*T<sub>A</sub> is defined as the "instant on" case temperature.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Standard		Low Power		Unit	
			Min.	Max.	Min.	Max.		
I <sub>OH</sub>	Output HIGH Current	V <sub>OH</sub> = 2.4 V	V <sub>CC</sub> = 4.5 V	-4		-4		mA
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4 V	T <sub>A</sub> = 70°C	8		8		mA
			T <sub>A</sub> = 125°C	8		N/A		
V <sub>IH</sub>	Input HIGH Voltage			2.0	6.0	2.0	6.0	V
V <sub>IL</sub>	Input LOW Voltage			-0.5	0.8	-0.5	0.8	V
I <sub>I</sub>	Input Load Current	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-10	10		10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled	T <sub>A</sub> = -55 to +125°C	-50	50	-50	50	μA
C <sub>I</sub>	Input Capacitance	Test Frequency = 1.0 MHz T <sub>A</sub> = 25°C, All Pins at 0 V, V <sub>CC</sub> = 5 V (Note 12)			5		5	pF
C <sub>I/O</sub>	Input/Output Capacitance					7		
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	Max. V <sub>CC</sub> , $\overline{CS} \leq V_{IL}$ Output Open	T <sub>A</sub> = 0 to +70°C		180		125	mA
			T <sub>A</sub> = -55 to +125°C		180		N/A	
I <sub>SB</sub>	Automatic $\overline{CS}$ Power Down Current	Max. V <sub>CC</sub> , ( $\overline{CS} \geq V_{IH}$ )	T <sub>A</sub> = 0 to +70°C		30		20	mA
			T <sub>A</sub> = -55 to +125°C		30		N/A	
I <sub>PO</sub>	Peak Power-On Current	Max. V <sub>CC</sub> , ( $\overline{CS} \geq V_{IH}$ ) (Notes 3 & 12)	T <sub>A</sub> = 0 to +70°C		50		30	mA
			T <sub>A</sub> = -55 to +125°C		50		N/A	
I <sub>OS</sub>	Output Short-Circuit Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> (Notes 11, 12)	T <sub>A</sub> = 0 to +70°C		±275		±275	mA
			T <sub>A</sub> = -55 to +125°C		±350		±350	

- Notes:
- Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance. Output timing reference is 1.5 V.
  - The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
  - A pullup resistor to V<sub>CC</sub> on the  $\overline{CS}$  input is required to keep the device deselected during V<sub>CC</sub> power up. Otherwise I<sub>PO</sub> will exceed values given (Am2148 only).
  - The operating ambient temperature is defined as the "instant-ON" case temperature.
  - Chip deselected greater than 55 ns prior to selection.
  - Chip deselected less than 55 ns prior to selection.
  - Transition is measured ±500 mV from steady state voltage with specified loading in Figure B. These parameters are sampled and not 100% tested.
  - $\overline{WE}$  is HIGH for read cycle.
  - Device is continuously selected,  $\overline{CS} = V_{IL}$ .
  - Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
  - For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
  - This parameter is sampled and not 100% tested, but guaranteed by characterization.

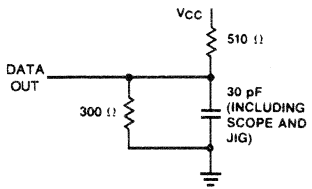
**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (Note 1) (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am2148/9-35		Am2148/9-45 Am21L48/9-45		Am2148/9-55 Am21L48/9-55		Am2148/9-70 Am21L48/9-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>											
1	t <sub>RC</sub>	Address Valid to Address Do Not Care Time (Read Cycle Time)	35		45		55		70		ns
2	t <sub>AA</sub>	Address Valid to Data Out Valid Delay (Address Access Time)		35		45		55		70	ns
3	t <sub>ACS1</sub>	Chip Select LOW to Data Out Valid (Am2148 only)		35		45		55		70	ns
4	t <sub>ACS2</sub>	Chip Select LOW to Data Out Valid (Am2149 only)		45		55		65		80	
5	t <sub>ACS</sub>	Chip Select LOW to Data Out Valid (Am2149 only)		15		20		25		30	ns
6	t <sub>LZ</sub>	Chip Select LOW to Data Out On (Notes 7 & 12)	Am2148	10		10		10		10	ns
			Am2149	5		5		5		5	
7	t <sub>HZ</sub>	Chip Select HIGH to Data Out Off (Notes 7 & 12)	0	20	0	20	0	20	0	20	ns
8	t <sub>OH</sub>	Output hold after address change	5		5		5		5		ns
9	t <sub>PD</sub>	Chip Select HIGH to Power Down Delay (Note 12)	Am2148		30		30		30		ns
10	t <sub>PU</sub>	Chip Select LOW to Power Up Delay (Note 12)	Am2148	0		0		0		0	ns
<b>Write Cycle</b>											
11	t <sub>WC</sub>	Address Valid to Address Do Not Care (Write Cycle Time)	35		45		55		70		ns
12	t <sub>WP</sub>	Write Enable LOW to Write Enable HIGH (Note 2)	30		35		40		50		ns
13	t <sub>WR</sub>	Write Enable HIGH to Address	5		5		5		5		ns
14	t <sub>WZ</sub>	Write Enable LOW to Output in High Z (Notes 7 & 12)	0	10	0	15	0	20	0	25	ns
15	t <sub>DW</sub>	Data In Valid to Write Enable HIGH	20		20		20		25		ns
16	t <sub>DH</sub>	Data Hold Time	0		0		0		0		ns
17	t <sub>AS</sub>	Address Valid to Write Enable LOW	0		0		0		0		ns
18	t <sub>CW</sub>	Chip Select LOW to Write Enable HIGH (Note 2)	30		40		50		65		ns
19	t <sub>OW</sub>	Write Enable HIGH to Output in Low Z (Notes 7 & 12)	0		0		0		0		ns
20	t <sub>AW</sub>	Address Valid to End of Write	30		40		50		65		ns

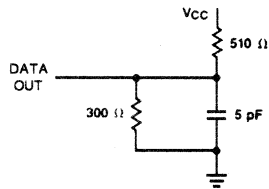
Notes: See notes following DC Characteristics table.

4

**SWITCHING TEST CIRCUITS**









**A. Output Load**



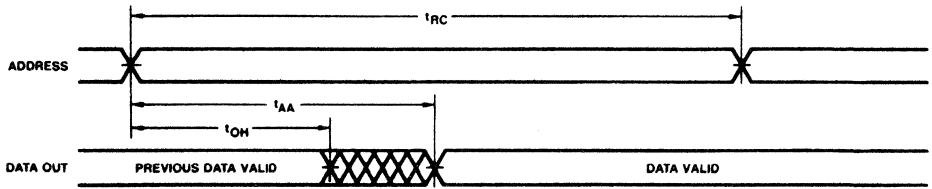
**B. Output Load  
for t<sub>HZ</sub>, t<sub>LZ</sub>, t<sub>OW</sub>, t<sub>WZ</sub>**

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

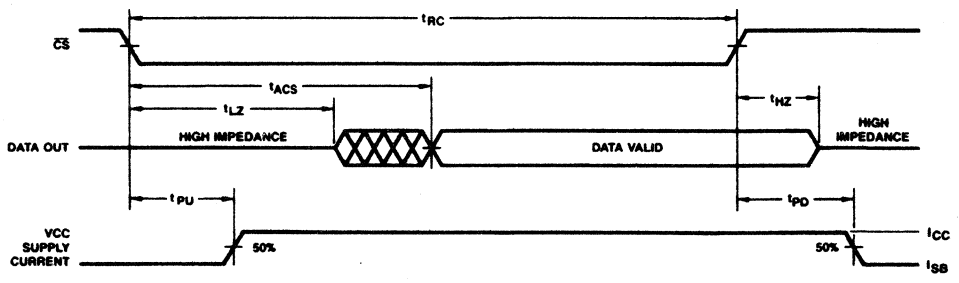
WAVEFORM	INPUTS	OUTPUTS
 	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF000461

**Read Cycle No. 1 (Notes 8, 9)**

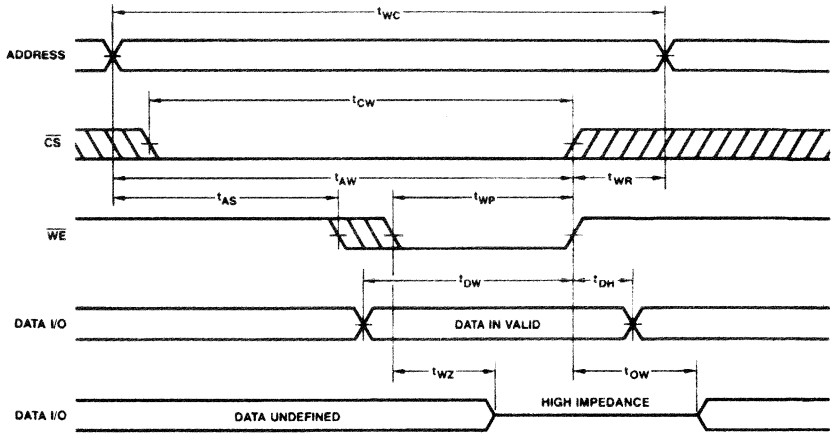


WF000241

**Read Cycle No. 2 (Notes 8, 10)**

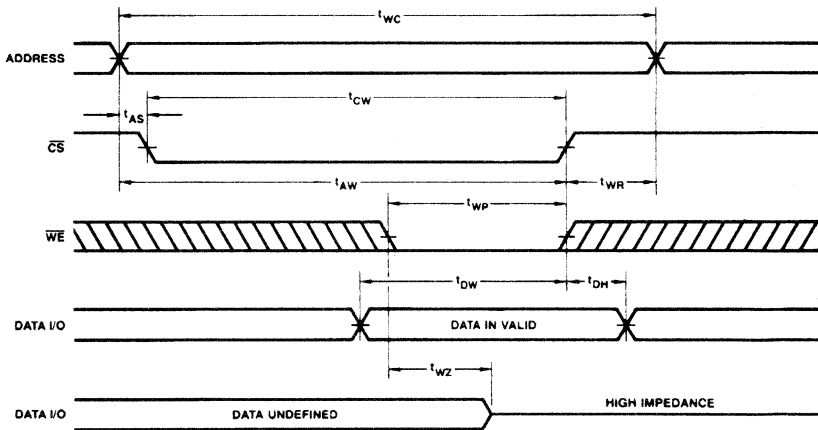
Notes: See notes following DC Characteristics table.

SWITCHING WAVEFORMS (Cont'd.)



WF000711

Write Cycle No. 1 ( $\overline{WE}$  Controlled)



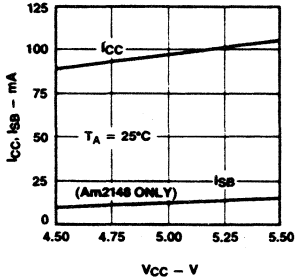
WF000721

Write Cycle No. 2 ( $\overline{CS}$  Controlled)

Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

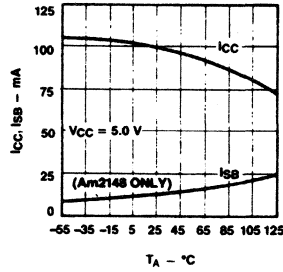
## TYPICAL PERFORMANCE CURVES

**Supply Current  
Versus Supply Voltage**



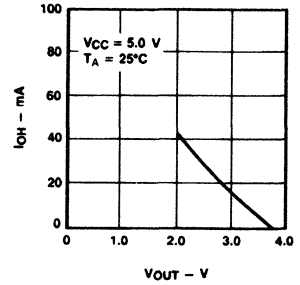
OP000730

**Supply Current  
Versus Ambient Temperature**



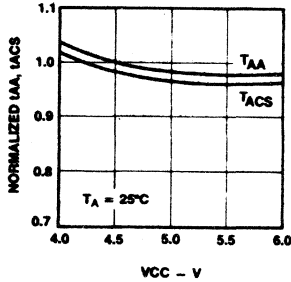
OP000741

**Output Source Current  
Versus Output Voltage**



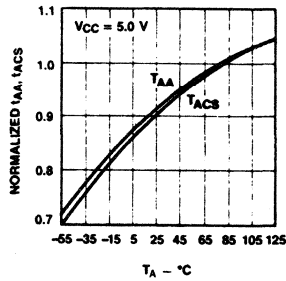
OP001081

**Normalized Access Time  
Versus Supply Voltage**



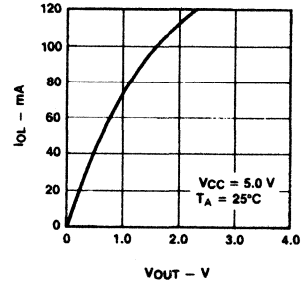
OP000761

**Normalized Access Time  
Versus Ambient Temperature**



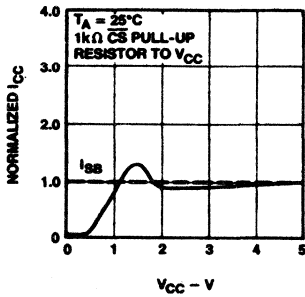
OP000771

**Output Sink Current  
Versus Output Voltage**



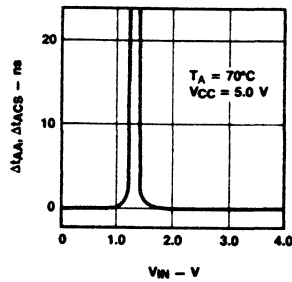
OP001091

**Typical Power-On Current  
Versus Power Supply**



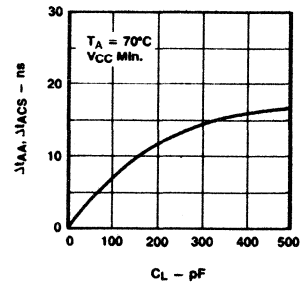
OP000791

**Access Time Change  
Versus Input Voltage**



OP000801

**Access Time Change  
Versus Output Loading**



OP001101

# Am9150

1024x4 High-Speed Static R/W RAM



## DISTINCTIVE CHARACTERISTICS

- 1024 x 4 organization
- High speed - 20 ns Max. access time
- Separate data inputs and outputs
- Memory reset function
- High density SLIM 24-pin 300-MIL package
- Three-state output buffers
- Single +5 V power supply  $\pm 10\%$
- Low-power version

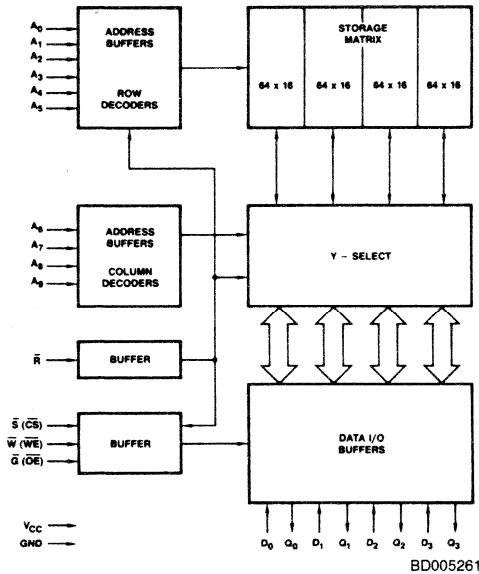
## GENERAL DESCRIPTION

The Am9150 is a high-performance, static, n-channel, read/write, random-access memory organized as 1024 x 4. It features single 5 V supply operation, TTL-compatible input and output levels, and separate input and output pins for improved system performance and ease of use.

The Am9150 also incorporates a reset feature which will reset the entire contents of the memory to logical LOW in two cycle times by controlling  $\bar{R}$  (RESET) and  $\bar{S}$  (CS).

The Am9150 has four control signals  $\bar{R}$ ,  $\bar{S}$ ,  $\bar{W}$  and  $\bar{G}$ . The  $\bar{S}$  input controls read, write and reset operations of the device and provides for easy selection of an individual device when the outputs are tied together. The  $\bar{W}$  ( $\bar{W}$ E) input controls the normal read and write operations, and the  $\bar{G}$  ( $\bar{O}$ E) controls the state of the outputs.

## BLOCK DIAGRAM



## MODE SELECT TABLE

Inputs				Outputs	Mode
$\bar{S}$	$\bar{W}$	$\bar{G}$	$\bar{R}$		
H	X	X	X	Hi-Z	Not Selected
L	H	X	L	Hi-Z	Reset*
L	L	X	H	Hi-Z	Write
L	H	L	H	Q <sub>0</sub> -Q <sub>3</sub>	Read
L	X	H	H	Hi-Z	Output Disable

H = High  
L = Low  
X = Don't Care

\*See Reset cycle description.

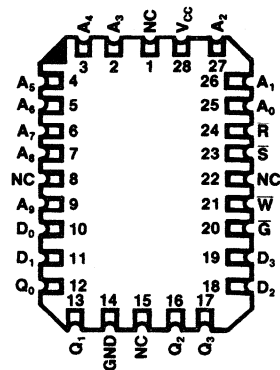
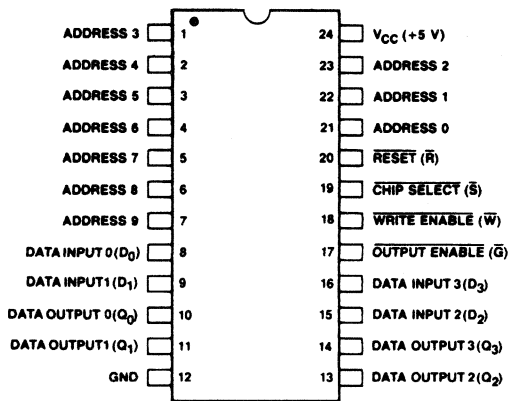
4

## PRODUCT SELECTOR GUIDE

Part Number	Am9150-20	Am9150-25	Am9150-35	Am9150-45	Am91L50-25	Am91L50-35	Am91L50-45
Maximum Access Time (ns)	20	25	35	45	25	35	45
I <sub>cc</sub> Max. (mA)	0°C to +70°C	180	180	180	130	130	130
	-55°C to +125°C	N/A	180	180	180	N/A	N/A

Publication # 04444  
Rev. C  
Amendment /0  
Issue Date: January 1989

## CONNECTION DIAGRAMS Top View

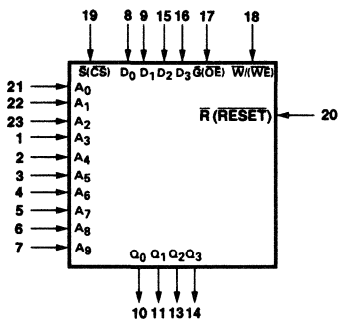


CD005931

CD005963

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL (DIP ONLY)

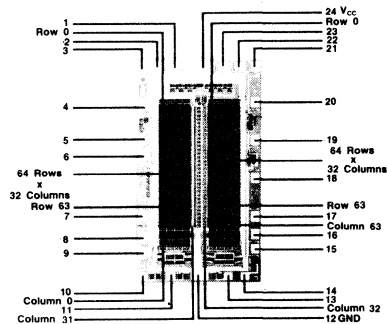


LS001821

### Address Designators

External	Internal
A <sub>0</sub>	AX <sub>0</sub>
A <sub>1</sub>	AX <sub>1</sub>
A <sub>2</sub>	AX <sub>2</sub>
A <sub>3</sub>	AX <sub>3</sub>
A <sub>4</sub>	AX <sub>4</sub>
A <sub>5</sub>	AX <sub>5</sub>
A <sub>6</sub>	AY <sub>0</sub>
A <sub>7</sub>	AY <sub>1</sub>
A <sub>8</sub>	AY <sub>2</sub>
A <sub>9</sub>	AY <sub>3</sub>

### METALLIZATION AND PAD LAYOUT



Die Size: 0.93" x 0.163"

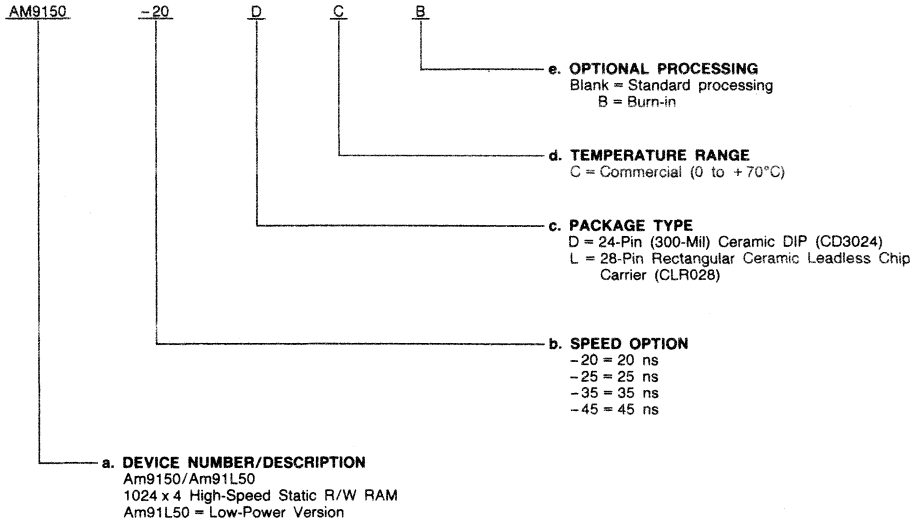


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM9150-20	DC, DCB, LC, LCB
AM9150-25	
AM9150-35	
AM9150-45	
AM91L50-25	
AM91L50-35	
AM91L50-45	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

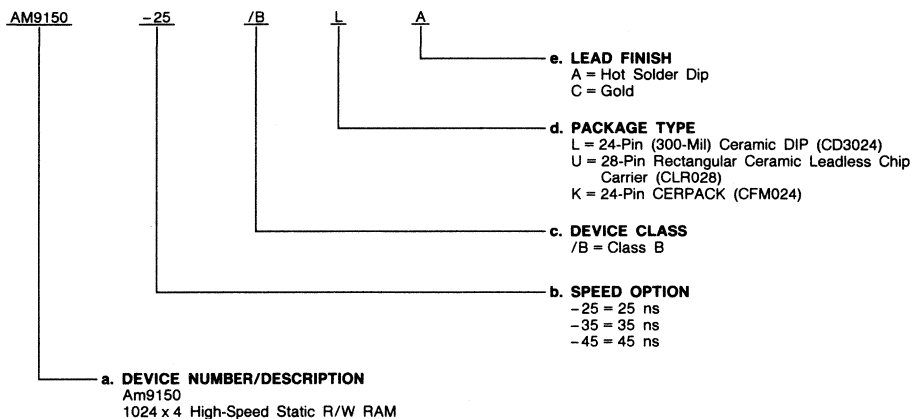
## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**

### APL Products



Valid Combinations	
AM9150-25	/BLA
AM9150-35	/BUC
AM9150-45	/BKA

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

### $A_0 - A_9$ Address (Inputs)

The 10 address inputs select one of the 1024 4-bit words in the RAM.

### $\bar{S}$ Chip Select (Input; Active LOW)

An active-LOW input which selects the device for operation. When  $\bar{S}$  is HIGH, the device is deselected and the outputs will be in a high-impedance state.

### $\bar{W}$ Write Enable (Input; Active LOW)

$\bar{W}$  controls read and write operations. When  $\bar{W}$  is HIGH and  $\bar{G}$  is LOW, data will be present at the data outputs. When  $\bar{W}$  is LOW, data present on the data inputs will be written into the selected memory location. The data outputs will be in a high-impedance state.

### $\bar{R}$ RESET (Input; Active LOW)

An active-Low pulse on  $\bar{R}$  while  $A_0 - A_9$  are stable,  $\bar{S}$  is LOW, and  $\bar{W}$  and  $\bar{G}$  are HIGH resets the whole memory.

### $\bar{G}$ Output Enable (Input; Active LOW)

$\bar{G}$  controls the state of the data outputs in conjunction with  $\bar{S}$  and  $\bar{W}$ .

### $D_0 - D_3$ Data Input

Data inputs to the RAM.

### $Q_0 - Q_3$ Data Output

Data outputs from the RAM. The data outputs will be in a high-impedance state when either  $\bar{S}$  or  $\bar{G}$  are HIGH or  $\bar{W}$  is LOW.

$V_{CC}$  Power Supply +5 Volts

$V_{SS}$  Ground

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage with Respect to Ground .....	-0.5 V to +7.0 V
Signal Voltages with Respect to Ground .....	-3.5 V to +7.0 V
Power Dissipation (Package Limitation) .....	1.2 W
DC Output Current .....	20 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGES (Note 2)

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +70°C
Supply Voltage (V <sub>CC</sub> ) .....	+5.0 V ±10%
Military (M) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+5.0 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Am9150		Am91L50		Unit
			Min.	Max.	Min.	Max.	
I <sub>OH</sub>	Output HIGH Current	V <sub>OH</sub> = 2.4 V	-4		-4		mA
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4 V	12		12		mA
V <sub>IH</sub>	Input HIGH Voltage		2.2	6.0	2.2	6.0	V
V <sub>IL</sub>	Input LOW Voltage		-2.5	0.8	-2.5	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	10	-10	10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled	-10	10	-10	10	μA
C <sub>I</sub>	Input Capacitance	Test Frequency = 1.0 MHz T <sub>A</sub> = 25°C, All Pins at 0 V. V <sub>CC</sub> = 5 V (Note 8)		5		5	pF
C <sub>O</sub>	Output Capacitance			7		7	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	Max V <sub>CC</sub> $\bar{S}$ < V <sub>IL</sub> Output Open	COM'L	180	MIL	130	mA
I <sub>OS</sub>	Output Short Circuit Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> (Notes 7, 8)		180		N/A	
			±50	±300	±50	±300	mA

- Notes: 1. Absolute Maximum Ratings are intended for user guidelines and are not tested.  
 2. For test and correlation purposes, ambient temperature is defined as the "instant-ON" case temperature.  
 3. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance. Output timing reference is 1.5 V.  
 4. The internal write time of the memory is defined by the overlap of  $\bar{S}$  LOW and  $\bar{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing is referenced to the rising edge of the signal that terminates the write.  $\bar{R}$  must be HIGH.  
 5. Transition is measured at 1.5 V on the inputs to V<sub>OH</sub> - 500 mV and V<sub>OL</sub> + 500 mV on the outputs using the load shown in B. under Switching Test Circuits.  
 6.  $\bar{W}$  and  $\bar{R}$  are HIGH for read cycle.  
 7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.  
 8. This parameter is not tested, but guaranteed by characterization.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol		Parameter Description	Am9150-20		Am9150-25 Am91L50-25		Am9150-35 Am91L50-35		Am9150-45 Am91L50-45		Unit
	Standard	Alternate		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>												
1	TAVAV	t <sub>RC</sub>	Read Cycle Time (Note 6)	20		25		35		45		ns
2	TAVQV	t <sub>AA</sub>	Address Access Time		20		25		35		45	ns
3	TSLQV	t <sub>ACS</sub>	Chip Select Access Time		10		15		20		25	ns
4	TGLQV	t <sub>OE</sub>	Output Enable Access Time		10		15		20		25	ns
5	TSLQX	t <sub>CLZ</sub>	Chip Select LOW to Output in Low-Z (Notes 5, 8)	0		0		0		0		ns
6	TSHQZ	t <sub>CHZ</sub>	Chip Select HIGH to Output in Hi-Z (Notes 5, 8)	0	15	0	20	0	25	0	30	ns
7	TGLQX	t <sub>OLZ</sub>	Output Enable LOW to Output in Low-Z (Note 5, 8)	0		0		0		0		ns
8	TGHQZ	t <sub>OHZ</sub>	Output Enable HIGH to Output in Hi-Z (Notes 5, 8)	0	15	0	20	0	25	0	30	ns
9	TAXQX	t <sub>OHA</sub>	Output Hold after Address Change	COM'L.								ns
				MIL.	3		3		3		3	
<b>WRITE CYCLE</b>												
10	TAVAV	t <sub>WC</sub>	Write Cycle Time (Note 4)	20		25		35		45		ns
11	TSLWH	t <sub>CW</sub>	Chip Select LOW to Write Enable HIGH	10		15		20		30		ns
12	TAVWH	t <sub>AW</sub>	Address Valid to End of Write	15		20		30		40		ns
13	TAVWL	t <sub>AS</sub>	Address Valid to Beginning of Write	5		5		5		5		ns
14	TWLWH	t <sub>WP</sub>	Write Pulse Width	10		15		20		30		ns
15	TWHAX	t <sub>WR</sub>	Address Hold after End of Write	5		5		5		5		ns
16	TDVWH	t <sub>DW</sub>	Data in Valid to Write Enable HIGH	10		15		20		30		ns
17	TWHDX	t <sub>DH</sub>	Data Hold after End of Write	5		5		5		5		ns
18	TWLQZ	t <sub>WZ</sub>	Write Enable LOW to Output in Hi-Z (Notes 5, 8)	0	15	0	20	0	25	0	30	ns
19	TWHQX	t <sub>OW</sub>	Write Enable HIGH to Output in Low-Z (Notes 5, 8)	0		0		0		0		ns
<b>RESET CYCLE</b>												
20	TAVAV	t <sub>RRC</sub>	Reset Cycle Time	40		50		70		90		ns
21	TAVRL	t <sub>RSA</sub>	Address Valid to Beginning of Reset	0		0		0		0		ns
22	TWHRL	t <sub>RSW</sub>	Write Enable HIGH to Beginning of Reset	0		0		0		0		ns
23	TSLRL	t <sub>RSCS</sub>	Chip Select LOW to Beginning of Reset	0		0		0		0		ns
24	TRLRH	t <sub>RP</sub>	Reset Pulse Width	20		20		30		40		ns
25	TRHSX	t <sub>RHCS</sub>	Chip Select Hold after End of Reset	0		0		0		0		ns
26	TRHWL	t <sub>RHW</sub>	Write Enable Hold after End of Reset	20		30		40		50		ns
27	TRHAX	t <sub>RHA</sub>	Address Hold after End of Reset	20		30		40		50		ns
28	TRLQZ	t <sub>RHZ</sub>	Reset LOW to Output in Hi-Z (Notes 5, 8)	0	15	0	20	0	25	0	35	ns
29	TRHQX	t <sub>RLZ</sub>	Reset HIGH to Output in Low-Z (Notes 5, 8)	0		0		0		0		ns

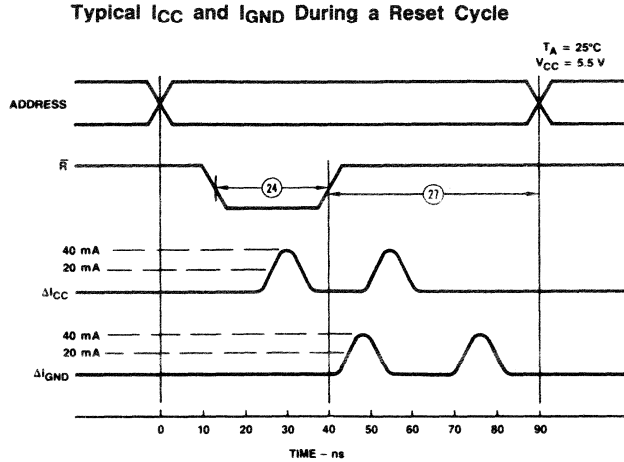
Notes: See notes following DC Characteristics table.

## RESET CYCLE

The reset cycle is initiated by  $\bar{R}$  going LOW for a time  $\geq t_{RP}$ , and is terminated by holding  $\bar{R}$  HIGH for a time  $\geq t_{RHA}$ . The addresses to the device must be stable during the RESET cycle time. The entire contents of the RAM will be reset to ZERO regardless of the address chosen during the cycle. The

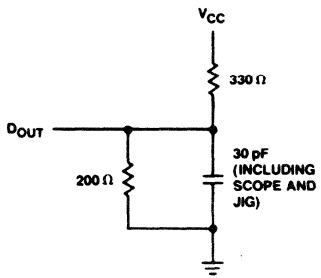
control  $\bar{S}$  must be  $\leq V_{IL}$  maximum, and  $\bar{W}$  must be  $\geq V_{IH}$  minimum and it is recommended that  $\bar{G}$  be  $\geq V_{IH}$  minimum.

The reset cycle is normally associated with current spikes, both at  $V_{CC}$  and GND as shown in the graph. To attenuate the current spikes, an external bypass capacitor (high frequency,  $0.1 \mu\text{F}$ ) for each Am9150 socket is recommended.

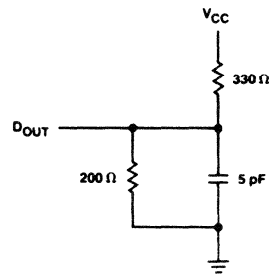


WF009920

## SWITCHING TEST CIRCUITS








A.



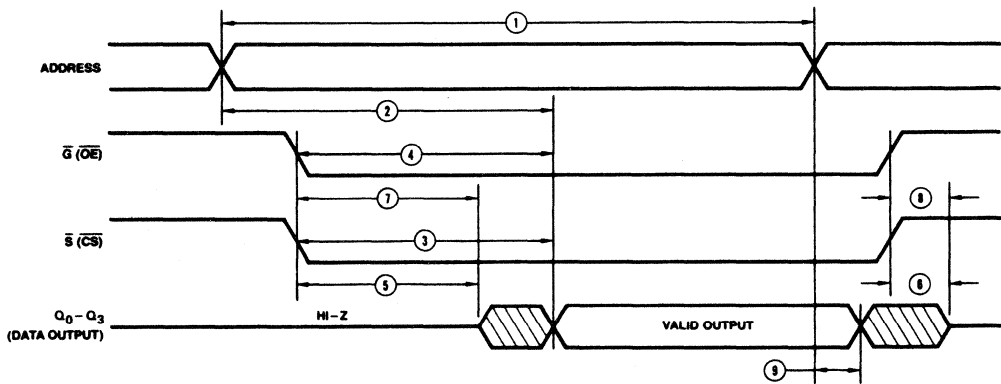
B.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

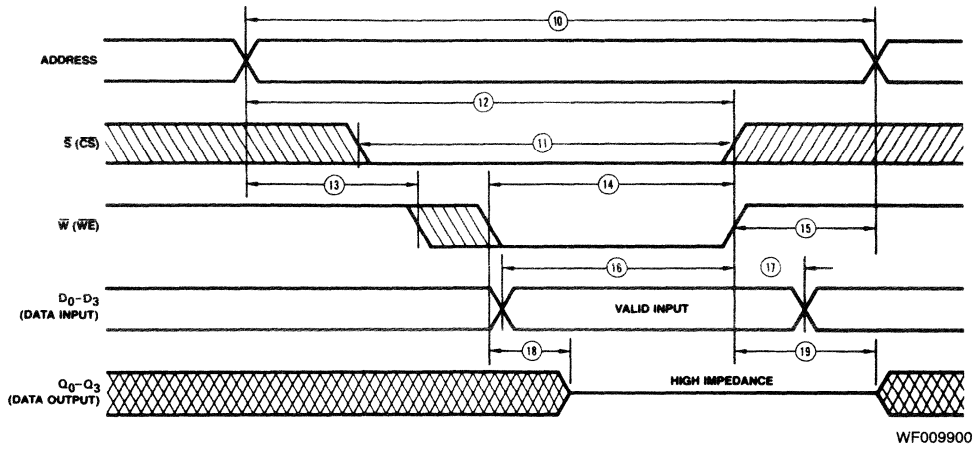
KS000010



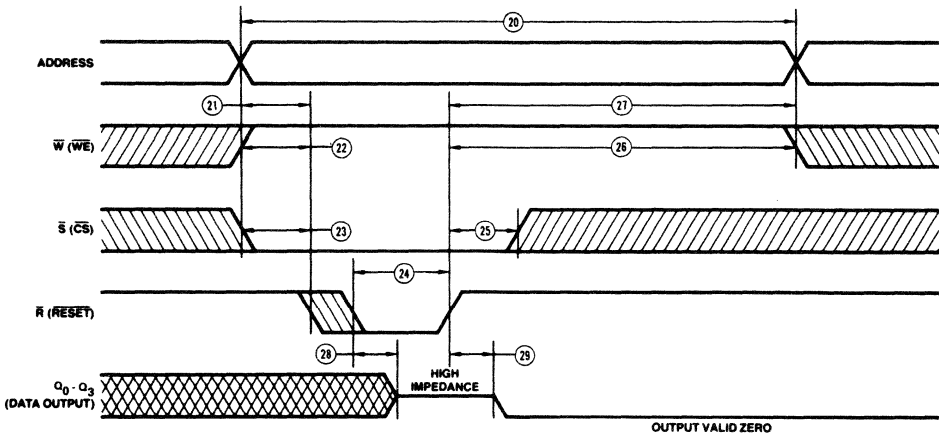
WF009890

**Read Cycle**

SWITCHING WAVEFORMS (Cont'd.)



Write Cycle



Reset Cycle

4

# Am2167

16,384x1 Static RAM



## DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 35 ns maximum
- Automatic power down when deselected
- Low power dissipation
  - Am2167: 660 mW active, 110 mW power down
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL-compatible interface levels
- No power-on current surge

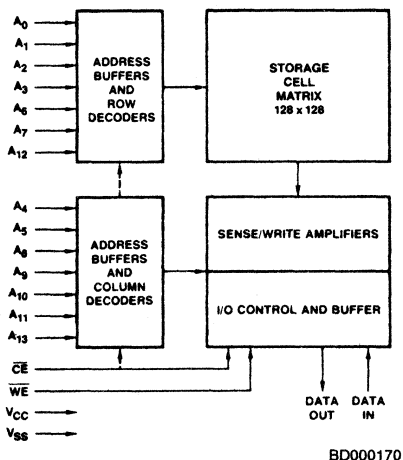
## GENERAL DESCRIPTION

The Am2167 is a high-performance, 16,384-bit, static, read/write, random-access memory. It is organized as 16,384 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to six standard Schottky TTL loads or up to seven standard TTL loads.

Only a single +5-volt power supply is required. When deselected ( $\overline{CE} \geq V_{IH}$ ), the Am2167 automatically enters a power-down mode which reduces power dissipation by 80%.

Data In and Data Out use separate pins and are the same polarity allowing them to be connected together for operation in a common data bus environment. Data Out is a three-state output allowing similar devices to be wire-OR'd together.

## BLOCK DIAGRAM



## PRODUCT SELECTOR GUIDE

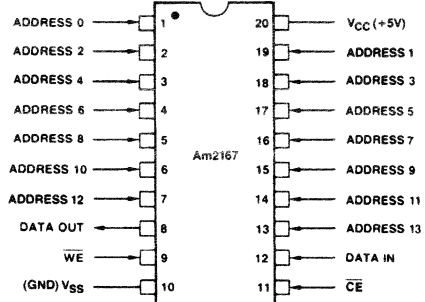
Part Number	Am2167-35	Am2167-45	Am2167-55	Am2167-70
Maximum Access Time (ns)	35	45	55	70
Maximum Active Current (mA)	120	120 (160 mil)	120 (160 mil)	120 (160 mil)
Maximum Standby Current (mA)	20	20 (30 mil)	20 (30 mil)	20 (30 mil)
Full Military Operating Range Version	No	Yes	Yes	Yes



## CONNECTION DIAGRAMS

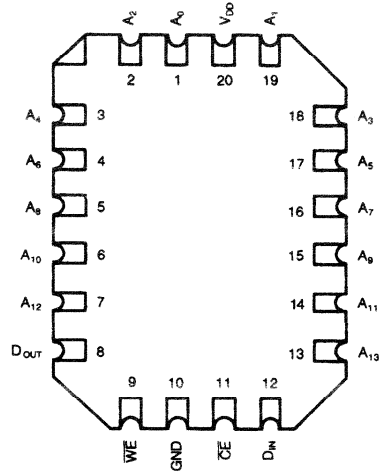
### Top View

**DIPs**



CD009680

**LCC**

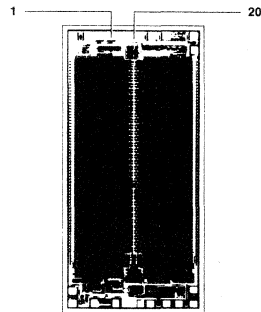


CD009690

Note: Pin 1 is marked for orientation.

## METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A <sub>0</sub>	A <sub>1</sub>
A <sub>1</sub>	A <sub>6</sub>
A <sub>2</sub>	A <sub>2</sub>
A <sub>3</sub>	A <sub>5</sub>
A <sub>4</sub>	A <sub>3</sub>
A <sub>5</sub>	A <sub>0</sub>
A <sub>6</sub>	A <sub>4</sub>
A <sub>7</sub>	A <sub>13</sub>
A <sub>8</sub>	A <sub>10</sub>
A <sub>9</sub>	A <sub>6</sub>
A <sub>10</sub>	A <sub>11</sub>
A <sub>11</sub>	A <sub>9</sub>
A <sub>12</sub>	A <sub>12</sub>
A <sub>13</sub>	A <sub>7</sub>



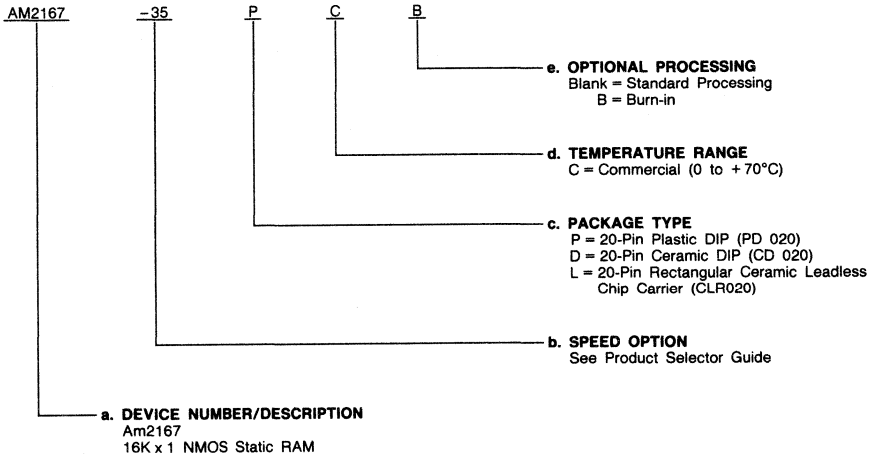
Die Size: 0.121" x 0.249"

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM2167-35	PC, PCB, DC, DCB, LC, LCB
AM2167-45	PD, PCB, DC, DCB
AM2167-55	
AM2167-70	

#### Valid Combinations

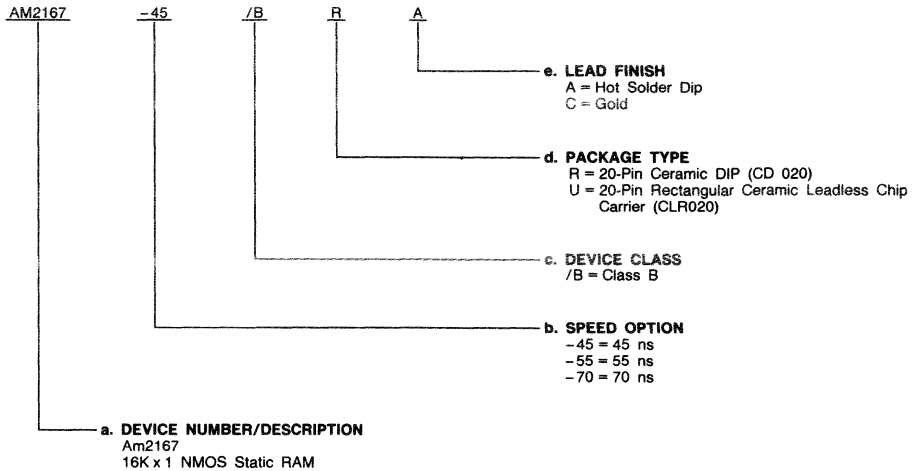
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM2167-45	/BRA, /BUA
AM2167-55	
AM2167-70	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

#### **A<sub>0</sub> - A<sub>13</sub> Address (Inputs)**

The address input lines select the RAM location to be read or written.

#### **CE Chip Enable (Input, Active LOW)**

The Chip Enable selects the memory device.

#### **WE Write Enable (Input, Active LOW)**

When Write Enable is LOW and Chip Enable is also LOW, data is written into the location specified on the address pins.

#### **D<sub>IN</sub> Data (Input)**

This pin issued for entering data during write operation.

#### **D<sub>OUT</sub> Data (Output, Three State)**

This pin is three state during write operation. It becomes active when  $\overline{CE}$  is LOW and  $\overline{WE}$  is HIGH.

#### **V<sub>CC</sub> Power Supply**

#### **V<sub>SS</sub> Ground**

4

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
Signal Voltages with Respect to Ground .....	-3.5 V to +7.0 V
Power Dissipation .....	1.2 W
DC Output Current .....	50 mA

Maximum rating are to be for system design reference, parameters given may not be 100% tested by AMD.

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGES (Note 4)

Commercial (C) Devices	Ambient Temperature (T <sub>A</sub> ) .....	0 to +70°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V
Military (M) Devices	Ambient Temperature (T <sub>A</sub> ) .....	-55 to +125°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted) (Note 4)

Parameter Symbol	Parameter Description	Test Conditions	Am2167-35		Am2167-45, Am2167-55, Am2167-70		Unit	
			Min.	Max.	Min.	Max.		
I <sub>OH</sub>	Output HIGH Current	V <sub>OH</sub> = 2.4 V	V <sub>CC</sub> = 4.5 V	-4		-4	mA	
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4 V	COM'L	16		16	mA	
			MIL	12		12		
V <sub>IH</sub>	Input HIGH Voltage			2.2	6.0	2.2	6.0	V
V <sub>IL</sub>	Input LOW Voltage			-2.5	0.8	-2.5	0.8	V
I <sub>Ix</sub>	Input Load Current	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-10	10	-10	10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled		-50	50	-50	50	μA
C <sub>1</sub>	Input Capacitance	Test Frequency = 1.0 MHz			5		5	pF
C <sub>O</sub>	Output Capacitance	T <sub>A</sub> = 25°C, All pins at 0 V, V <sub>CC</sub> = 5 V (Note 9)			6		6	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	Max V <sub>CC</sub> , CE ≤ V <sub>IL</sub> Output Open	COM'L		120		120	mA
			MIL		N/A		160	
I <sub>SB</sub>	Automatic $\overline{CE}$ Power Down Current	MAX V <sub>CC</sub> , (CE ≥ V <sub>IH</sub> ) (Note 3)	COM'L		20		20	mA
			MIL		N/A		30	

- Notes: 1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power up. Otherwise I<sub>SB</sub> will exceed values given.
4. For test and correlation purposes, ambient temperature is defined as the "Instant-on" case temperature.
5. The device must be selected during the previous cycle. Otherwise t<sub>AA</sub> and t<sub>RC</sub> are equivalent to t<sub>ACS</sub>.
6. Transition is measured ±500 mV from steady state voltage with load specified in Figure 2 for t<sub>HZ</sub>, t<sub>LZ</sub>, t<sub>OW</sub> and t<sub>wz</sub>.
7.  $\overline{WE}$  is HIGH for read cycle.
8. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
9. Parameter not 100% tested. Guaranteed by characterization.

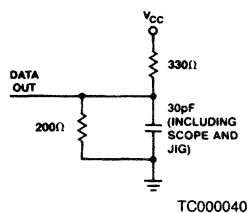
**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (Note 1) (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am2167-35		Am2167-45		Am2167-55		Am2167-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>											
1	t <sub>RC</sub>	Address Valid to Address Do Not Care Time (Read Cycle Time) (Note 5)	30		40		50		70		ns
2	t <sub>AA</sub>	Address Valid to Data Out Valid Delay (Address Access Time) (Note 5)		30		40		50		70	ns
3	t <sub>ACS</sub>	Chip Enable LOW to Data Out Valid (Chip Enable Access Time)		35		45		55		70	ns
4	t <sub>LZ</sub>	Chip Enable LOW to Data Out On (Notes 6, 9)	5		5		5		5		ns
5	t <sub>HZ</sub>	Chip Enable HIGH to Data Out Off (Notes 6, 9)	0	20	0	25	0	30	0	40	ns
6	t <sub>OH</sub>	Output hold time from address change	COM'L	3		3		3		3	ns
			MIL	1		1		1		1	ns
7	t <sub>PD</sub>	Chip Enable HIGH to Power Down Delay (Note 9)		25		30		30		55	ns
8	t <sub>PU</sub>	Chip Enable LOW to Power Up Delay (Note 9)	0		0		0		0		ns
<b>WRITE CYCLE</b>											
9	t <sub>WC</sub>	Address Valid to Address Do Not Care (Write Cycle Time)	30		40		50		70		ns
10	t <sub>WP</sub>	Write Enable LOW to Write Enable HIGH (Note 2)	20		20		25		40		ns
11	t <sub>WR</sub>	Write Enable HIGH to Address	0		0		0		0		ns
12	t <sub>WZ</sub>	Write Enable LOW to Output in HIGH Z (Notes 6 & 9)	0	20	0	20	0	25	0	35	ns
13	t <sub>DW</sub>	Data In Valid to Write Enable HIGH	15		15		20		30		ns
14	t <sub>DH</sub>	Data Hold Time	5		5		5		5		ns
15	t <sub>AS1</sub>	Address Valid to Write Enable LOW (WE Controlled Write)	5		5		5		5		ns
	t <sub>AS2</sub>	Address Valid to Write Enable LOW (CE Controlled Write)	0		0		0		0		ns
16	t <sub>CW</sub>	Chip Enable LOW to Write Enable HIGH (Note 2)	30		40		50		55		ns
17	t <sub>OW</sub>	Write Enable HIGH to Output in LOW Z (Notes 6 & 9)	0		0		0		0		ns
18	t <sub>AW</sub>	Address Valid to End of Write	30		40		50		70		ns

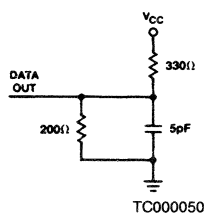
Notes: See notes following DC Characteristics table.

4

**SWITCHING TEST CIRCUITS**



**A. Output Load**



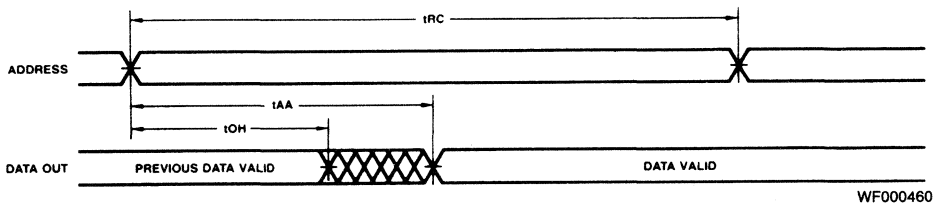
**B. Output Load for t<sub>HZ</sub>, t<sub>LZ</sub>, t<sub>OW</sub>, t<sub>WZ</sub>**

# SWITCHING WAVEFORMS

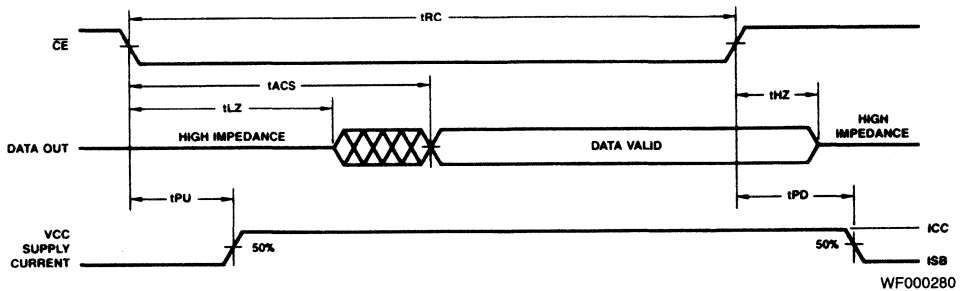
## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



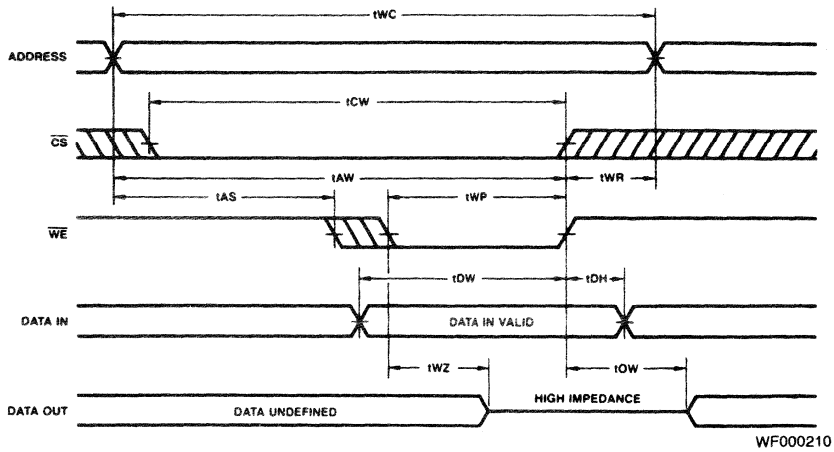
**Read Cycle No. 1 (Notes 5, 7)**



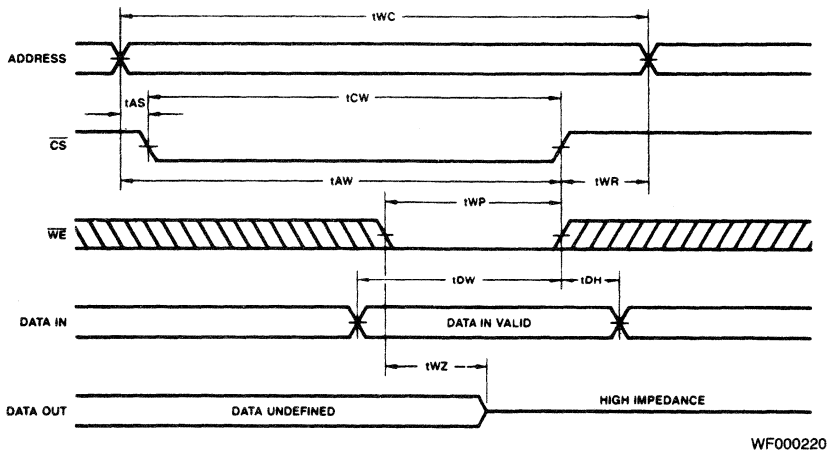
**Read Cycle No. 2 (Notes 7, 8)**

Notes: See notes following DC Characteristics table.

SWITCHING WAVEFORMS (Cont'd.)



Write Cycle No. 1 ( $\overline{WE}$  Controlled)

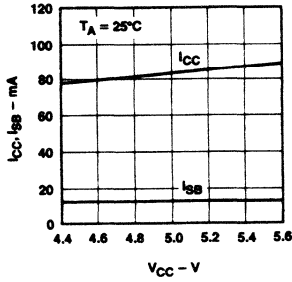


Write Cycle No. 2 ( $\overline{CE}$  Controlled)

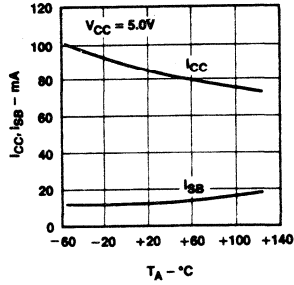
Note: If  $\overline{CE}$  goes high simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

## TYPICAL PERFORMANCE CURVES

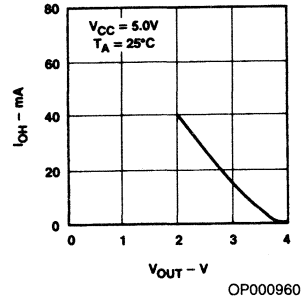
**Supply Current  
versus Supply Voltage**



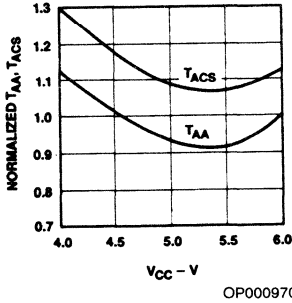
**Supply Current  
versus Ambient Temperature**



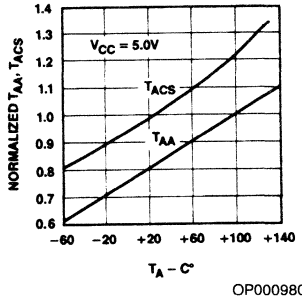
**Output Source Current  
versus Output Voltage**



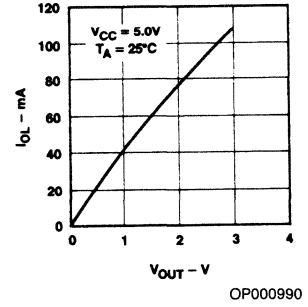
**Normalized Access Time  
versus Supply Voltage**



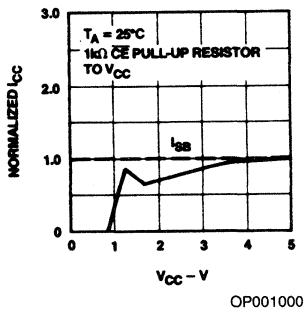
**Normalized Access Time  
versus Ambient Temperature**



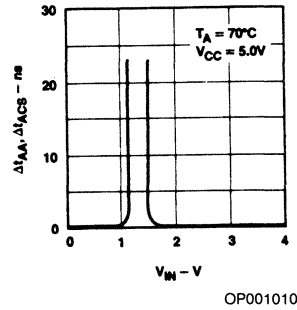
**Output Sink Current  
versus Output Voltage**



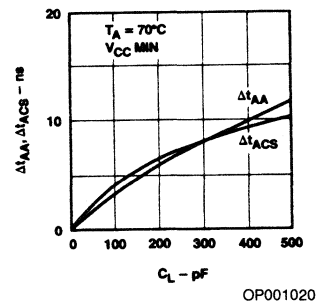
**Typical Power-On Current  
versus Power Supply**



**Access Time Change  
versus Input Voltage**



**Access Time Change  
versus Output Loading**





# Am2168/Am2169

4096 X 4 Static R/W Random-Access Memory



## DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 40 ns
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Automatic power down when deselected (Am2168)
- Power dissipation
  - Am2168: 660 mW active, 165 mW standby
  - Am2169: 660 mW
- Standard 20-pin, .300 inch dual-in-line package
- Standard 20-pin rectangular ceramic leadless chip carrier
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL-compatible interface levels

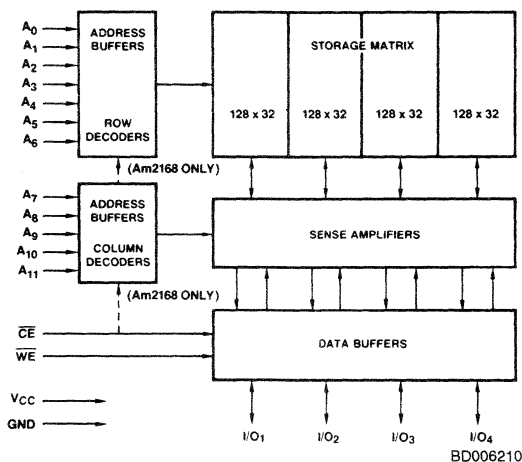
## GENERAL DESCRIPTION

The Am2168 and Am2169 are high-performance, static, N-channel, read/write, random-access memories organized as 4096 words of 4 bits. Operation is from a single 5 V supply, and all input/output levels are identical to standard TTL specifications. The Am2168 and Am2169 are the same except that the Am2168 offers an automatic Chip Enable ( $\overline{CE}$ ) power-down feature.

The Am2168 remains in a low-power standby mode as long as  $\overline{CE}$  remains HIGH, thus reducing its power requirements from 660 mW to 165 mW maximum.

The data read out is not destructive and has the same polarity as the input data. The device is packaged in either a .300 slim DIP or 20-pin leadless chip carrier. The outputs of similar devices can be OR-tied and easy selection obtained by use of the  $\overline{CE}$ .

## BLOCK DIAGRAM



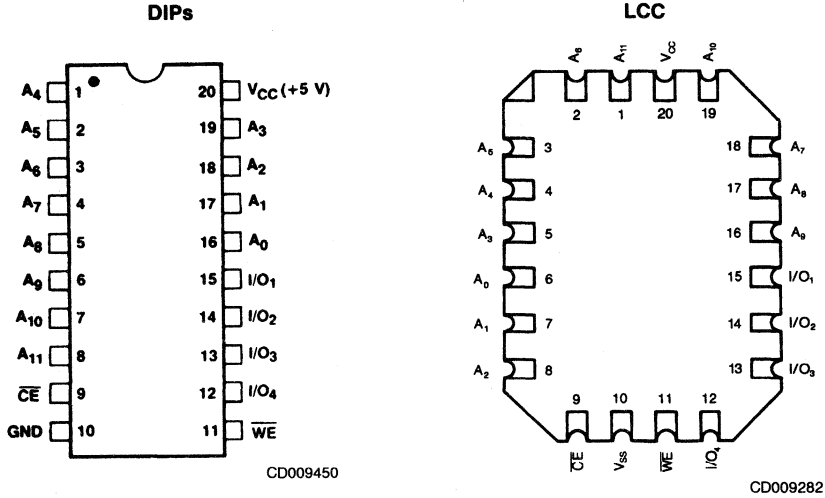
4

## PRODUCT SELECTOR GUIDE

Part Number		Am2168-35	Am2168-45	Am2169-40	Am2168-55	Am2169-50	Am2168-70	Am2169-70
Maximum Access Time (ns)		35	45	40	55	50	70	70
0 to +70°C	$I_{CC}$ (mA)	120	120	120	120	120	120	120
	$I_{SB}^*$ (mA)	30	30	N/A	30	N/A	30	N/A
-55 to +125°C	$I_{CC}$ (mA)	N/A	160	N/A	160	160	160	160
	$I_{SB}^*$ (mA)	N/A	30	N/A	30	N/A	30	N/A

\*Am2168

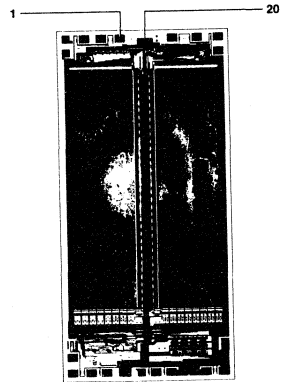
## CONNECTION DIAGRAMS Top View



Note: Pin 1 is marked for orientation.

## METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A <sub>0</sub>	A <sub>0</sub>
A <sub>1</sub>	A <sub>1</sub>
A <sub>2</sub>	A <sub>2</sub>
A <sub>3</sub>	A <sub>3</sub>
A <sub>4</sub>	A <sub>4</sub>
A <sub>5</sub>	A <sub>5</sub>
A <sub>6</sub>	A <sub>6</sub>
A <sub>7</sub>	A <sub>7</sub>
A <sub>8</sub>	A <sub>8</sub>
A <sub>9</sub>	A <sub>11</sub>
A <sub>10</sub>	A <sub>10</sub>
A <sub>11</sub>	A <sub>9</sub>



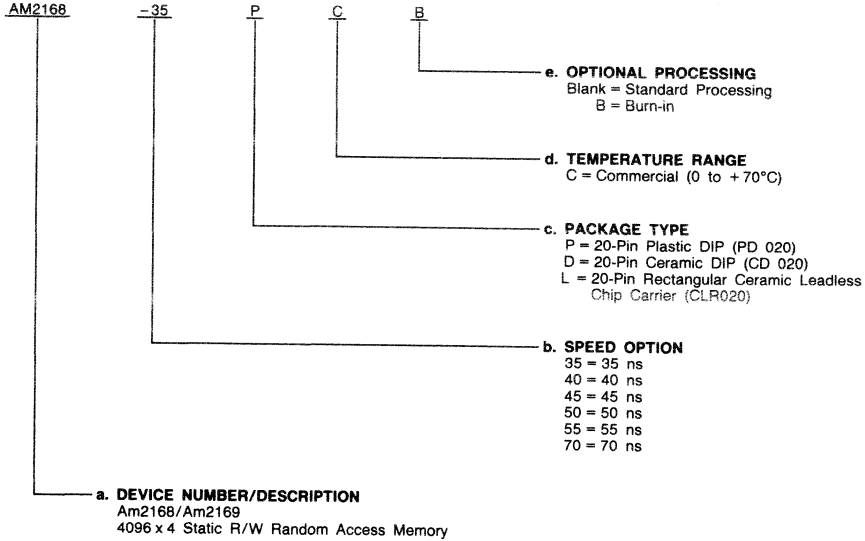
Die Size: 0.123" x 0.252"

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM2168-35	PC, PCB, DC,
AM2169-40	DCB, LC, LCB
AM2168-45	PC, PCB, DC, DCB
AM2168-55	
AM2169-50	
AM2168-70	
AM2169-70	

#### Valid Combinations

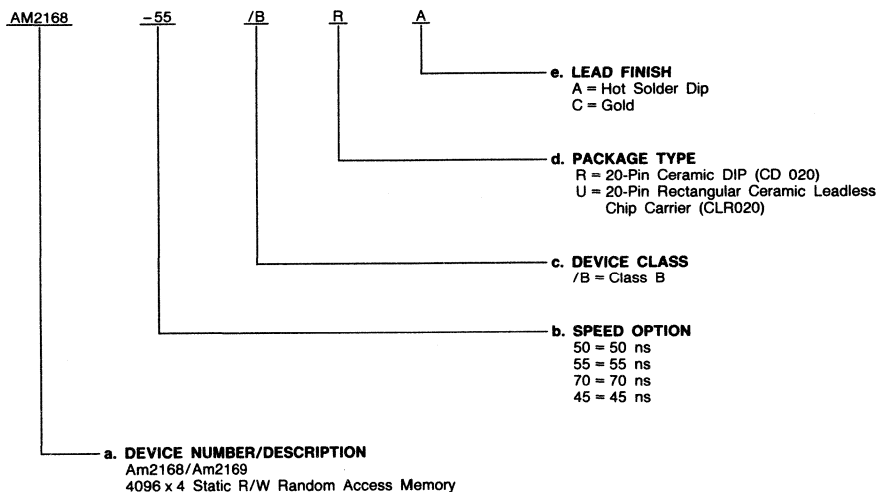
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM2168-45	/BRA, /BUA
AM2168-55	
AM2169-50	
AM2168-70	
AM2169-70	
AM2168-45	
AM2168-55	
AM2169-50	
AM2168-70	
AM2169-70	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>11</sub> Address Inputs (Inputs)

The address input lines select the RAM location to be read or written.

### CE Chip Enable (Input, Active LOW)

The Chip Enable selects the memory device.

### WE Write Enable (Input, Active LOW)

When Write Enable is LOW and Chip Enable is also LOW, data is written into the location specified on the address pins.

### I/O<sub>1</sub> - I/O<sub>4</sub> Data In/Out Bus (Bidirectional Active HIGH)

These I/O lines provide the path for data to be read from or written to the selected memory location.

### V<sub>CC</sub> Power Supply

### V<sub>SS</sub> Ground

## ABSOLUTE MAXIMUM RATINGS\*

Supply Voltage	-0.5 V to +7.0 V
All Signal Voltages	-3.5 V to +7.0 V
DC Output Current	20 mA
Power Dissipation	
Cerdip & Leadless Packages	1.2 W
Plastic Packages	0.7 W
Ambient Temperature with Power Applied	
Cerdip & Leadless Packages	-55 to +125°C
Plastic Packages	-10 to +85°C
Storage Temperature	
Cerdip & Leadless Packages	-65 to +150°C
Plastic Packages	-55 to +150°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

\*Maximum ratings are for system design reference; parameters given may not be 100% tested.

## OPERATING RANGES (Note 4)

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> )	0 to +70°C
Supply Voltage (V <sub>CC</sub> )	4.5 V to +5.5 V
Military (M) Devices	
Ambient Temperature (T <sub>A</sub> )	-55 to +125°C
Supply Voltage (V <sub>CC</sub> )	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted) (Note 4)

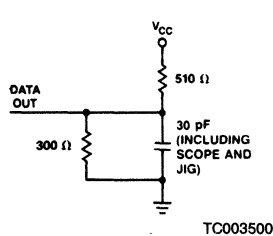
Parameter Symbol	Parameter Description	Test Conditions	Am2168-35, -45, & -40		Am2168-55 & -70 Am2169-50 & -70		Unit	
			Min.	Max.	Min.	Max.		
I <sub>OH</sub>	Output HIGH Current	V <sub>OH</sub> = 2.4 V	V <sub>CC</sub> = 4.5 V		-4	-4	mA	
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4 V	COM'L		8	8	mA	
			MIL		8	8		
V <sub>IH</sub>	Input HIGH Voltage		2.2	6.0	2.2	6.0	V	
V <sub>IL</sub>	Input LOW Voltage	Note 3	-0.5	0.8	-0.5	0.8	V	
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	10	-10	10	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled	-50	50	-50	50	μA	
C <sub>1</sub>	Input Capacitance	Test Frequency = 1.0 MHz		5		5	pF	
C <sub>I/O</sub>	Input/Output Capacitance	T <sub>A</sub> = 25°C, All Pins at 0 V, V <sub>CC</sub> = 5 V (Note 5)		7		7		
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	Max. V <sub>CC</sub> , CE ≤ V <sub>IL</sub> Output Open	COM'L			120	120	mA
			MIL			N/A	160	
I <sub>SB</sub>	Automatic $\overline{CE}$ Power Down Current (Am2168 Only)	Max. V <sub>CC</sub> , (CE ≥ V <sub>IH</sub> )	COM'L			30	30	mA
			MIL			N/A	30	

- Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance. Output timing reference is 1.5 V.
  2. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
  3. V<sub>IL</sub> voltages of less than -0.5 V on the I/O pins will cause the output current to exceed the maximum rating and thus should not exceed 30 seconds in duration.
  4. For test and correlation purposes, ambient temperature is defined as the "Instant-on" case temperature.
  5. At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> and t<sub>WZ</sub> is less than t<sub>OW</sub> for all devices. Transition is measured at 1.5 V on the input to V<sub>OH</sub> - 500 mV and V<sub>OL</sub> + 500 mV on the outputs using the load shown in B. under Switching Test Circuits. C<sub>L</sub> = 5 pF.
  6. Not 100% tested parameter; parameter guaranteed by characterization.

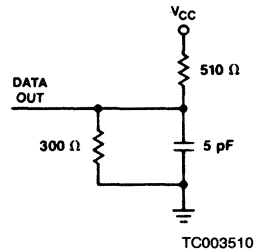
**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 1)

No.	Parameter Symbol	Parameter Description	Am2168-35		Am2168-45, Am2169-40		Am2168-55, Am2169-50		Am2168-70, Am2169-70		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
<b>READ CYCLE</b>												
1	$t_{RC}$	Address Valid to Address Do Not Care Time (Read Cycle Time)	35		40		50		70		ns	
2	$t_{AA}$	Address Valid to Data Out Valid Delay (Address Access Time)		35		40		50		70	ns	
3	$t_{ACS}$	Chip Enable LOW to Data Out Valid (Chip Enable Access Time)	Am2168	35	Am2169	45	Am2168	55	Am2169	70	ns	
4	$t_{LZ}$	Chip Enable LOW to Data Out On	Am2168	(Notes 4, 5)	5	5	Am2168	5	Am2169	5		
			Am2169			2	Am2168	2	Am2169	2		
5	$t_{HZ}$	Chip Enable HIGH to Data Out Off	(Notes 4, 5)	0	20	0	20	0	25	0	30	ns
6	$t_{OH}$	Output hold time from address change	COM'L	3	MIL	3		3		3		
						1		1		1		
7	$t_{PD}$	Chip Enable HIGH to Power-Down Delay	Am2168	(Note 5)		35		45		55	70	ns
8	$t_{PU}$	Chip Enable LOW to Power-Up Delay	Am2168	(Note 5)	0		0		0		0	ns
<b>WRITE CYCLE</b>												
9	$t_{WC}$	Address Valid to Address Do Not Care (Write Cycle Time)	35		40		50		70		ns	
10	$t_{WP}$	Write Enable LOW to Write Enable HIGH	(Note 2)	30		35		45		65	ns	
11	$t_{WR}$	Write Enable HIGH to Address Do Not Care		0		0		0		0	ns	
12	$t_{WZ}$	Write Enable LOW to Output in Hi-Z	(Notes 4, 5)	0	15	0	15	0	20	0	25	ns
13	$t_{DW}$	Data In Valid to Write Enable HIGH		20		20		25		35	ns	
14	$t_{DH}$	Data Hold Time		5		5		5		5	ns	
15	$t_{AS}$	Address Valid to Write Enable LOW		0		0		0		0	ns	
16	$t_{CW}$	Chip Enable LOW to Write Enable HIGH	(Note 2)	30		35		45		65	ns	
17	$t_{OW}$	Write Enable HIGH to Output in Low-Z	(Notes 4, 5)	0		0		0		0	ns	
18	$t_{AW}$	Address Valid to End of Write		30		35		45		65	ns	

**SWITCHING TEST CIRCUITS**









**A. Output Load**



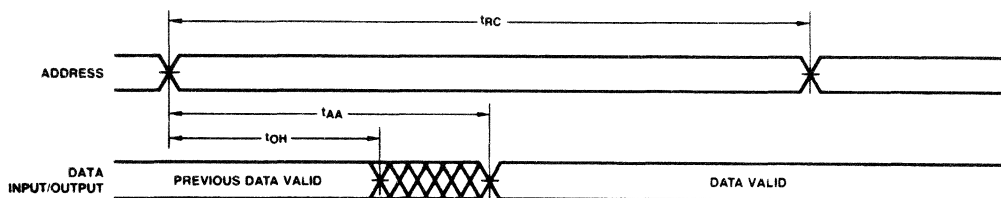
**B. Output Load for  $t_{HZ}$ ,  $t_{LZ}$ ,  $t_{OW}$ ,  $t_{WZ}$**

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
 	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

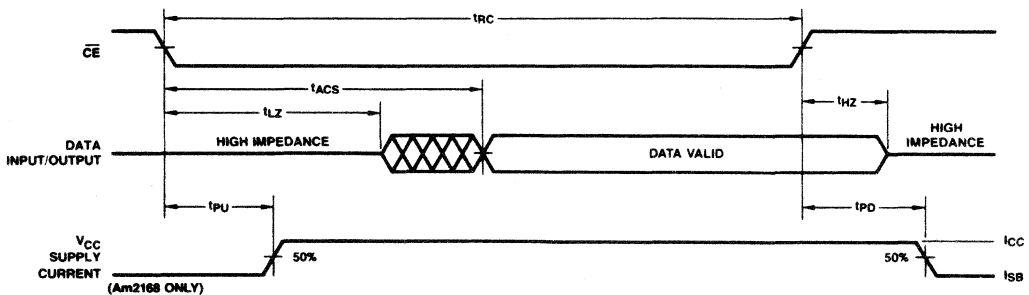
KS000010



WF021270

**Read Cycle No. 1 ( $\overline{WE}$  HIGH,  $\overline{CE}$  LOW)**

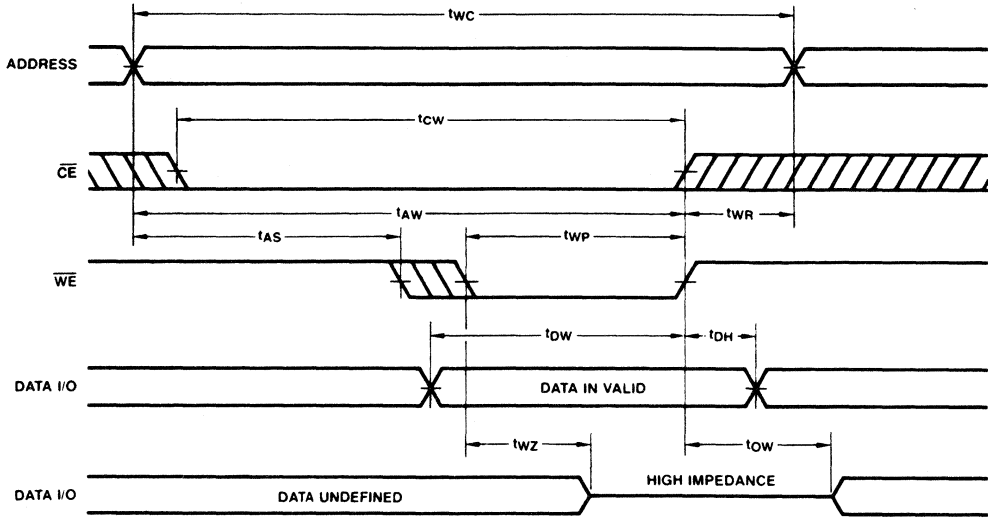
4



WF021280

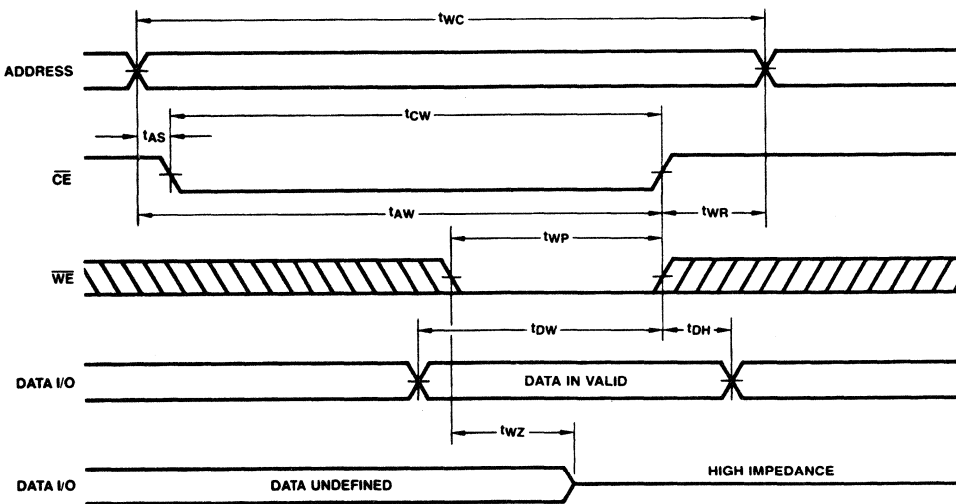
**Read Cycle No. 2 ( $\overline{WE}$  HIGH, Address Valid Prior to  $\overline{CE}$  Transition to LOW)**

SWITCHING WAVEFORMS (Cont'd.)



WF021970

Write Cycle No. 1 ( $\overline{WE}$  Controlled)



WF021300

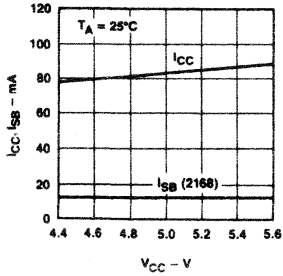
Write Cycle No. 2 ( $\overline{CE}$  Controlled)

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.



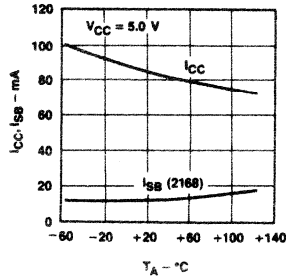
## TYPICAL PERFORMANCE CURVES

**Supply Current  
versus Supply Voltage**



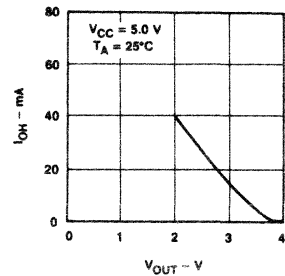
OP001980

**Supply Current  
versus Ambient Temperature**



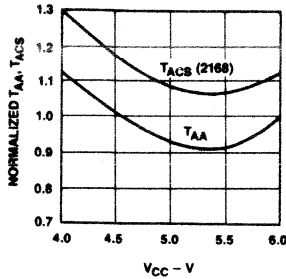
OP001990

**Output Source Current  
versus Output Voltage**



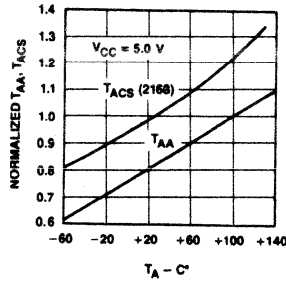
OP002000

**Normalized Access Time  
versus Supply Voltage**



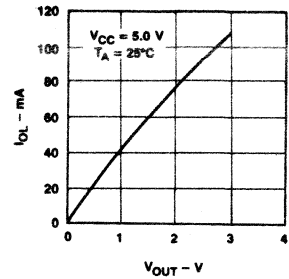
OP002010

**Normalized Access Time  
versus Ambient Temperature**



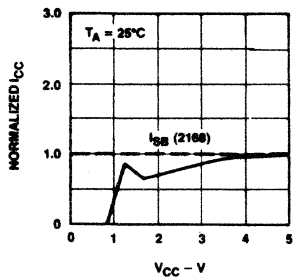
OP002020

**Output Sink Current  
versus Output Voltage**



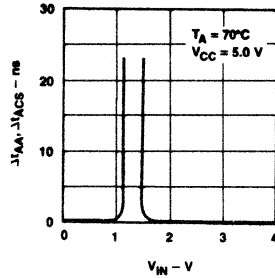
OP002030

**Typical Power-On Current  
versus Power Supply**



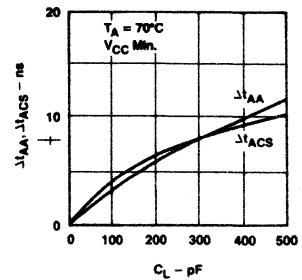
OP002040

**Access Time Change  
versus Input Voltage**



OP002050

**Access Time Change  
versus Output Loading**



OP002060

4

# Am9128

## 2048x8 Static RAM

### DISTINCTIVE CHARACTERISTICS

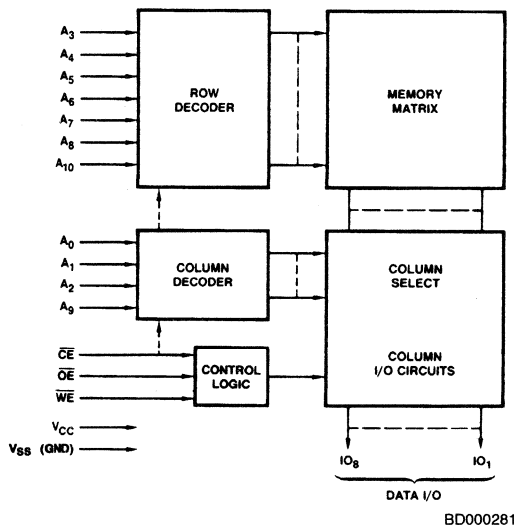
- Logic voltage levels compatible with TTL
- Three-state output buffers and common I/O
- $I_{CC}$  Max., as low as 100 mA
- $t_{AA}/t_{ACS}$  as low as 70 ns
- Power-Down mode ( $I_{SB}$  as low as 15 mA)

### GENERAL DESCRIPTION

The Am9128 is a 16,384-bit Static Random Access Memory organized as 2048 words of 8 bits. It uses fully static circuitry, requiring no clocks or refresh to operate. Directly TTL-compatible inputs and outputs and operation from a single +5 V supply simplify system

designs. Common data I/O pins using three-state outputs are provided. The Am9128 is available in an industry-standard 24-pin DIP package with 0.6-inch pin row spacing. The Am9128 uses the JEDEC standard pinout for byte-wide memories (compatible to 16K EPROMs).

### BLOCK DIAGRAM

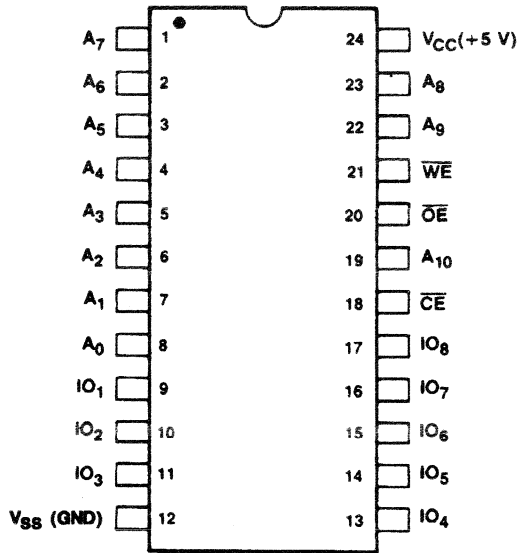


### PRODUCT SELECTOR GUIDE

Part Number	Am9128-70	Am9128-90	Am9128-10	Am9128-12	Am9128-15	Am9128-20	
Maximum Access Time (ns)	70	90	100	120	150	200	
Maximum Operating Current (mA)	0 to 70°C	140	N/A	120	N/A	100	140
	-55° to 125°C	N/A	180	N/A	150	150	150
Maximum Standby Current (mA)	0° to 70°C	30	N/A	15	N/A	15	30
	-55° to 125°C	N/A	30	N/A	30	30	30

**CONNECTION DIAGRAMS**  
**Top View**

**DIPs**

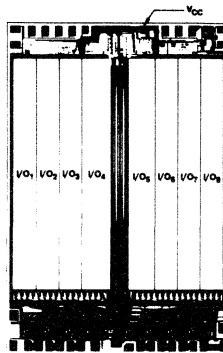


CD000121

Note: Pin 1 is marked for orientation.

**METALLIZATION AND PAD LAYOUT**

Address Designators	
External	Internal
A <sub>3</sub>	AX <sub>0</sub>
A <sub>4</sub>	AX <sub>1</sub>
A <sub>5</sub>	AX <sub>2</sub>
A <sub>6</sub>	AX <sub>3</sub>
A <sub>7</sub>	AX <sub>4</sub>
A <sub>8</sub>	AX <sub>5</sub>
A <sub>10</sub>	AX <sub>6</sub>
A <sub>0</sub>	AY <sub>0</sub>
A <sub>1</sub>	AY <sub>1</sub>
A <sub>2</sub>	AY <sub>2</sub>
A <sub>9</sub>	AY <sub>3</sub>



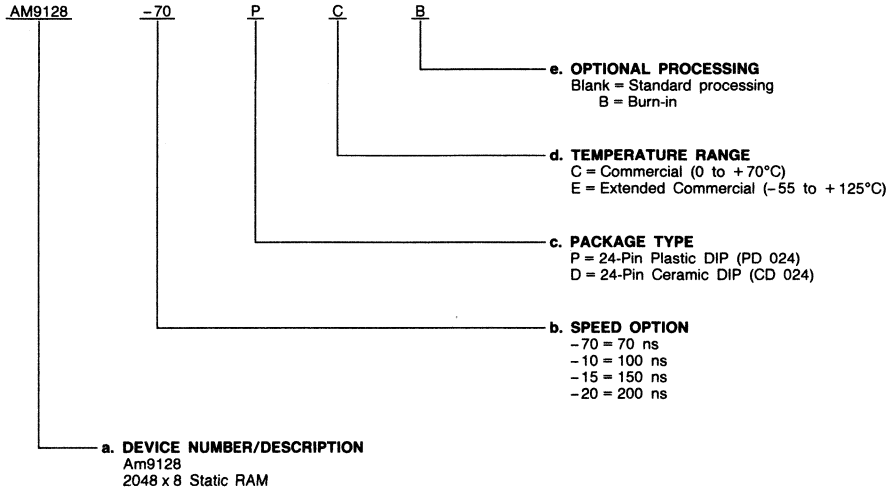
DIE SIZE: 0.162" x 0.240"

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM9128-70	PC, DC, DCB, DE, DEB
AM9128-10	
AM9128-15	
AM9128-20	

#### Valid Combinations

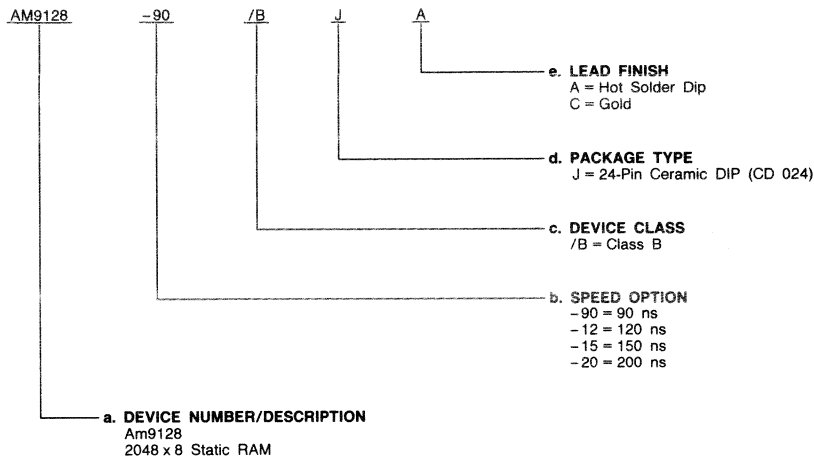
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM9128-90	/BJA, /BJC
AM9128-12	
AM9128-15	
AM9128-20	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11

## PIN DESCRIPTION

#### $A_0 - A_{10}$ Addresses (Input)

The 10-bit field presented at the address inputs selects one of the 2048 memory locations to be read from — or written into — via the data lines.

#### $I/O_1 - I/O_8$ Data In/Out Port (Input/Output)

If  $\overline{WE}$  is LOW, the data represented on the I/O lines can be written into the selected memory location. If  $\overline{WE}$  is HIGH, the I/O lines represent the data read from the selected memory location.

#### $\overline{CE}$ Chip Enable (Input, Active LOW)

Read and Write cycles can be executed only when  $\overline{CE}$  is LOW.

#### $\overline{WE}$ Write Enable (Input, Active LOW)

Data is written into the memory if  $\overline{WE}$  is LOW and read from the memory if  $\overline{WE}$  is HIGH.

#### $\overline{OE}$ Output Enable (Input, Active LOW)

Read cycles can be executed only when  $\overline{OE}$  is LOW.

## ABSOLUTE MAXIMUM RATINGS (Note 11)

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
Signal Voltage with Respect to Ground .....	-3.0 V to +7.0 V
Power Dissipation .....	1.0 W
DC Output Current .....	10 mA

\*Maximum ratings are to be for system design reference, parameters given may not be 100% tested by AMD.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES (Note 3)

Commercial (C) Devices	Ambient Temperature ( $T_A$ ) .....	0 to +70°C
	Supply Voltage ( $V_{CC}$ ) .....	+4.5 V to +5.5 V
Military* (M) and Extended Commercial (E) Devices	Case Temperature ( $T_A$ ) .....	-55 to +125°C
	Supply Voltage ( $V_{CC}$ ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted) (Note 3)

Parameter Symbol	Parameter Description	Test Conditions	Am9128-90 Am9128-10		Am9128-15		Am9128-70 Am9128-12 Am9128-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>OH</sub>	Output HIGH Current	V <sub>OH</sub> = 2.4 V	-2	4	-2	4	-2	4	mA
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4 V							
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 1.0	2.0	V <sub>CC</sub> + 1.0	2.0	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>Ix</sub>	Input Load Current	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		10		10		10	μA
I <sub>OZ</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled		10		10		10	μA
C <sub>IN</sub>	Input Capacitance (Note 12)	Test Frequency = 1.0 MHz, T <sub>A</sub> = 25°C, All pins at 0	V <sub>CC</sub> = 5.0 V	6		6		6	pF
C <sub>I/O</sub>	Input/Output Capacitance (Note 12)			7		7		7	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	Max. V <sub>CC</sub> , $\overline{CE} \leq V_{IL}$ Outputs Open	COM'L	120		100	140		mA
			MIL/E-COM'L	180		150	150		
I <sub>SB</sub>	Automatic $\overline{CE}$ Power Down Current	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$	COM'L	15		15	30		mA
			MIL/E-COM'L	30		30	30		
I <sub>PO</sub>	Peak Power On Current (Note 12)	V <sub>CC</sub> = GND to V <sub>CC</sub> Max. $\overline{CE} \geq V_{IH}$ (Note 2)	COM'L	15		15	30		mA
			MIL/E-COM'L	30		30	30		

- Notes: 1. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. A pull up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required during power up to keep the device deselected, otherwise I<sub>PO</sub> will exceed values given.
3. For test and correlation purposes, ambient temperature is defined as the "Instant-on" case temperature.
4. At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub>.
5.  $\overline{WE}$  is HIGH for read cycle.
6. Device is continuously selected,  $\overline{CE} = V_{IL}$ .
7. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
8.  $\overline{OE} = V_{IL}$ .
9. C<sub>L</sub> = 30 pF.
10. Transition is measured from 1.5 V on the input to V<sub>OH</sub> - 500 mV and V<sub>OL</sub> + 500 mV on the outputs using the load shown in Switching Test Circuits. C<sub>L</sub> = 5 pF.
11. The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling, and use to avoid exposure to excessive voltages.
12. The parameter is guaranteed by characterization, but is not tested.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted.)

**Am9128-70, -90, -10**

No.	Parameter Symbol	Parameter Description	Am9128-70		Am9128-90		Am9128-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>									
1	t <sub>RC</sub>	Read Cycle Time	70		90		100		ns
2	t <sub>ACC</sub>	Address Access Time (Note 9)		70		90		100	ns
3	t <sub>ACS</sub>	Chip Select Access Time (Note 9)		70		90		100	ns
4	t <sub>OE</sub>	Output Enable Time (Note 9)	COM'L		N/A		50		ns
			MIL		N/A		N/A		
5	t <sub>OH</sub>	Output Hold Time from Address Change	5		5		5		ns
6	t <sub>CLZ</sub>	Output in Low-Z from $\overline{CE}$ (Notes 4, 10, 12)	5		5		5		ns
7	t <sub>CHZ</sub>	Output in Hi-Z from $\overline{CE}$ (Notes 4, 10, 12)		35		40		40	ns
8	t <sub>OLZ</sub>	Output in Low-Z from $\overline{OE}$ (Notes 4, 10, 12)	5		5		5		ns
9	t <sub>OHZ</sub>	Output in Hi-Z from $\overline{OE}$ (Notes 4, 10, 12)		30		35		35	ns
10	t <sub>PU</sub>	Chip Selection to Power-Up Time (Note 12)	0		0		0		ns
11	t <sub>PD</sub>	Chip Deselection to Power-Down Time (Note 12)		40		45		50	ns
<b>WRITE CYCLE</b>									
12	t <sub>WC</sub>	Write Cycle Time	70		90		100		ns
13	t <sub>CW</sub>	Chip Selection to End of Write (Note 1)	0 to +70°C		N/A		90		ns
			-55 to -125°C		N/A		N/A		
14	t <sub>AS</sub>	Address Setup Time	5		10		10		ns
15	t <sub>WP</sub>	Write Pulse Width (Note 1)	40		55		60		ns
16	t <sub>WR</sub>	Write Recovery Time	5		5		5		ns
17	t <sub>DS</sub>	Data Setup Time	30		35		40		ns
18	t <sub>DH</sub>	Data Hold Time	5		5		5		ns
19	t <sub>WLZ</sub>	Output in Low-Z from $\overline{WE}$ (Notes 4, 10, 12)	5		5		5		ns
20	t <sub>WHZ</sub>	Output in Hi-Z from $\overline{WE}$ (Notes 4, 10, 12)		30		35		35	ns
21	t <sub>AW</sub>	Address to End of Write	65		80		80		ns

Notes: See notes following DC Characteristics table.

## SWITCHING CHARACTERISTICS (Cont'd.)

Am9128-12, -15, -20

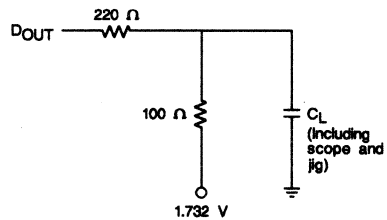
No.	Parameter Symbol	Parameter Description	Am9128-12		Am9128-15		Am9128-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>									
1	t <sub>RC</sub>	Read Cycle Time	120		150		200		ns
2	t <sub>ACC</sub>	Address Access Time (Note 9)		120		150		200	ns
3	t <sub>ACS</sub>	Chip Select Access Time (Note 9)		120		150		200	ns
4	t <sub>OE</sub>	Output Enable Time (Note 9)	COM'L	N/A		60		70	ns
			MIL	70		70		80	
5	t <sub>OH</sub>	Output Hold Time from Address Change	5		5		5		ns
6	t <sub>CLZ</sub>	Output in Low-Z from $\overline{CE}$ (Notes 4, 10, 12)	5		5		5		ns
7	t <sub>CHZ</sub>	Output in Hi-Z from $\overline{CE}$ (Notes 4, 10, 12)		50		55		55	ns
8	t <sub>OLZ</sub>	Output in Low-Z from $\overline{OE}$ (Notes 4, 10, 12)	5		5		5		ns
9	t <sub>OHZ</sub>	Output in Hi-Z from $\overline{OE}$ (Notes 4, 10, 12)		45		50		50	ns
10	t <sub>PU</sub>	Chip Selection to Power-Up Time (Note 12)	0		0		0		ns
11	t <sub>PD</sub>	Chip Deselection to Power-Down Time (Note 12)		55		60		60	ns
<b>WRITE CYCLE</b>									
12	t <sub>WC</sub>	Write Cycle Time	120		150		200		ns
13	t <sub>CW</sub>	Chip Selection to End of Write (Note 1)	COM'L	N/A		120		150	ns
			MIL	105		130		160	
14	t <sub>AS</sub>	Address Setup Time	10		20		20		ns
15	t <sub>WP</sub>	Write Pulse Width (Note 1)	70		85		100		ns
16	t <sub>WR</sub>	Write Recovery Time	5		5		5		ns
17	t <sub>DS</sub>	Data Setup Time	45		50		60		ns
18	t <sub>DH</sub>	Data Hold Time	5		5		5		ns
19	t <sub>WLZ</sub>	Output in Low-Z from $\overline{WE}$ (Notes 4, 10, 12)	5		5		5		ns
20	t <sub>WHZ</sub>	Output in Hi-Z from $\overline{WE}$ (Notes 4, 10, 12)		50		50		50	ns
21	t <sub>AW</sub>	Address to End of Write	105		120		120		ns

Notes: See notes following DC Characteristics table.

### SWITCHING TEST CONDITIONS

Input Pulse Levels	.4 to 2.4 V
Input Rise and Fall Times	10 ns
Input Timing Reference Levels	1.4 V
Output Timing Reference Levels	1.4 V

### SWITCHING TEST CIRCUIT









TC003700

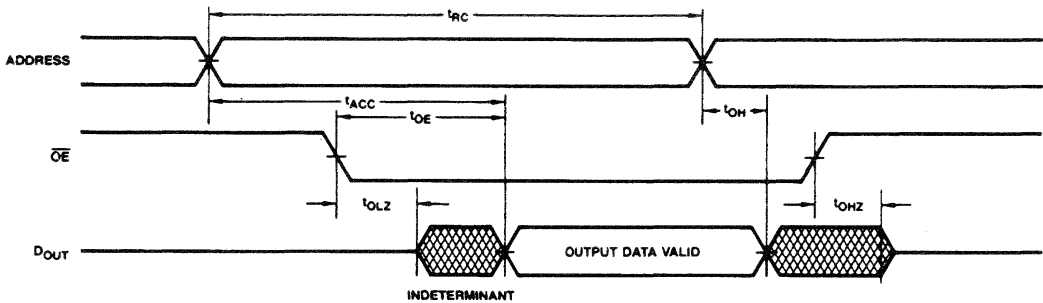


# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
 	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE. ANY CHANGE PERMITTED	CHANGING. STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE 'OFF' STATE

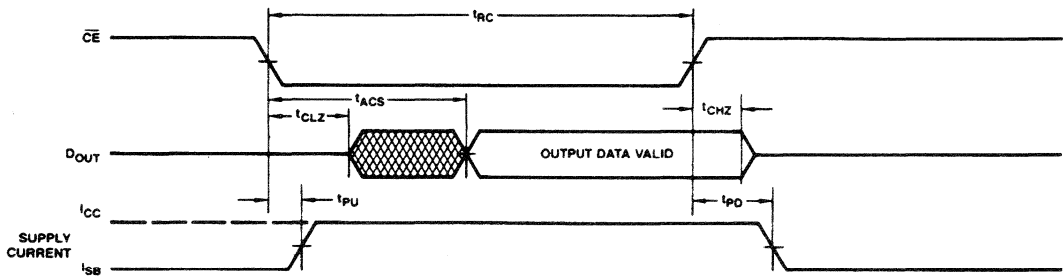
KS000010



WF000130

**Read Cycle No. 1 (Notes 5, 6)**

4

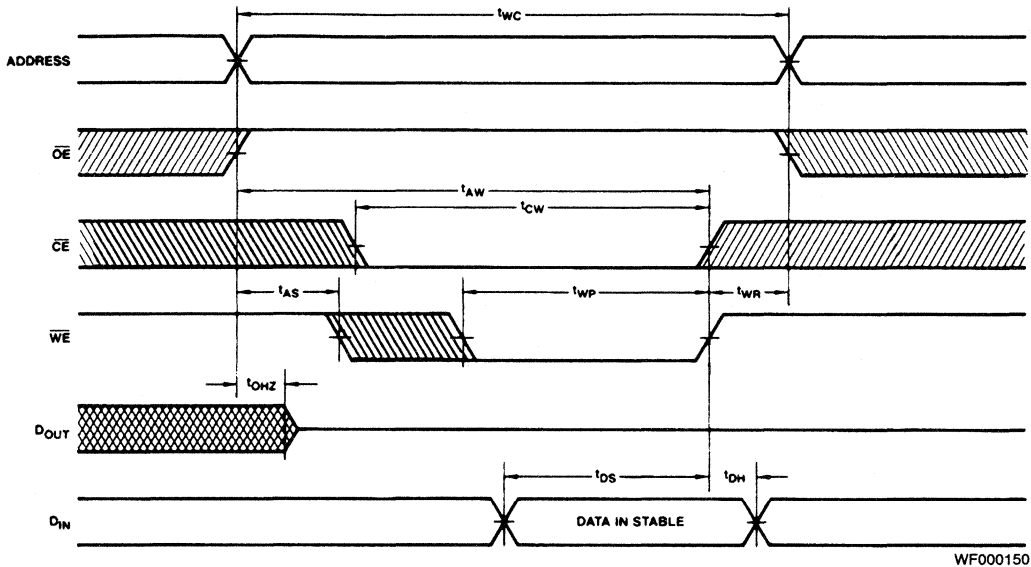


WF000140

**Read Cycle No. 2 (Notes 5, 7, 8)**

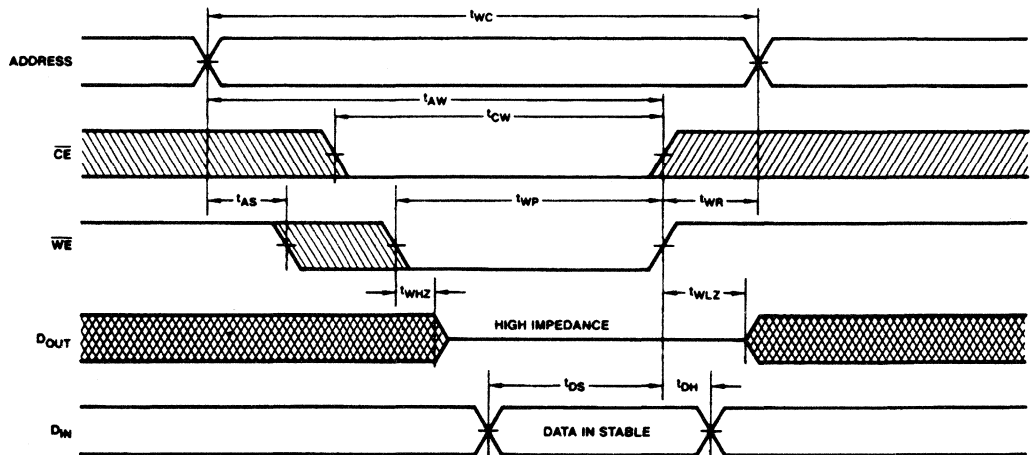
Notes: See notes following DC Characteristics table.

**SWITCHING WAVEFORMS (Cont'd.)**



WF000150

**Write Cycle No. 1**



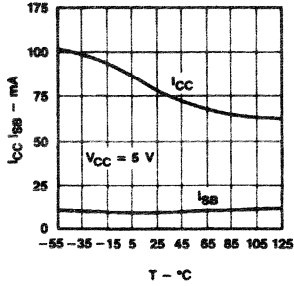
WF000160

**Write Cycle No. 2 (Notes 7, 8)**

Notes: See notes following DC Characteristics table.

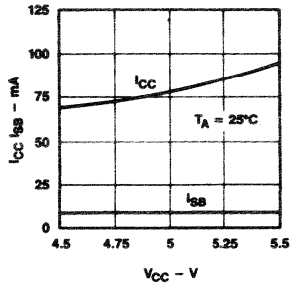
## TYPICAL PERFORMANCE CURVES

**Supply Current  
Versus Ambient Temperature**



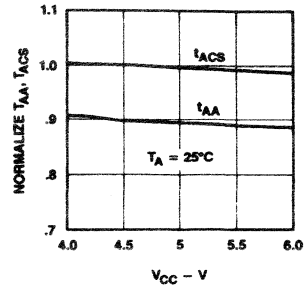
OP000640

**Supply Current  
Versus Supply Voltage**



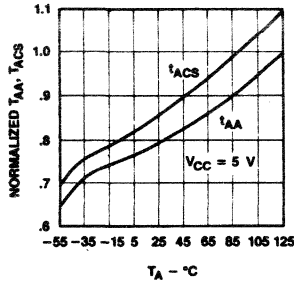
OP000650

**Normalized Access Time  
Versus Supply Voltage**



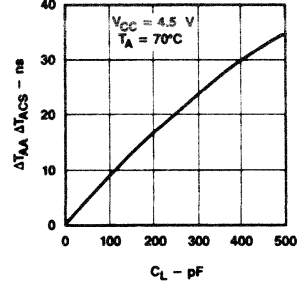
OP000660

**Normalized Access Time  
Versus Ambient Temperature**



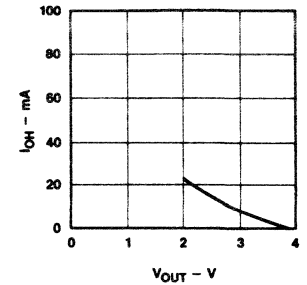
OP000670

**Access Time Change  
Versus Output Loading**



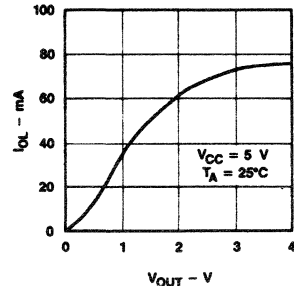
OP000680

**Output Source Current  
Versus Output Voltage**



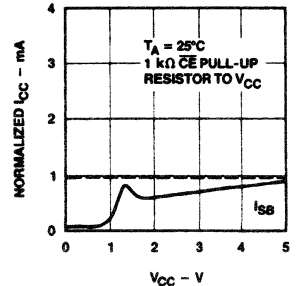
OP000690

**Output Sink Current  
Versus Output Voltage**



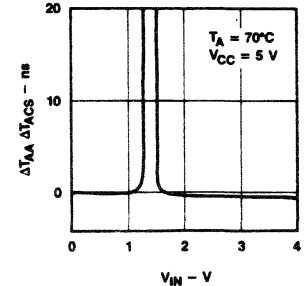
OP000700

**Typical Power-On Current  
Versus Power Supply**



OP000710

**Access Time Change  
Versus Input Voltage**



OP000720



# Am2130/Am2140

1024x8 Dual-Port Static Random-Access Memories

## DISTINCTIVE CHARACTERISTICS

- True dual port operation
- Access time as fast as 55 ns
- Master device (Am2130) has on-chip arbitration
- Expandable data bus width in multiples of 8 bits using one master (Am2130) and required number of slave devices (Am2140)
- Automatic power-down feature
- All inputs and outputs are TTL-compatible
- 48-pin DIP or 52-pin PLCC
- Single +5-volt power supply
- Advanced N-MOS technology

## GENERAL DESCRIPTION

The Am2130 and the Am2140 are members of the 1K x 8 dual-port static RAM family. The Am2130 is designated as the master and the Am2140 as the slave device. The master provides the necessary control signal to the slave devices to facilitate implementing a wider data bus in a system. The master/slave concept allows expansion with minimal external logic.

Both devices have two independent ports called Left and Right port. Each port consists of an 8-bit bidirectional data bus and a 10-bit address input bus and necessary control signals.

The Am2130 has an on-board arbiter to resolve contention between the left and right ports. When contention between ports occurs, one port is given priority while the other port receives a busy indication.

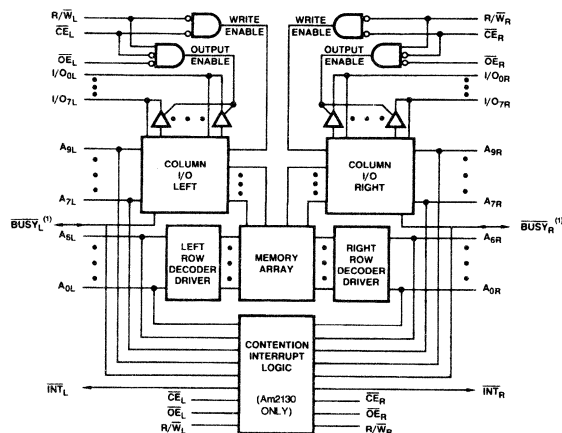
The Am2130 also contains on-chip facilities for supporting semaphores. Addresses (3FE)<sub>H</sub> and (3FF)<sub>H</sub> serve as

interrupt generators. If any data is written at the address (3FF)<sub>H</sub> from the left port, an interrupt signal becomes active for the right port. The interrupt signal is deactivated by reading from the right port at the same address. The address (3FE)<sub>H</sub> is used in a similar fashion by the right port to activate the interrupt signal for the left port.

The Am2130/Am2140 also have two chip enable signals corresponding to the left and right ports. Before any transaction on a port takes place, the corresponding chip enable input must be activated. If a chip enable signal is not active, the circuitry corresponding to its side automatically powers down and enters standby mode.

The Am2130/Am2140 are packaged in 48-pin DIPs or 52-pin plastic leaded chip carrier. All inputs and outputs are TTL-compatible and the devices operate from a single +5-volt power supply.

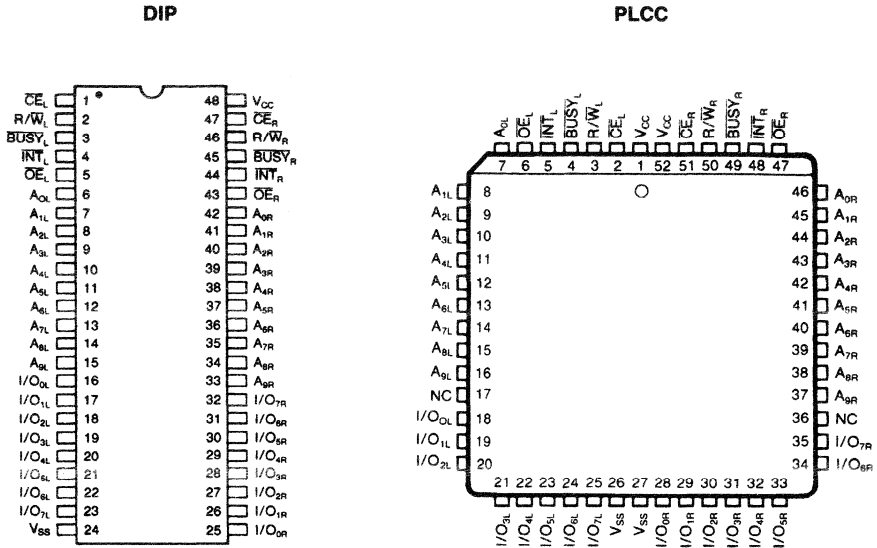
## BLOCK DIAGRAM



BD005085

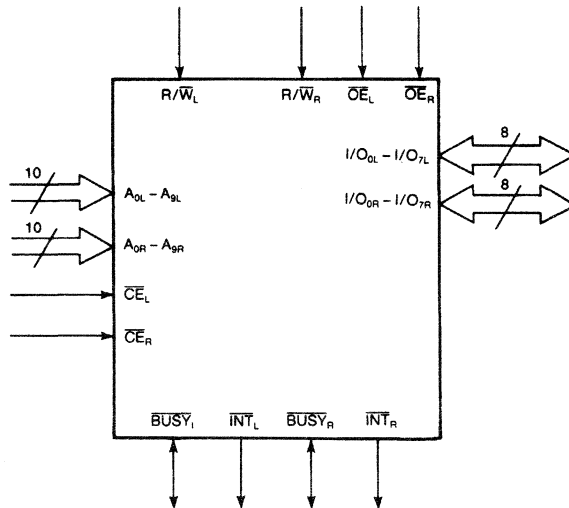
Notes: 1. Am2130 (Master): BUSY is open-drain output and requires pull-up resistor.  
Am2140 (Slave): BUSY is an input.

## CONNECTION DIAGRAMS Top View



Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



LS002232

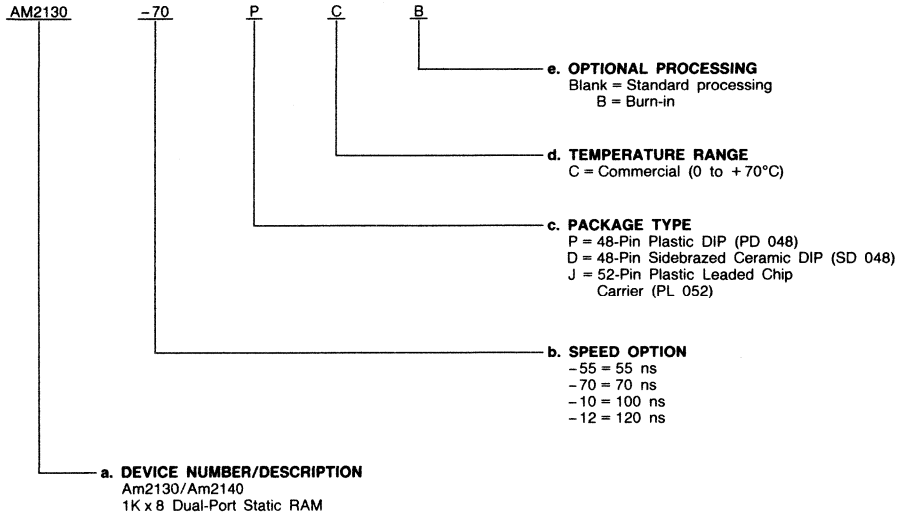
V<sub>CC</sub> = +5-V Power Supply  
V<sub>SS</sub> = Ground

## ORDERING INFORMATION

### Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM2130-55	PC, PCB, DC, DCB, JC, JCB
AM2130-70	
AM2130-10	
AM2130-12	
AM2140-55	
AM2140-70	
AM2140-10	
AM2140-12	

#### Valid Combinations

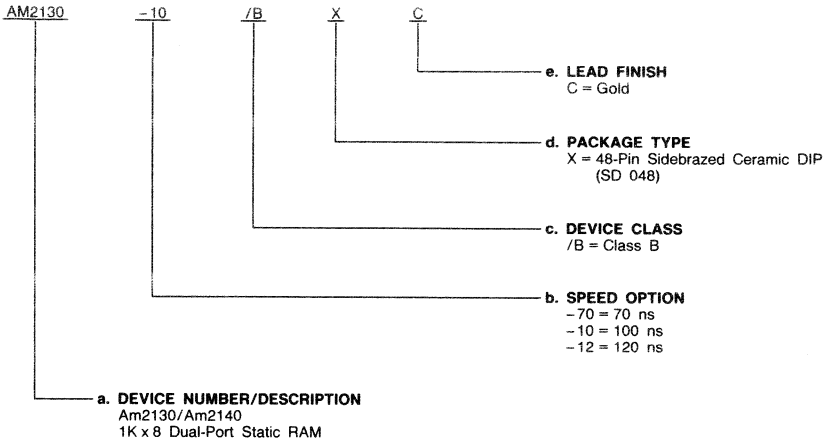
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM2130-70	/BXC
AM2130-10	
AM2130-12	
AM2140-70	
AM2140-10	
AM2140-12	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

### Am2130

#### **A<sub>0L</sub> – A<sub>9L</sub> Left Port Address (Inputs)**

These 10 inputs constitute the memory address for the left port. A<sub>0</sub> is the least significant bit position and A<sub>9</sub> is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and LOW represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

If a write operation is performed using (3FF)<sub>H</sub>, an interrupt signal is activated for the right port (see  $\overline{\text{INT}}_R$  pin description).

If a read operation is performed using (3FE)<sub>H</sub>, the  $\overline{\text{INT}}_L$  signal will be deactivated (see  $\overline{\text{INT}}_L$  description).

#### **A<sub>0R</sub> – A<sub>9R</sub> Right Port Address (Inputs)**

These 10 inputs constitute the memory address for the right port. A<sub>0</sub> is the least significant bit position and A<sub>9</sub> is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and LOW represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

If a write operation is performed using (3FE)<sub>H</sub>, an interrupt signal is activated for the left port (see  $\overline{\text{INT}}_L$  pin description).

If a read operation is performed using (3FF)<sub>H</sub>, the  $\overline{\text{INT}}_R$  signal will be deactivated (see  $\overline{\text{INT}}_R$  description).

#### **$\overline{\text{BUSY}}_L$ Left Port Busy Flag (Output; Open Drain)**

This open-drain output requires a pull-up resistor for proper operation. A LOW on this output indicates that the on-chip arbitration logic detected a contention between the left and right ports and the right port is given priority. All left port signals must be held stable until a HIGH on this output is indicated.

The  $\overline{\text{BUSY}}_L$  signal generation is a logical function of the left and right port address inputs and the  $\overline{\text{CE}}_L$  and  $\overline{\text{CE}}_R$  inputs. The transient behavior of the  $\overline{\text{BUSY}}_L$  output is not assured while the inputs are changing.

#### **$\overline{\text{BUSY}}_R$ Right Port Busy Flag (Output; Open Drain)**

This open-drain output requires a pull-up resistor for proper operation. A LOW on this output indicates that the on-chip arbitration logic detected a contention between the left and right ports and the left port is given priority. All right port signals must be held stable until a HIGH on this output is indicated.

The  $\overline{\text{BUSY}}_R$  signal generation is a logical function of the left and right port address inputs and the  $\overline{\text{CE}}_L$  and  $\overline{\text{CE}}_R$  inputs. The transient behavior of the  $\overline{\text{BUSY}}_R$  output is not assured while the inputs are changing.

#### **$\overline{\text{CE}}_L$ Left Port Chip Enable (Input)**

This input must be LOW before any transaction from the left port and remain LOW for the duration of the transaction. When this input goes HIGH, left port logic circuits enter standby power mode and remain in this mode as long as this input remains HIGH. It should be noted that powering down the left port to standby mode does not affect the  $\overline{\text{INT}}_L$  or  $\overline{\text{INT}}_R$  outputs. This input going HIGH also initializes the internal arbitration latch. It is recommended that  $\overline{\text{CE}}_L$  go HIGH after completing a transaction (see discussion on arbitration).

#### **$\overline{\text{CE}}_R$ Right Port Chip Enable (Input)**

Operation of this input is identical to  $\overline{\text{CE}}_L$  except that the  $\overline{\text{CE}}_R$  input controls the right port.

#### **GND (V<sub>SS</sub>) Ground**

#### **I/O<sub>0L</sub> – I/O<sub>7L</sub> Left Port Input/Output Bus (Input/Output; Three State)**

These eight lines constitute the data bus for the left port. If a read operation is performed using the left port, data from the location addressed by the left port address will be available on these lines. Similarly, to perform a write operation using the left port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the  $\overline{\text{CE}}_L$  is LOW,  $\overline{\text{OE}}_L$  is LOW and R/ $\overline{\text{W}}_L$  is HIGH.

#### **I/O<sub>0R</sub> – I/O<sub>7R</sub> Right Port Input/Output Bus (Input/Output; Three State)**

These eight lines constitute the data bus for the right port. If a read operation is performed using the right port, data from the location addressed by the right port address will be available on these lines. Similarly, to perform a write operation using the right port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the  $\overline{\text{CE}}_R$  is LOW,  $\overline{\text{OE}}_R$  is LOW and R/ $\overline{\text{W}}_R$  is HIGH.

#### **$\overline{\text{INT}}_L$ Left Port Interrupt Flag (Output; Open Drain)**

This open-drain output requires a pull-up resistor for proper operation. If the right port performs any write operation using address (3FE)<sub>H</sub>, then this output goes LOW. It will remain LOW until the left port successfully completes any read operation using the address (3FE)<sub>H</sub>. It should be noted that powering down the ports has no effect on this output.

#### **$\overline{\text{INT}}_R$ Right Port Interrupt Flag (Output; Open Drain)**

This open-drain output requires a pull-up resistor for proper operation. If the left port performs any write operation using address (3FF)<sub>H</sub>, then this output goes LOW. It will remain LOW until the right port successfully completes any read operation using the address (3FF)<sub>H</sub>. It should be noted that powering down the ports has no effect on this output.

#### **$\overline{\text{OE}}_L$ Output Enable Left I/O Port (Input)**

When this input is HIGH, the left port I/O bus lines are in high impedance state. If this input is LOW and  $\overline{\text{CE}}_L$  is LOW and R/ $\overline{\text{W}}_L$  is HIGH, the left port drivers are enabled and data from the location addressed by the A<sub>0L</sub> – A<sub>9L</sub> inputs will be available on the I/O bus lines of the left port. It may be of interest to note that the  $\overline{\text{OE}}_L$  input has no effect on the  $\overline{\text{BUSY}}_L$  or  $\overline{\text{BUSY}}_R$  or  $\overline{\text{INT}}_L$  or  $\overline{\text{INT}}_R$  signals. Even though the left port I/O port drivers are disabled when the R/ $\overline{\text{W}}_L$  input goes LOW (write operation), it is recommended that the  $\overline{\text{OE}}_L$  signal be kept HIGH during write operations to the left port.

#### **$\overline{\text{OE}}_R$ Output Enable Right I/O Port (Input)**

When this input is HIGH, the right port I/O bus lines are in high impedance state. If this input is LOW and  $\overline{\text{CE}}_R$  is LOW and R/ $\overline{\text{W}}_R$  is HIGH, the right port drivers are enabled and data from the location addressed by the A<sub>0R</sub> – A<sub>9R</sub> inputs will be available on the I/O bus lines of the right port. It may be of interest to note that the  $\overline{\text{OE}}_R$  input has no effect on the  $\overline{\text{BUSY}}_L$  or  $\overline{\text{BUSY}}_R$  or  $\overline{\text{INT}}_L$  or  $\overline{\text{INT}}_R$  signals. Even though the left port I/O port drivers are disabled when the R/ $\overline{\text{W}}_R$  input goes LOW (write operation), it is recommended that the  $\overline{\text{OE}}_R$  signal be kept HIGH during write operations to the right port.



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**R/ $\overline{W}$ <sub>L</sub> Left Port Read/Write Enable (Input)**

This input is used to specify the left port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the  $\overline{CE}_L$  is LOW and the  $\overline{OE}_L$  is LOW and the R/ $\overline{W}_L$  is HIGH, data from the location addressed by the A<sub>0L</sub> – A<sub>9L</sub> will be available on the I/O<sub>0L</sub> – I/O<sub>7L</sub> lines. As mentioned earlier, reading from the left port at the location (3FE)<sub>H</sub> disables the  $\overline{INT}_L$  output.

When the  $\overline{CE}_L$  is LOW and the R/ $\overline{W}_L$  goes LOW, data present on the I/O<sub>0L</sub> – I/O<sub>7L</sub> lines will be written into the location addressed by the A<sub>0L</sub> – A<sub>9L</sub> inputs. It should be noted that the write operation is not affected by the  $\overline{OE}_L$  input. However, it is recommended that the  $\overline{OE}_L$  input be held HIGH during a write operation. As mentioned earlier, performing a write operation from the left port at the address (3FF)<sub>H</sub> causes the  $\overline{INT}_R$  output to go LOW.

It should be noted that even though R/ $\overline{W}_L$  is LOW, writing is internally inhibited if the right port is given priority by the arbiter. Discussion on arbitration can be found in a later section.

**R/ $\overline{W}$ <sub>R</sub> Right Port Read/Write Enable (Input)**

This input is used to specify the right port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the  $\overline{CE}_R$  is LOW and the  $\overline{OE}_R$  is LOW and the R/ $\overline{W}_R$  is HIGH, data from the location addressed by the A<sub>0R</sub> – A<sub>9R</sub> will be available on the I/O<sub>0R</sub> – I/O<sub>7R</sub> lines. As mentioned earlier, reading from the right port at the location (3FF)<sub>H</sub> disables the  $\overline{INT}_R$  output.

When the  $\overline{CE}_R$  is LOW and the R/ $\overline{W}_R$  goes LOW, data present on the I/O<sub>0R</sub> – I/O<sub>7R</sub> lines will be written into the location addressed by the A<sub>0R</sub> – A<sub>9R</sub> inputs. It should be noted that the write operation is not affected by the  $\overline{OE}_R$  input. However, it is recommended that the  $\overline{OE}_R$  input be held HIGH during a write operation. As mentioned earlier, performing a write operation from the left port at the address (3FE)<sub>H</sub> causes the  $\overline{INT}_L$  output to go LOW.

It should be noted that even though R/ $\overline{W}_R$  is LOW, writing is internally inhibited if the left port is given priority by the arbiter. Discussion on arbitration can be found in a later section.

**V<sub>CC</sub> +5-Volt Power Supply**

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**Am2140**

The Am2140 is functionally very similar to the Am2130. The Am2140 differs from the Am2130 in two signals only —  $\overline{BUSY}_L$  and  $\overline{BUSY}_R$ . In the case of the Am2140 they are used as inputs and play a significant role in expanding the word width.

 **$\overline{BUSY}_L$  Left Port Busy Flag (Input)**

If this input is LOW, a write enable signal to the left side of the memory array is internally disabled. In expanded systems where an Am2130 is used as the master, this input is connected to the  $\overline{BUSY}_L$  output of the Am2130.

 **$\overline{BUSY}_R$  Right Port Busy Flag (Output; Open Drain)**

If this input is LOW, a write enable signal to the right side of the memory array is internally disabled. In expanded systems where an Am2130 is used as the master, this input is connected to the  $\overline{BUSY}_R$  output of the Am2130.

## FUNCTIONAL DESCRIPTION

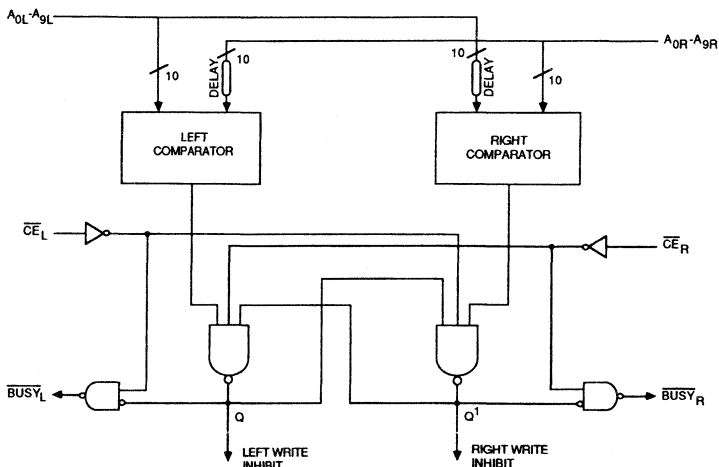
As shown in the block diagram, the Am2130/Am2140 is a true 1K x 8 dual-port RAM. It consists of a memory array with two sets of address decoders and associated logic. This arrangement allows the accessing of every word in the memory array from two independent sources. We call these sources left side and right side for convenience. Data accessed by the left-side address inputs appears on the left-side data lines of the array and is connected to the left-side I/O pins through the associated three-state buffers. The enable control signal for these buffers is generated using the  $R/\overline{W}_L$ ,  $\overline{CE}_L$  and  $\overline{OE}_L$  inputs. If the I/O buffers are disabled on the chip, the I/O pins can be used as inputs. Data to be written from the left port is presented on these inputs. Writing into the memory array from the left side is controlled by the left write enable signal generated on the chip using the  $R/\overline{W}_L$  and  $\overline{CE}_L$  inputs. An identical arrangement exists for the right side also. In addition, there is on-chip arbitration logic to give priority to one port over the other in case of a contention, and interrupt flag logic.

### Contention Arbitration

Two independent access facilities are provided in a dual-port memory to eliminate physical interference between signals. However, there are two significant possibilities of "logical" interference which are not tolerable: when one port is reading from a location while the other port is writing into the same location at the same time. In this case, data received by the reading port may not be predictable. Similarly, consider the situation when both ports write information into the same location simultaneously. The resultant data that finally ends up in the memory location may not be valid. These two situations are commonly called contention. The Am2130 has on-chip logic to detect contention and give priority to one port over the other. In a true dual-port RAM, simultaneous reading from both ports at the same address does not corrupt the data. Hence, it can be construed that no contention occurs. However, for the sake of simplicity and compatibility with the industry standard practices, the Am2130 arbitration is based purely on addresses. Hence, in the case of a simultaneous read from both ports at the same address, the arbitration logic will sense contention and give priority to one of the ports. The other port will receive a busy indication.

Figure 1 is a conceptual logic diagram of contention arbitration logic. It consists of two equality comparators. The left comparator compares the left port address inputs to the delayed version of the right port address. Similarly, the right comparator compares the right-port address to the delayed version of the left port address. The output of the comparators is connected to a latch formed by two cross-coupled NAND gates as shown in Figure 1. The chip enable signals,  $\overline{CE}_L$  and  $\overline{CE}_R$ , are also inputs to this latch as shown. The  $\overline{BUSY}_L$  and  $\overline{BUSY}_R$  outputs are generated by gating the latch output with the proper chip enable signal as shown. Also note that the latch outputs are used internally for left and right write inhibit signals. For example, if the right side write inhibit signal in Figure 1 is LOW, writing into the memory does not occur even if the  $R/\overline{W}_R$  input of the Am2130 is LOW.

The operation of the arbitration circuit can now be explained. Assume that the left port address had been stable and  $\overline{CE}_L$  is LOW. Both Q and Q' outputs of the latch will be HIGH because the output of both comparators is LOW (addresses are different). So the  $\overline{BUSY}$  output on both sides is HIGH. Now assume that the right address changes and becomes equal to the left address. The right address comparator output goes HIGH and the Q' output of the latch goes LOW. Eventually the output of the left comparator also goes HIGH, but because of the cross coupling of the Q' into the gate generating the Q output, Q output remains HIGH. As soon as the  $\overline{CE}_R$  input goes LOW,  $\overline{BUSY}_R$  becomes LOW. Thus, the arbitrator gave priority to the left port by indicating a busy signal to the right port. Thus in this example, the left port is the winner and the right port is the loser in the contention for the memory. Sooner or later the left port will finish its transaction at the contended location and change the address or its chip enable will go HIGH. Thus when the contention is over the Q output of the latch will become HIGH and  $\overline{BUSY}_R$  will go HIGH. A similar reasoning can be used to understand the operation of the left side. It should be clear then, in cases of contention, the arbiter will decide one port as the winner and the losing port must wait for the winner to complete the use of the memory. The winning port must indicate to the arbiter that it has completed its operation either by changing the address or making its chip enable input HIGH. Without such an indication, the arbiter will not remove the busy indication to the losing port.



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Figure 1. Conceptual Arbitration Logic

## Read/Write Operations

Performing read/write operations when there is no contention is relatively straightforward. The sequence of events for a read is listed below. The timing relationships between various signals can be found in later sections of this data sheet.

1. Establish HIGH on the  $R/\overline{W}$  and LOW on the  $\overline{CE}$  input of the desired port.
2. Establish the desired address on the desired port address lines.
3. Make the  $\overline{OE}$  input of the desired port LOW.
4. The I/O lines of the selected port will contain the data after the access time has elapsed.
5. Make the output enable and chip enable inputs HIGH to complete the read operation.

Performing write operations when there is no contention is equally straightforward. The sequence of events for a write is listed below. The timing relationships between various signals can be found in later sections of this data sheet.

1. Establish LOW on the  $\overline{CE}$  input of the desired port.
2. Establish the desired address on the desired port address lines.
3. Establish the desired data on the I/O lines of the port.
4. Make the  $R/\overline{W}$  input of the port LOW and bring it HIGH after the specified amount of time.
5. Make the  $\overline{CE}$  input HIGH to complete the operation.

When a read or write operation is initiated by a port and contention from the other port occurs, the implications are very simple. The losing port will see its  $\overline{BUSY}$  line go LOW. The port must wait until a HIGH is indicated on the  $\overline{BUSY}$  line. Thus in this case of contention, the operation did not really start when the port initiated it. Instead, the operation actually started when the  $\overline{BUSY}$  line went HIGH. See the timing diagram for details.

## Interrupts

Each port has an associated output called interrupt. The interrupt outputs are activated and deactivated by the on-chip logic when read and write operations occur with a particular address location. For example, if a write operation is performed by the left port with address  $(3FF)_H$ , an on-chip latch is set. This latch drives the  $\overline{INT}_R$  output LOW. The latch is cleared only when a read operation from the right port using the address  $(3FF)_H$  takes place. Similarly, if a write operation from the right port using the address  $(3FE)_H$  occurs, a latch is set to drive the  $\overline{INT}_L$  output LOW. The  $\overline{INT}_L$  will go HIGH (latch is cleared) only after a read operation from the left port using the address  $(3FE)_H$  occurs. As mentioned before, powering down a port to standby mode does not affect these outputs.

## Depth Expansion Using Multiple Am2130s

The Am2130 has an intrinsic storage capacity of 1K bytes. However, it is simple to expand the storage capacity by using multiple devices. Figure 2 is a conceptual diagram of a 2K byte dual port memory system using two Am2130 devices. The principle behind such expansion is obvious: all that needs to be done is to decode the most significant system address to generate the individual  $\overline{CE}$  inputs for the Am2130s. For

example in Figure 2,  $A_{10}$  is the most significant address bit. When this signal is LOW and  $\overline{CE}$  input is LOW, the chip enable input of the upper Am2130 goes LOW. Thus, the first 1K locations are selected for transactions. On the other hand, if  $A_{10}$  is HIGH and  $\overline{CE}$  is LOW, the chip enable input of the lower Am2130 goes LOW selecting the second 1K locations. As depicted in the figure, the address inputs of both Am2130 devices are bussed together. Similarly, the I/O signals are also bussed to create the overall data bus. Also note that the other control signals are connected between the two devices.

In this example, we have not used the interrupt outputs. However, it should be noted that depth expansion using multiple devices does not change the operation of the interrupt outputs. The interrupt output of each device behaves as described before. Hence, the user must decide which interrupt output from which device will be used in his system.

## Width Expansion

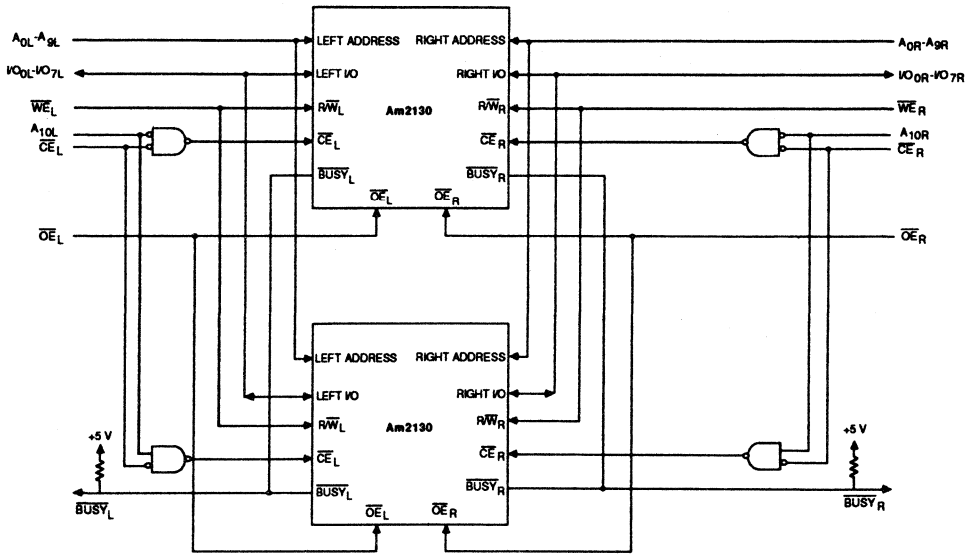
The intrinsic width of the data word of the Am2130 is eight bits. However, it is possible to realize wider data words (multiples of 8) by using multiple devices. The instinctive solution of taking the required number of the devices and assigning the data bits to individual devices is potentially unreliable. As we know, the Am2130 has arbitration logic on the chip, and hence is called the master. When several of these masters are present, device-to-device variations and other factors may cause one device to give priority to one port, while another device gives priority to the other port. In essence both ports are busy! This is an undesirable situation and should not be allowed in operation. The most elegant way to avoid the situation is to allow only one device to arbitrate the contention. It is recommended that when expanding the width of the data words, the Am2130 be used as the master and a number of Am2140s be used as slave devices. The Am2140 does not have the arbitration capability; instead it accepts the  $\overline{BUSY}$  outputs generated by the Am2130 as inputs.

Figure 3 is a conceptual diagram of a 16-bit system using one Am2130 and one Am2140. As can be seen, using master/slave devices avoids external logic for expansion. For the sake of completeness of this discussion, it may be noted that it is indeed possible to expand the width using Am2130s only. However, external logic must be provided to prevent every device of the system from arbitrating. We want only one device to be the arbitrator. As explained in Figure 1, arbitration can be defeated by suitable control of the  $\overline{CE}$  input of the Am2130.

Figure 4 shows a conceptual diagram of a 16-bit system using two Am2130s. Device 1 in this figure behaves as the master. The external logic shown in the figure ensures that the  $\overline{CE}$  input of Device 2 is HIGH if the corresponding  $\overline{BUSY}$  output of Device 1 is LOW. Thus the arbitration logic of Device 2 is prevented from taking part in resolving contention.

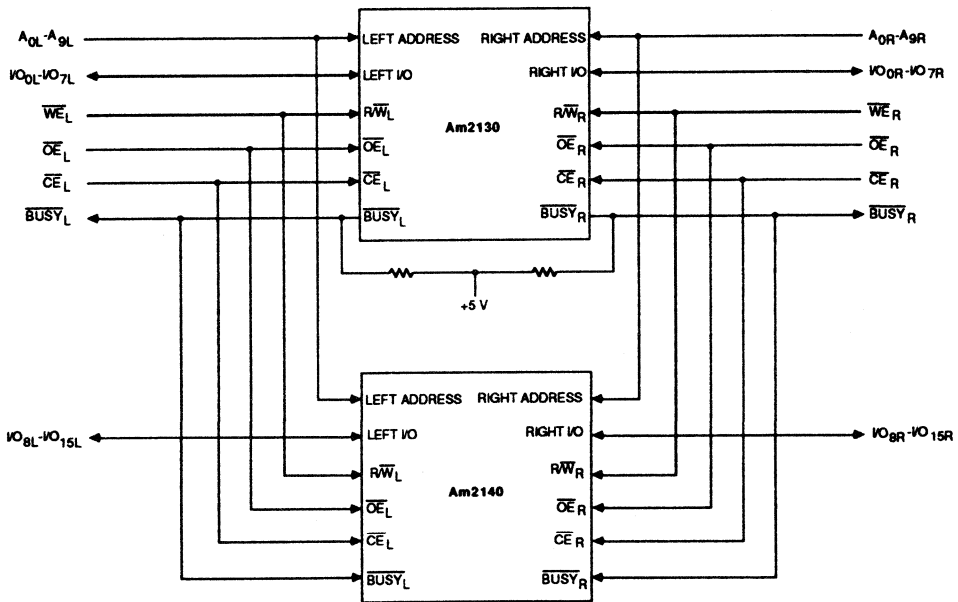
## Simultaneous Width and Depth Expansion

By combining the depth and width expansion schemes discussed, it is possible to build systems with greater depth (multiples of 1K) and wider words (multiples of 8). Figure 5 shows a conceptual diagram of a 2K x 16 system. The operation of this scheme is understood by suitably combining the explanation of Figure 2 and Figure 3 and hence is not repeated here.



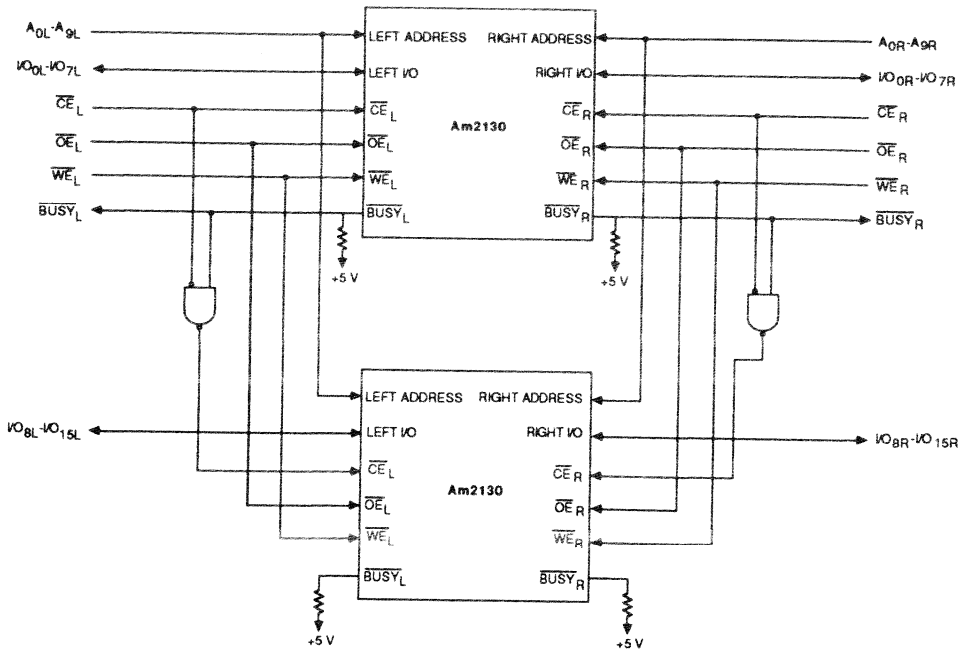
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Figure 2. Conceptual Depth Expansion



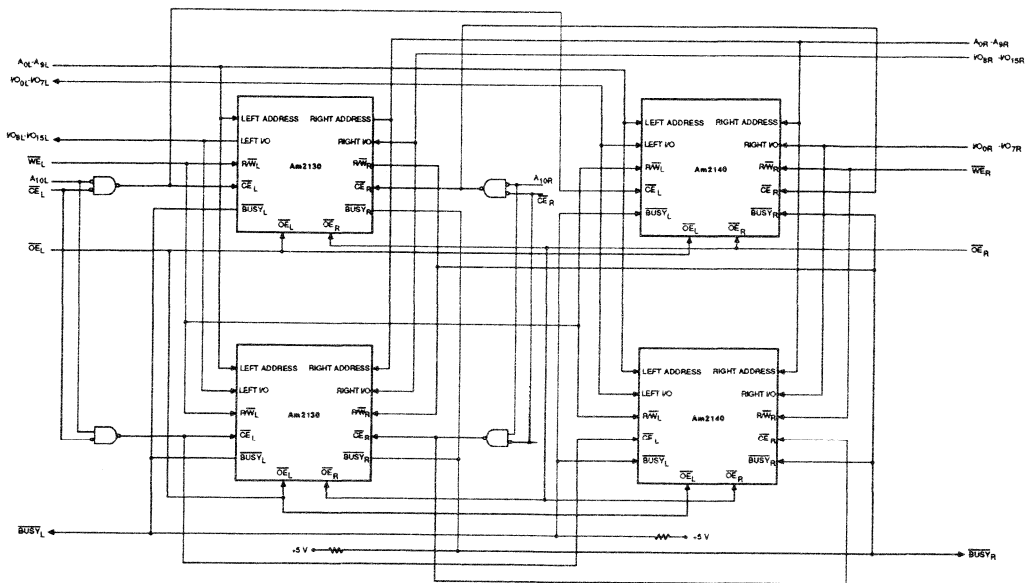
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Figure 3. Width Expansion with Master/Slave



BD007410

Figure 4. Width Expansion with Master



BD007390

Figure 5. Conceptual Diagram of a 2K x 16 System Using Master/Slave

**TABLE 1. NON-CONTENTION READ/WRITE CONTROL**

R/W <sub>L</sub>	Left Port Inputs			Right Port Inputs				Left Flags		Right Flags		Function
	$\overline{CE}_L$	$\overline{OE}_L$	A <sub>0L</sub> - A <sub>9L</sub>	R/W <sub>R</sub>	$\overline{CE}_R$	$\overline{OE}_R$	A <sub>0R</sub> - A <sub>9R</sub>	$\overline{BUSY}_L$	INT <sub>L</sub>	$\overline{BUSY}_R$	INT <sub>R</sub>	
X	H	X	X	X	X	X	X	H	X	H	X	Left port in power-down mode
X	X	X	X	X	H	X	X	H	X	H	X	Right port in power-down mode
L	L	X	X	X	X	X	X	H	X	X	X	Data on left port written to memory location A <sub>0L</sub> - A <sub>9L</sub>
H	L	L	X	X	X	X	X	H	X	X	X	Data in memory location A <sub>0L</sub> - A <sub>9L</sub> output on left port
X	X	X	X	L	L	X	X	X	X	H	X	Data on right port written to memory location A <sub>0R</sub> - A <sub>9R</sub>
X	X	X	X	H	L	L	X	X	X	H	X	Data in memory location A <sub>0R</sub> - A <sub>9R</sub> output on right port
L	L	X	3FF	X	X	X	X	H	X	H	L	Left port flags right port to read memory location 3FF
X	X	X	X	L	L	X	3FE	H	L	H	X	Right port flags left port to read memory location 3FE

**TABLE 2. BUSY ARBITRATION OF ADDRESS CONTENTION**

Left Port				Right Port				Flags (Note 1)		Function
R/W <sub>L</sub>	$\overline{CE}_L$	$\overline{OE}_L$	A <sub>0L</sub> - A <sub>9L</sub>	R/W <sub>R</sub>	$\overline{CE}_R$	$\overline{OE}_R$	A <sub>0R</sub> - A <sub>9R</sub>	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	L (LIV)	X	Match	X	L	X	Match	L	H	Right-Port operation only is permitted. (Note 3)
X	L	X	Match (LIV)	X	L	X	Match	L	H	
X	L	X	Match	X	L (LIV)	X	Match	H	L	Left-port operation only is permitted. (Note 4)
X	L	X	Match	X	L	X	Match (LIV)	H	L	

**TABLE 3. INTERRUPT FLAG**

Left Port				Right Port						Function
R/W <sub>L</sub>	$\overline{CE}_L$	$\overline{OE}_L$	A <sub>0L</sub> -A <sub>9L</sub>	INT <sub>L</sub>	R/W <sub>R</sub>	$\overline{CE}_R$	$\overline{OE}_R$	A <sub>0R</sub> -A <sub>9R</sub>	INT <sub>R</sub>	
L	L	X	3FF	X	X	X	X	X <sub>1</sub>	L	Set INT <sub>R</sub>
X	X	X	X <sub>1</sub>	X	H	L	L	3FF	H	Reset INT <sub>R</sub>
X	X	X	X <sub>1</sub>	L	L	L	X	3FE	X	Set INT <sub>L</sub>
H	L	L	3FE	H	X	X	X	X <sub>1</sub>	X	Reset INT <sub>L</sub>

Key: H = HIGH  
 L = LOW  
 LIV = Last Input Valid; meets t<sub>APS</sub> spec (Note 2)  
 X = Don't Care  
 X<sub>1</sub> = No Match, or  
 Same port deselected, or  
 Opposite port has priority

Notes: 1. INT Flags = X  
 2. If LIV violates t<sub>APS</sub> spec then one of the two ports receives priority, and the remaining port's  $\overline{BUSY}$  Flag goes LOW. However, there is an extremely rare metastable event which can occur when the arbitration circuitry cannot determine which port was "first" at the matching address. On this rare occurrence, both ports may momentarily receive  $\overline{BUSY} = \text{LOW}$  signals until the metastable state is resolved (usually within a few nanoseconds). Thereafter, one port's  $\overline{BUSY}$  remains LOW while the other completes its operation and resumes normal operation.  
 3. A Left-Port Read operation is also permitted if the Right-Port is also reading.  
 4. A Right-Port Read operation is also permitted if the Left-Port is also reading.

## ABSOLUTE MAXIMUM RATINGS (Note 15)

Storage Temperature .....	-65 to +150°C
Ambient Temperature	
with Power Applied .....	-55 to +125°C
Supply Voltage	
with Respect to Ground .....	-0.5 to +7.0 V
All Signal Voltages .....	-3.5 to +7.0 V
Power Dissipation .....	1.2 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES (Note 8)

Commercial (C) Devices	
Temperature (T <sub>A</sub> ) .....	0 to +70°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 to +5.5 V
Military (M) Devices	
Temperature (T <sub>A</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Am2130/Am2140		Units	
			Min.	Max.		
I <sub>LI</sub>	Input Load Current (All Input Pins)	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ , V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA	
I <sub>CC</sub>	Power Supply Current (Both Ports Active)	V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$ Outputs Open	C Devices M Devices	170 185	mA	
I <sub>SB1</sub>	Standby Current (Both Ports Standby)	V <sub>CC</sub> = Min. to Max., $\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$	C Devices M Devices	30 40	mA	
I <sub>SB2</sub>	Standby Current (One Port Standby)	V <sub>CC</sub> = Max., $\overline{CE}_L = V_{IL}$ and $\overline{CE}_R = V_{IH}$ or $\overline{CE}_L = V_{IH}$ and $\overline{CE}_R = V_{IL}$	C Devices M Devices	110 125	mA	
V <sub>IL</sub>	Input LOW Voltage			-0.5	0.8	V
V <sub>IH</sub>	Input HIGH Voltage			2.2	6.0	V
V <sub>OL1</sub>	Output LOW Voltage (I/O <sub>0</sub> - I/O <sub>7</sub> )	I <sub>OL</sub> = 3.2 mA			0.4	V
V <sub>OL2</sub>	Open-Drain Output LOW Voltage (BUSY (Note 14), INT)	I <sub>OL</sub> = 4 mA (Note 7)			0.5	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA (Note 7)		2.4		V

## CAPACITANCE (Note 9)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C <sub>OUT</sub>	Output Capacitance			10	pF
C <sub>IN</sub>	Input Capacitance			10	

Notes: See notes following Switching Waveforms.



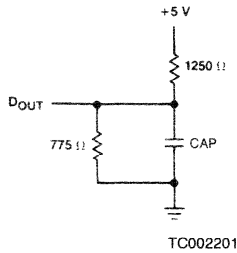
**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 7, 8, 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am2130/Am2140								Units
				-55		-70		-10		-12		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE (Note 10)</b>												
1	t <sub>RC</sub>	Read Cycle Time		55		70		100		120		ns
2	t <sub>AA</sub>	Address Access Time			55		70		100		120	ns
3	t <sub>ACE</sub>	Chip Enable Access Time			55		70		100		120	ns
4	t <sub>AOE</sub>	Output Enable Access Time			30		35		40		60	ns
5	t <sub>OH</sub>	Output Hold from Address Change		5		5		5		5		ns
6	t <sub>LZ</sub>	Output Low Z Time	(Notes 5 & 9)	5		5		5		5		ns
7	t <sub>HZ</sub>	Output High Z Time	(Notes 5 & 9)	0	25	0	30	0	40	0	40	ns
8	t <sub>PU</sub>	Chip Enable to Power Up Time	(Note 9)	0		0		0		0		ns
9	t <sub>PD</sub>	Chip Disable to Power Down Time	(Note 9)			35	35		50		60	ns
<b>WRITE CYCLE (Note 10)</b>												
10	t <sub>WC</sub>	Write Cycle Time		55		70		100		120		ns
11	t <sub>EW</sub>	Chip Enable to End of Write		55		65		90		100		ns
12	t <sub>AW</sub>	Address Valid to End of Write		50		65		90		100		ns
13	t <sub>AS</sub>	Address Setup Time		0		0		0		0		ns
14	t <sub>WP</sub>	Write Pulse Width		45		50		60		70		ns
15	t <sub>WR</sub>	Write Recovery Time		0		0		0		0		ns
16	t <sub>DW</sub>	Data Valid to End of Write		30		35		40		40		ns
17	t <sub>DH</sub>	Data Hold Time		0		0		0		0		ns
18	t <sub>WZ</sub>	Write Enabled to Output in High Z	(Notes 5 & 9)	0	25	0	30	0	40	0	50	ns
19	t <sub>OW</sub>	Output Active from End of Write	(Notes 5 & 9)	0		0		0		0		ns
<b>BUSY FLAG TIMING (Notes 7 &amp; 14)</b>												
20	t <sub>RC</sub>	Read Cycle Time		55		70		100		120		ns
21	t <sub>WC</sub>	Write Cycle Time		55		70		100		120		ns
22	t <sub>BW</sub>	BUSY to Write	(Note 13)	-5		-5		-5		-5		ns
23	t <sub>WH</sub>	Write Hold After BUSY	(Note 13)	20		20		20		20		ns
24	t <sub>BAA</sub>	BUSY Access Time to Address	(Note 9)		45		45		50		60	ns
25	t <sub>BDA</sub>	BUSY Disable Time to Address	(Note 9)		40		45		50		60	ns
26	t <sub>BAC</sub>	BUSY Access Time to Chip Enable or Chip Select	(Note 9)		40		45		50		60	ns
27	t <sub>BDC</sub>	BUSY Disable Time to Chip Enable or Chip Select	(Note 9)		40		45		50		60	ns
28	t <sub>APS</sub>	Arbitration Priority Setup Time		10		10		10		10		ns
<b>INTERRUPT TIMING (Note 7)</b>												
29	t <sub>WINS</sub>	$\overline{WE}$ to Interrupt Set Time			30		30		35		45	ns
30	t <sub>EINS</sub>	$\overline{CE}$ to Interrupt Set Time			50		55		60		70	ns
31	t <sub>INS</sub>	Address to Interrupt Set Time			50		55		60		70	ns
32	t <sub>OINR</sub>	Output Enable to Interrupt Reset Time			30		30		35		45	ns
33	t <sub>INR</sub>	Address to Interrupt Reset Time			50		55		60		70	ns
34	t <sub>EINR</sub>	Chip Enable to Interrupt Reset Time			50		55		60		70	ns

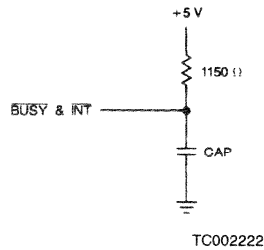
Notes: See notes following Switching Waveforms.



## SWITCHING TEST CIRCUITS



Test Loads A and B



Test Loads C and D

TEST OUTPUT LOADS	
Test Load	CAP
A	5 pF (Note 1)
B	100 pF
C	50 pF
D	5 pF (Note 1)

Notes: 1. Includes Scope and Jig Capacitance.

## SWITCHING TEST WAVEFORM

AC Test Conditions	
Input Levels	GND to 3.0 V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Test Output Load	See Test Output Loads Table

4

## SWITCHING WAVEFORMS

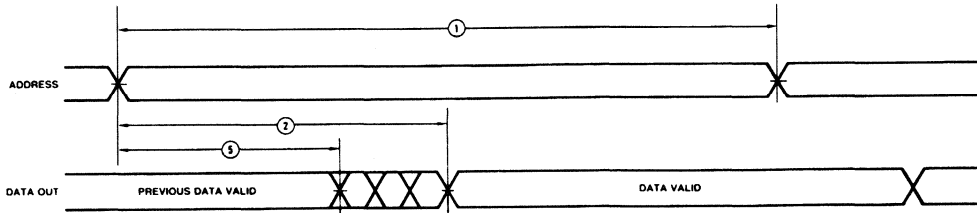
### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

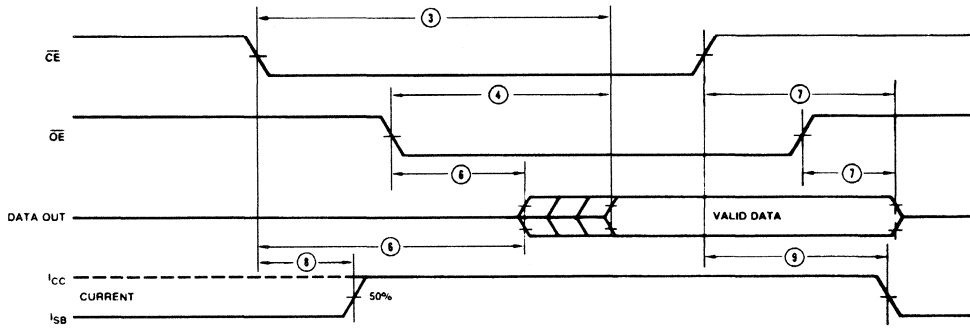
## SWITCHING WAVEFORMS (Cont'd.)

### READ CYCLE (Either Side)



WF009391

### Address Access (Notes 1 & 2)

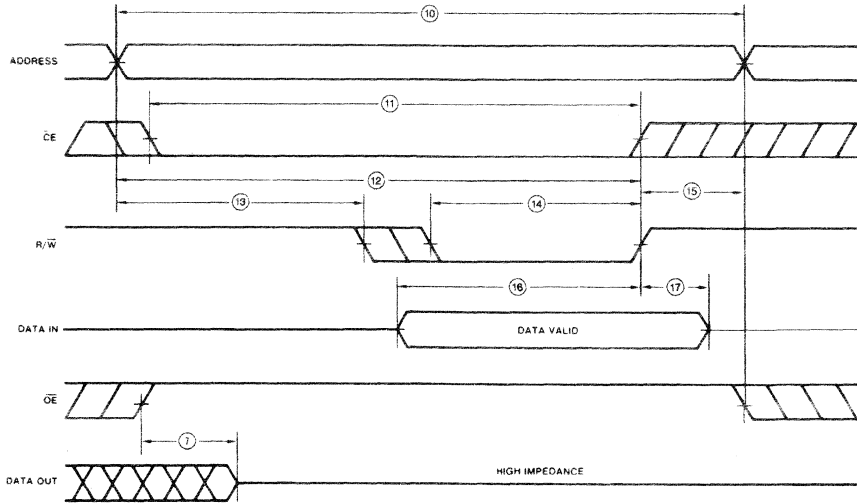


WF009401

### $\overline{CE}$ and $\overline{OE}$ -Controlled Access (Notes 1 & 3)

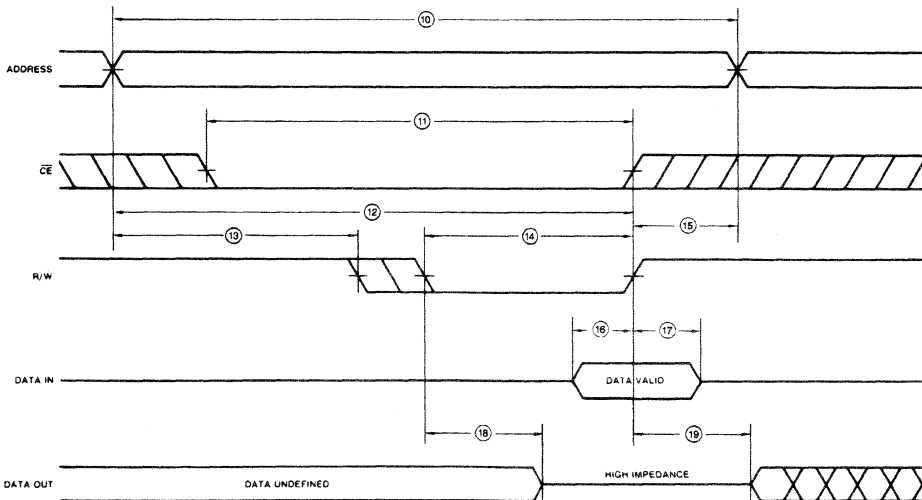
SWITCHING WAVEFORMS (Cont'd.)

WRITE CYCLE  
(Either Side — Note 4)



WF009411

$\overline{OE}$ -Controlled Data Out

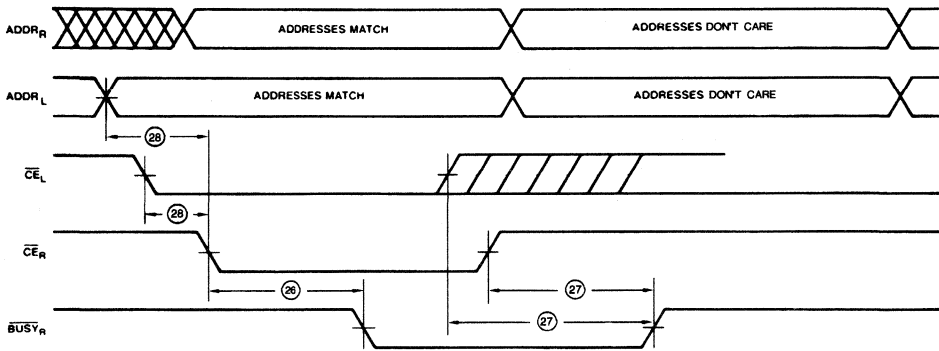


WF009421

$\overline{WE}$ -Controlled Data Out  
( $OE = V_{IL}$ )

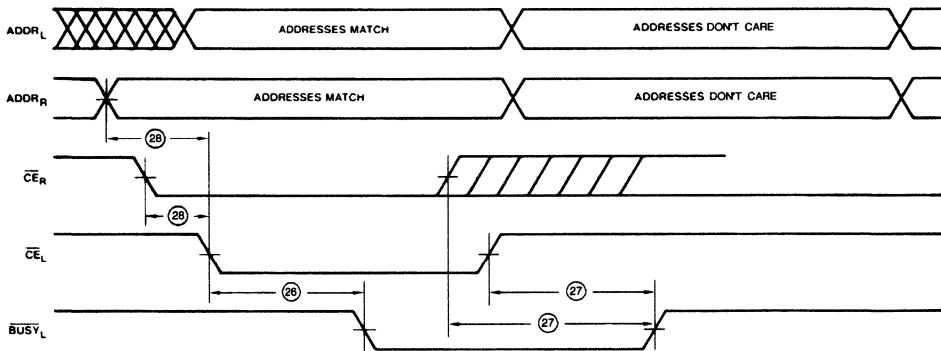
**SWITCHING WAVEFORMS (Cont'd.)**

**$\overline{\text{BUSY}}$  FLAG TIMING (1 of 2) (Note 12)**  
**(Chip Enable Arbitration)**



WF009433

**$\overline{\text{CE}}_R$  Valid Last**

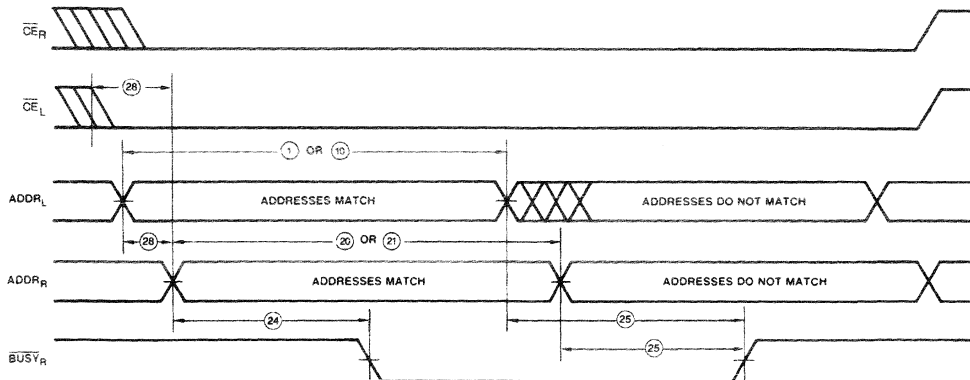


WF009434

**$\overline{\text{CE}}_L$  Valid Last**

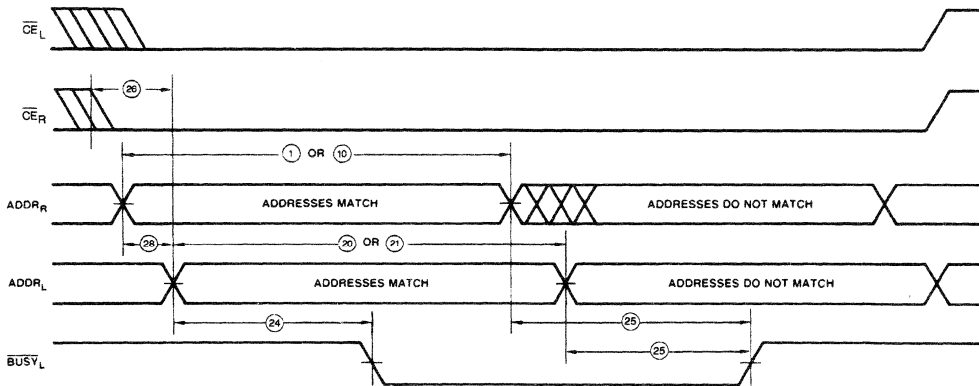
SWITCHING WAVEFORMS (Cont'd.)

BUSY FLAG TIMING (2 of 2)  
(Address Arbitration)



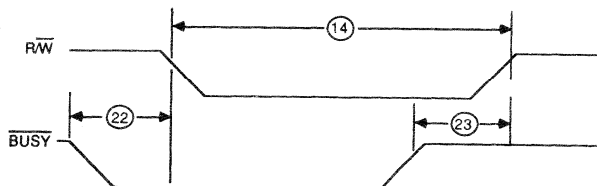
WF009443

ADDR<sub>R</sub> Valid Last



WF009444

ADDR<sub>L</sub> Valid Last



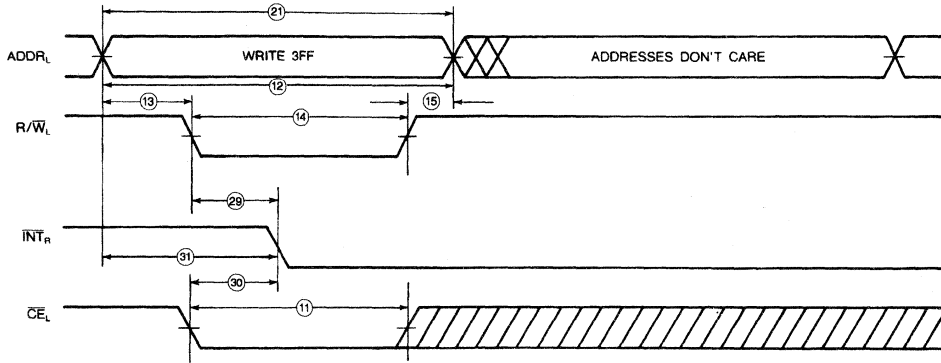
WF024680

For Am2140 Only

4

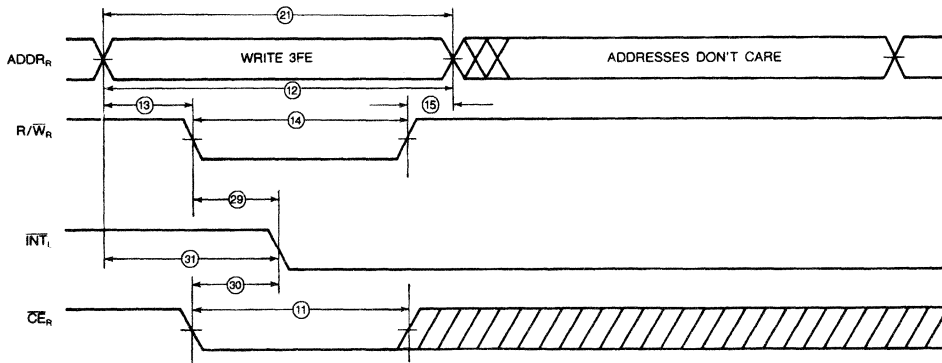
**SWITCHING WAVEFORMS (Cont'd.)**

**INTERRUPT TIMING (1 of 2)**  
**(Set INT Flag — Note 11)**



WF009486

**Left Side Flags Right Side**

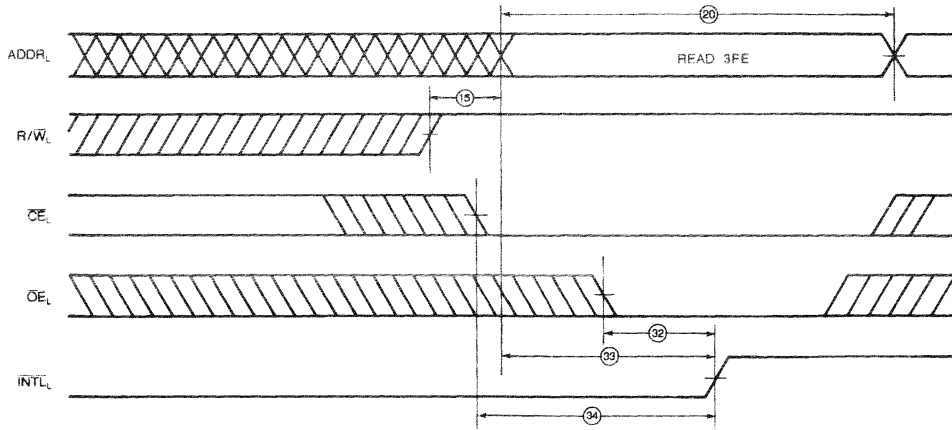


WF009487

**Right Side Flags Left Side**

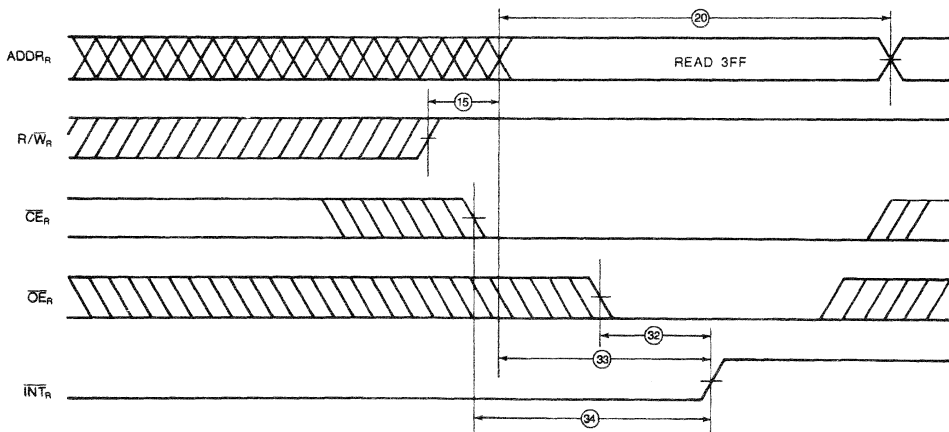
SWITCHING WAVEFORMS (Cont'd.)

INTERRUPT TIMING (2 of 2)  
(Clear INT Flag)



WF009489

Left Side Clears  $\overline{INT}_L$



WF009488

Right Side Clears  $\overline{INT}_R$

---

## Notes\*

1.  $R/\overline{W}$  is HIGH for Read Cycles.
  2. Device is continuously enabled,  $\overline{CE} = V_{IL}$ ,  $\overline{OE} = V_{IL}$ .
  3. Addresses valid prior to or coincident with  $\overline{CE}$  transition LOW.
  4. If  $\overline{CE}$  and  $R/\overline{W}$  go HIGH simultaneously, the outputs remain in the high-impedance state.
  5. Transition is measured at 1.5 V on the input to VOH – 500 mV and VOL + 500 mV on the outputs using the Load shown in Load A.
  6.  $\overline{CE}_L = \overline{CE}_R = V_{IL}$ .
  7. The  $\overline{BUSY}$  and  $\overline{INT}$  outputs are open drain. A pull-up resistor is required for system operation. For measurement purposes, Load C is used for HIGH-to-LOW transitions; output reference level is 1.5 V. Load D is used for LOW-to-HIGH transitions; output reference level is +500 mV from the output LOW voltage level.
  8. For test and correlation purposes, ambient temperature is defined as the instant-on case temperature.
  9. This parameter is guaranteed by design but is not 100% tested.
  10. Except where indicated, I/O pins use Load B.
  11. For a given port to Set or Clear an Interrupt Flag, 1) that port must have priority if addresses match and both  $\overline{CE}_L = \overline{CE}_R = \text{LOW}$ ; or 2) Addresses do not match.
  12. If the last input valid transition, which would ordinarily cause a match, occurs at the same time that the opposite port address or  $\overline{CE}$  changes to a no-match condition, then  $\overline{BUSY}$  will remain HIGH (i.e., if there is never a match, then  $\overline{BUSY}$  remains HIGH).
  13. For Slave Am2140 only.
  14. For Master Am2130 only.
  15. Absolute Maximum Ratings are intended for user guidelines and are not tested.
- \* Notes listed correspond to reference made in the following sections:
- Operating Ranges
  - DC Characteristics table
  - Switching Characteristics table
  - Switching Waveforms





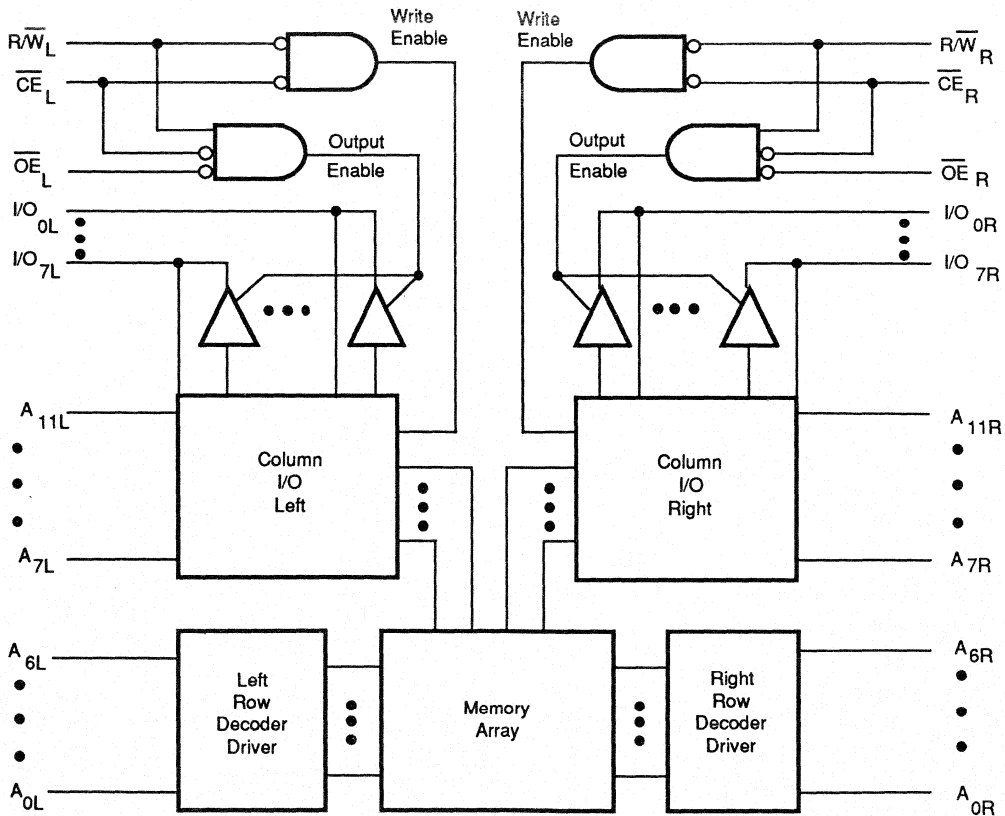
# Am99C134

## 4K x 8 Dual-Port Static Random Access Memory

### DISTINCTIVE CHARACTERISTICS

- True dual port operation
- Access time as fast as 35ns
- Low power dissipation
  - 900 mW max. operating power
  - 2.5 mW max. standby power for CMOS interface levels
- 2V Data retention capability
- Automatic power-down feature
- All inputs and outputs are TTL-compatible
- 48-pin DIP or 52-pin LCC/PLCC
- Single +5V power supply
- Advanced CMOS technology

### BLOCK DIAGRAM



11690-001A

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## GENERAL DESCRIPTION

The AM99C134 is an extremely high-speed 4K X 8 Dual-Port static RAM designed to be used in systems where on-chip hardware arbitration is not needed. This part is suitable for those systems which are to be able to externally arbitrate when both ports simultaneously access the same dual-port RAM location.

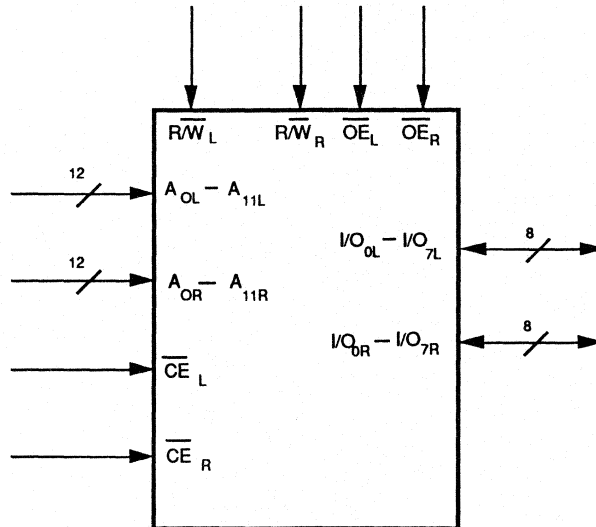
The AM99C134 has two independent ports called Left and Right port. Each port consists of an 8-bit bidirectional data bus and a 12-bit address input and necessary control signals.

The AM99C134 also has two chip enable signals corresponding to the left and right ports. Before any transaction on a port takes place, the corresponding chip enable input must be activated. If a chip enable signal is not active, the circuitry corresponding to its side automatically powers down and enters standby mode.

The AM99C134 is packaged in 48-pin DIPs or 52-pin chip carriers. All inputs and outputs are TTL-compatible and the device requires a single +5-volt power supply while operating, but will hold the data when the power supply level is maintained as low as 2V.

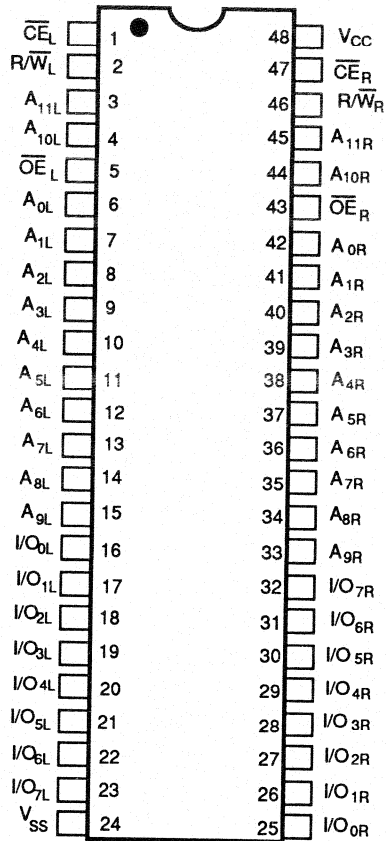
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## LOGIC SYMBOL



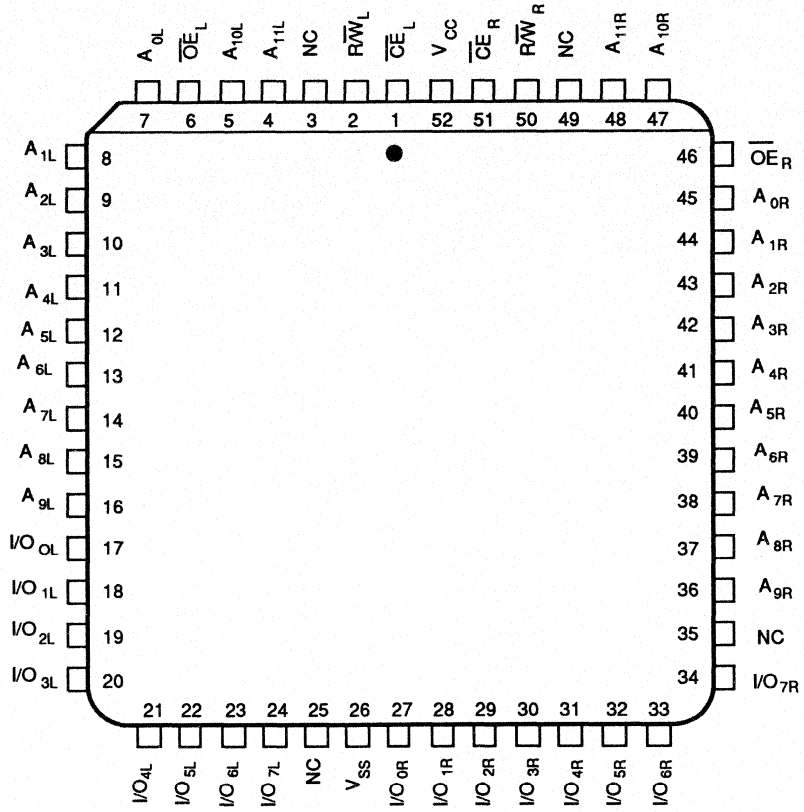
11690-002A

# CONNECTION DIAGRAM



11690-003A

# PLCC PIN CONNECTION



11690-004A

## PIN DESCRIPTION

### $A_{OL} - A_{11L}$

#### Left Port Address (Inputs)

These twelve (12) inputs constitute the memory address for the left port.  $A_0$  is the least significant bit position and  $A_{11}$  is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and low represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

### $A_{OR} - A_{11R}$

#### Right Port Address (Inputs)

These twelve (12) inputs constitute the memory address for the right port.  $A_0$  is the least significant bit position and  $A_{11}$  is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and low represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

### $\overline{CE}_L$

#### Left Port Chip Enable (Input)

This input must be LOW before any transaction from the left port and remain LOW for the duration of the transaction. When this input goes HIGH, left port logic circuits enter standby power mode and remain in this mode as long as this input remains HIGH.

### $\overline{CE}_R$

#### Right Port Chip Enable (Input)

Operation of this input is identical to  $\overline{CE}_L$  except that the  $\overline{CE}_R$  input controls the right port.

### GND

#### $V_{SS}$ Ground.

### $I/O_{OL} - I/O_{7L}$

#### Left Port Input/Output Bus (Input/Output; Three State)

These eight lines constitute the data bus for the left port. If a read operation is performed using the left port, data from the location addressed by the left port address will be available on these lines. Similarly, to perform a write operation using the left port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the  $\overline{CE}_L$  is LOW,  $\overline{OE}_L$  is LOW and  $R/\overline{W}_L$  is HIGH.

### $I/O_{OR} - I/O_{7R}$

#### Right Port Input/Output Bus (Input/Output; Three State)

These eight lines constitute the data bus for the right port. If a read operation is performed using the right port, data from the location addressed by the right port address will be available on these lines. Similarly, to perform a write operation using the left port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the  $\overline{CE}_R$  is LOW,  $\overline{OE}_R$  is LOW and  $R/\overline{W}_R$  is HIGH.

### $\overline{OE}_L$

#### Output Enable Left I/O Port (Input)

When this input is HIGH, the left port I/O bus lines are in high impedance state. If this input is LOW and  $\overline{CE}_L$  is LOW and  $R/\overline{W}_L$  is HIGH, the left port drivers are enabled and data from the location addressed by the  $A_{OL} - A_{11L}$  inputs will be available on the I/O bus lines of the left port.

### $\overline{OE}_R$

#### Output Enable Right I/O Port (Input)

When this input is HIGH, the right port I/O bus lines are in high impedance state. If this input is LOW and  $\overline{CE}_R$  is LOW and  $R/\overline{W}_R$  is HIGH, the right port drivers are enabled and data from the location addressed by the  $A_{OR} - A_{11R}$  inputs will be available on the I/O bus lines of the right port.

### $R/\overline{W}_L$

#### Left Port Read/Write Enable (Input)

This input is used to specify the left port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the  $\overline{CE}_L$  is LOW and the  $\overline{OE}_L$  is LOW and the  $R/\overline{W}_L$  is HIGH, data from the location addressed by the  $A_{OL} - A_{11L}$  will be available on the  $I/O_{OL} - I/O_{7L}$  lines.

When the  $\overline{CE}_L$  is LOW and the  $R/\overline{W}_L$  goes LOW, data present on the  $I/O_{OL} - I/O_{7L}$  lines will be written into the location addressed by the  $A_{OL} - A_{11L}$  inputs. It should be noted that the write operation is not effected by the  $\overline{OE}_L$  input. However, it is recommended that the  $\overline{OE}_L$  input be held HIGH during a write operation.

---

## $R/\overline{W}_R$

### Right Port Read/Write Enable (Input)

This input is used to specify the right port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the  $\overline{CE}_R$  is LOW and the  $\overline{OE}_R$  is LOW and the  $R/\overline{W}_R$  is HIGH, data from the location addressed by the  $A_{OR} - A_{11R}$  will be available on the  $I/O_{OR} - I/O_{7R}$  lines.

When the  $\overline{CE}_R$  is LOW and the  $R/\overline{W}_R$  goes LOW, data present on the  $I/O_{OR} - I/O_{7R}$  lines will be written into the location addressed by the  $A_{OR} - A_{11R}$  inputs. It should be noted that the write operation is not effected by the  $\overline{OE}_R$  input. However, it is recommended that the  $\overline{OE}_R$  input be held HIGH during a write operation.

## $V_{CC}$

**+5-Volt Power Supply.**

## OPERATING RANGES

### Commercial (C) Devices

Temperature ( $T_A$ )	0 to 70°C
Supply Voltage ( $V_{CC}$ )	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

# Am99C1341/Am99C1441

4096x8 Dual-Port Static Random-Access Memories



## DISTINCTIVE CHARACTERISTICS

- True dual port operation
- Access time as fast as 35 ns
- Master device (Am99C1341) has on-chip arbitration
- Expandable data bus width in multiples of 8 bits using one master (Am99C1341) and required number of slave devices (Am99C1441)
- Automatic power-down feature
- All inputs and outputs are TTL-compatible
- 52-pin PLCC
- Single +5-volt power supply
- Advanced C-MOS technology
- 2 V Data retention capability

## GENERAL DESCRIPTION

The Am99C1341 and the Am99C1441 are members of the 4K x 8 dual-port static RAM family. The Am99C1341 is designated as the master and the Am99C1441 as the slave device. The master provides the necessary control signal to the slave devices to facilitate implementing a wider data bus in a system. The master/slave concept allows expansion with minimal external logic.

Both devices have two independent ports called Left and Right port. Each port consists of an 8-bit bidirectional data bus and a 12-bit address input bus and necessary control signals.

The Am99C1341 has an on-board arbiter to resolve contention between the left and right ports. When contention between ports occurs, one port is given priority while the other port receives a busy indication.

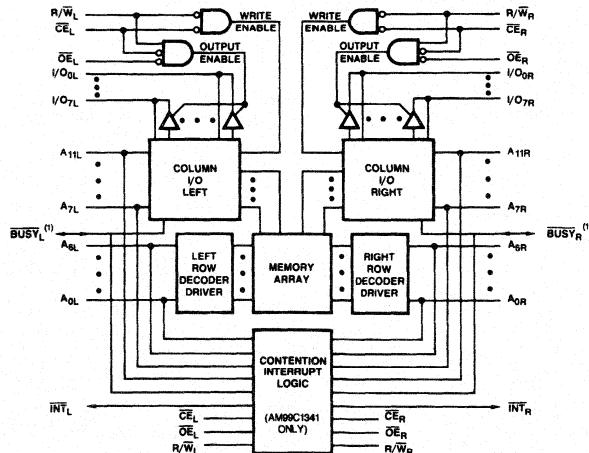
The Am99C1341 also contains on-chip facilities for supporting semaphores. Addresses (FFE)<sub>H</sub> and (FFF)<sub>H</sub> serve

as interrupt generators. If any data is written at the address (FFF)<sub>H</sub> from the left port, an interrupt signal becomes active for the right port. The interrupt signal is deactivated by reading from the right port at the same address. The address (FFE)<sub>H</sub> is used in a similar fashion by the right port to activate the interrupt signal for the left port.

The Am99C1341/Am99C1441 also have two chip enable signals corresponding to the left and right ports. Before any transaction on a port takes place, the corresponding chip enable input must be activated. If a chip enable signal is not active, the circuitry corresponding to its side automatically powers down and enters standby mode.

The Am99C1341/Am99C1441 are packaged in 52-pin plastic leaded chip carrier. All inputs and outputs are TTL-compatible and the devices require a single +5-volt power supply while operating, but will hold the data when the power supply level is maintained as low as 2 V.

## BLOCK DIAGRAM



BD008420

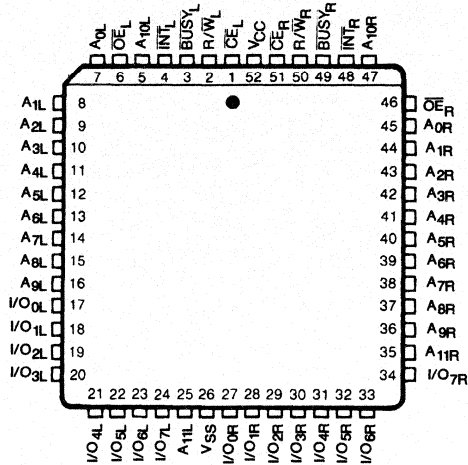
Notes: 1. Am99C1341 (Master): BUSY is open-drain output and requires pull-up resistor.  
Am99C1441 (Slave): BUSY is an input.

Publication #	Rev.	Amendment
12075	A	/0
Issue Date: March 1989		

## CONNECTION DIAGRAMS

### Top View

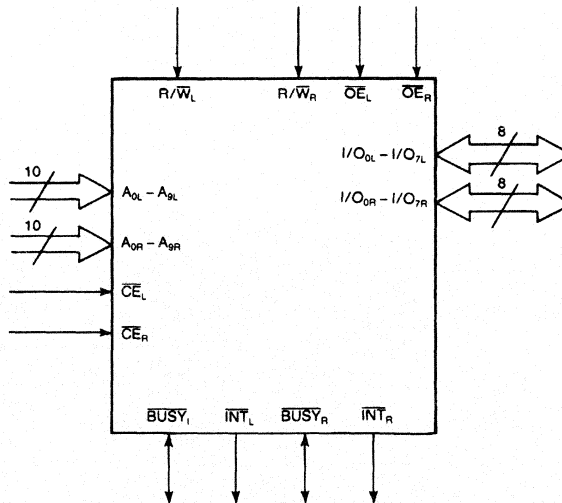
#### PLCC



CD011910

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



LS002232

$V_{CC}$  = +5-V Power Supply  
 $V_{SS}$  = Ground





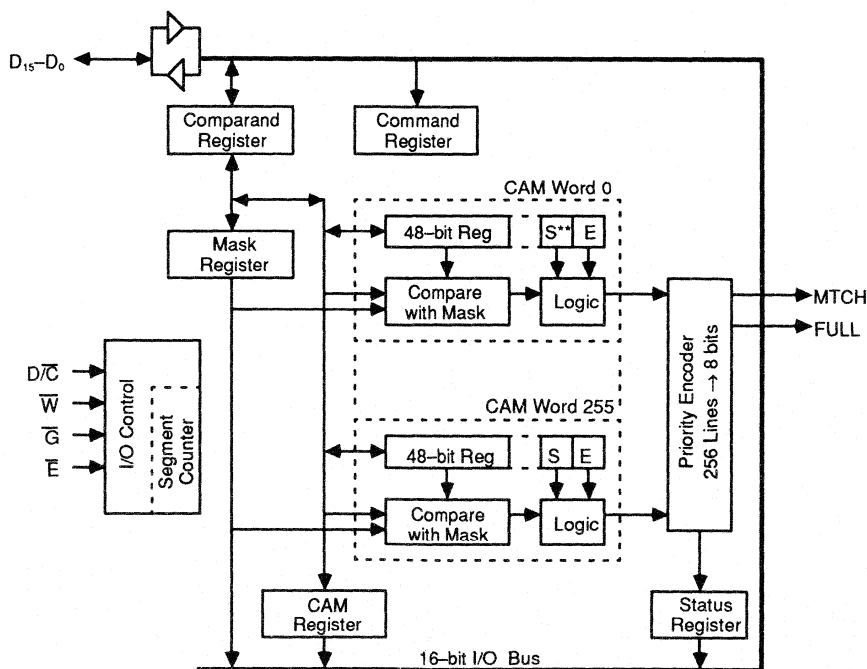
# Am99C10

## 256 x 48 Content Addressable Memory

### DISTINCTIVE CHARACTERISTICS

- 256 word x 48-bit Content Addressable Memory (CAM)
  - Optimized for Address Decoding in Local Area Networks (LAN) and bridging applications
- Each CAM word has a 48-bit register and 48-bit maskable comparator
  - Maskable-bits and maskable-words
- 48-bit input word compared against all 256 words in the CAM in a single (100ns) cycle
- Single and multiple match detection with fast on-chip priority address encoder
- Single cycle reset on all 256 words of the CAM Array
- User programmable word width of 16 bit or 48 bit
- Flexible operation and diagnostics capability through user programmable control logic
- TTL-compatible inputs and outputs
- Available in a 28-pin 400 mil CERDIP, (300 mil plastic DIP and 32-pin PLCC under development).
- Low power CMOS technology
  - 715mW max. operating power
  - 55mW max. standby

### BLOCK DIAGRAM



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## GENERAL DESCRIPTION

The Am99C10 is a high performance Content Addressable Memory (CAM) with a capacity of 256 words and a user-programmable word width of 16 bits or 48 bits. The Am99C10 is ideal for use in high speed Ethernet and FDDI local area network applications where it can function as an address filter and perform the network address look-up function. It can also find use in Database Machines, File Servers, Image Processing, Neural Networks and many other applications.

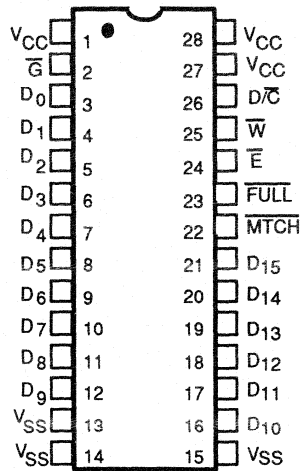
The Am99C10 CAM is composed of 256 words, each consisting of a 48-bit comparator and a 48-bit register. A block diagram of the Am99C10 is shown below. When data (the comparand) is presented to the CAM array, a simultaneous compare operation is performed between the comparand and all data (256 words) in the CAM in a single cycle. When the comparand and a word in the CAM are matched, the on-chip priority encoder generates a match word address identifying the location of the

data in the CAM. If multiple matches occur, the encoder generates the lowest matched address. Any or all bits of the comparand value can be selectively masked. The masked bits do not participate in the compare decisions, allowing comparison on a portion of the data word.

The Am99C10 is user programmable. The user can read and write to any location in the CAM Array and to all of the Am99C10 internal registers. Each word in the CAM array can be loaded with data or set to the empty state so that it does not participate in match operations. All words in the CAM Array can be set to empty in a single cycle.

The Am99C10 is manufactured with state-of-the-art CMOS processing technology. It is assembled in a 28 pin, 400 mil CERDIP; a 300 mil plastic DIP and a 32 pin PLCC are under development, and require a single 5-V power supply.

## CONNECTION DIAGRAM



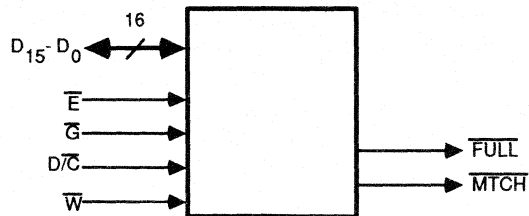
V<sub>CC</sub> = Power Supply

V<sub>SS</sub> = Ground

08125-004A

4

## LOGIC SYMBOL



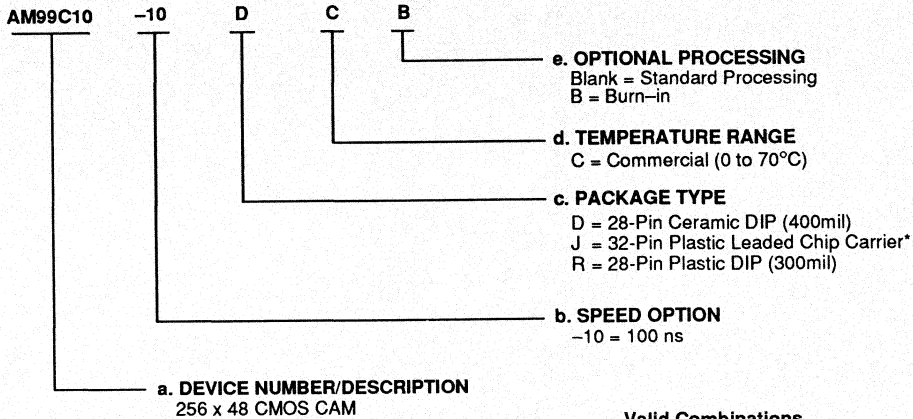
08125-002A

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM99C10	RC, RCB DC, DCB JC*, JCB*

\* Under development

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## PIN DESCRIPTION

### $\overline{D/C}$

#### Data/Command mode selection, Input, TTL

A LOW on this input selects the command mode. A HIGH on this input selects the data mode.

### $\overline{W}$

#### Write enable, Input, TTL

This pin controls the writing of the internal registers and the CAM Array. New data may be written into a register or memory by forcing the appropriate state of  $\overline{D/C}$  and  $\overline{E}$ , and by switching  $\overline{W}$  LOW and back HIGH.

### $\overline{G}$

#### Output Enable, Input, TTL

This pin controls reading of the internal registers. A LOW on both the  $\overline{E}$  and  $\overline{G}$  inputs gates the selected register onto the data bus and turns on the output drivers.

### $\overline{E}$

#### Chip Enable, Input, TTL

A LOW on this input enables the chip operations as specified by the state of  $\overline{D/C}$ ,  $\overline{W}$ ,  $\overline{G}$  inputs and the Command Register. A high on this pin powers down the chip. This signal must be low during all operations including match.

### $D_{15-0}$

#### Data Bus, 16-bit, Bidirectional, Three-state

$D_0$  is the least significant bit position and  $D_{15}$  is the most significant bit position. A HIGH on the Data Bus specifies

logic 1 and a LOW specifies logic 0. The Data Bus is not driven by the device when  $\overline{W}$  is LOW, when  $\overline{G}$  is HIGH or when chip enable  $\overline{E}$  is HIGH.

### $\overline{FULL}$

#### Address Full, Output, TTL

A LOW on this output indicates that all the words in the 256 address locations in CAM Array are full. A HIGH on this output indicates that one or more words in the CAM Array are still available or that the  $\overline{FULL}$  output is disabled. The  $\overline{FULL}$  output is in the HIGH state when  $\overline{E}$  is HIGH and is valid otherwise.

### $\overline{MTCH}$

#### Match, Output, TTL

A LOW on this output indicates that the masked data of the Comparand Register and one or more words in the CAM Array are matched. A HIGH on this output indicates that a mismatch has taken place or that the match output is disabled. The match output is in the HIGH state when  $\overline{E}$  is HIGH and is valid otherwise.

### $V_{CC}$

Power Supply Pin, Input, +5 Volts

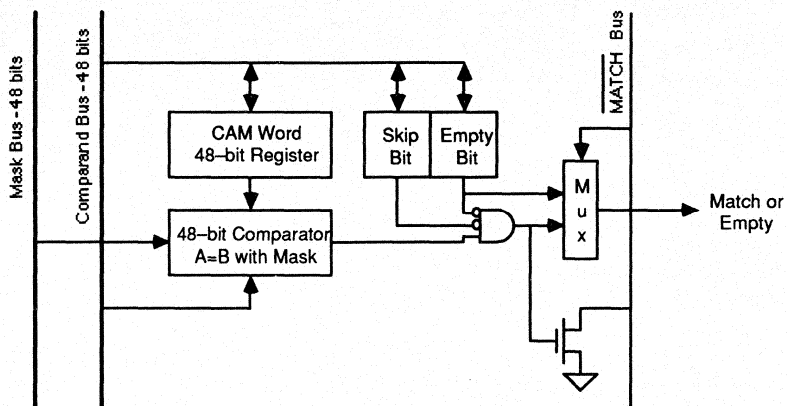
### $V_{SS}$

Ground Supply Pin, Input, 0 Volts

## FUNCTIONAL DESCRIPTION

The CAM ARRAY is a bank of 256 CAM words, each a combination of a 48 bit wide logic comparator and a 48 bit register, as shown in Figure 1. The CAM Array compares a 48 bit input data word against all of its 256 words simultaneously for logic equality in one cycle. If any of the CAM Array 256 words find an exact match with the incoming bit pattern, the CAM Array raises a Match flag and outputs the 8 bit address of the matching word.

When a Match cycle is initiated, every CAM word compares each bit in its register against the appropriate bit of the incoming 48 bit pattern. Additionally, a logic "1" (HIGH level) set in any Mask Register bit will disable that bit position in the CAM Array. A match is declared if all enabled CAM cells find an exact comparison with the input data. The CAM Array word that finds a match activates an internal signal called the Match Line (ML). There are 256 match lines: ML0-ML255.



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Figure 1. CAM Word Block Diagram

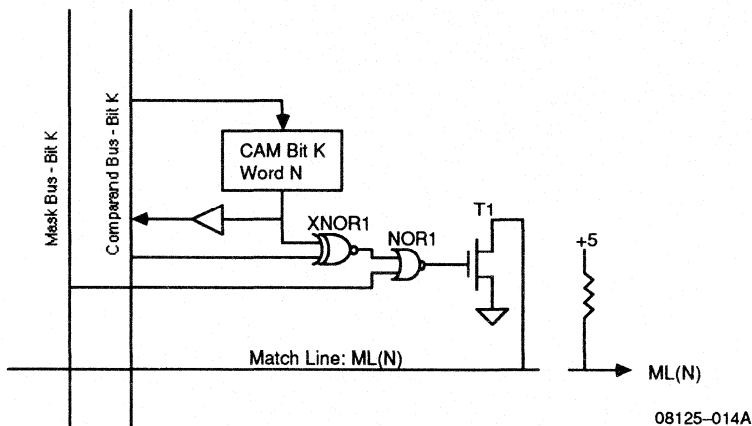


Figure 2. CAM Bit Block Diagram

Each CAM word consists of 48 CAM data bits. Each CAM data bit consists of a register bit latch, an exclusive-NOR comparator, an OR gate for masking, and a transistor for performing a 48-bit wire-AND across the 48 data bits, as shown in Figure 2. The logic comparator exclusive-Nors the contents of the register bit with the corresponding bit of the Comparand Register. A match between the two bits result in a HIGH level at the output of the exclusive-Nor gate (XNOR1). The output of XNOR1 is further gated (Nor function) with a bit of the Mask Register. A HIGH level on either one of the inputs to NOR1 forces its output LOW, indicating a match. The ML signal will stay HIGH (indicating a match for that CAM word) if all 48 CAM cells of this word have their T1 transistors shut off by their NOR1 gates. If any one of the 48 NOR1 outputs is HIGH, the ML line will be forced LOW, indicating a mismatch.

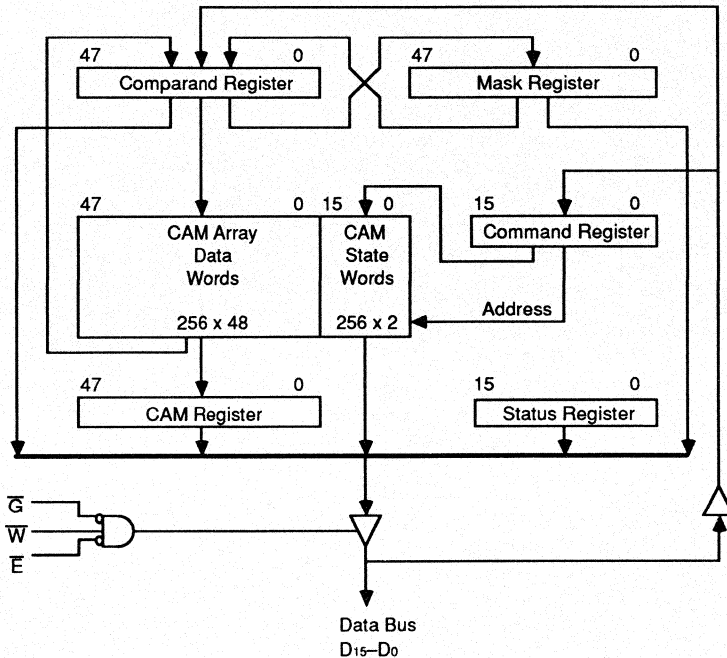
The Priority Encoder identifies the address of the CAM word that found a match. All 256 comparators of the CAM Array receive the same bit pattern for matching at the same time, and more than one of them can find a match with the masked data. All 256 ML lines are presented to the Priority Encoder block that decides which comparator of the ones that activate their MLs has the lowest address. If at least one ML is active the Priority Encoder will activate the  $\overline{MTCH}$  line and at the same time will set the  $\overline{MTC}$  bit in the Status Register. The Priority Encoder will transfer the 8 bit address of the lowest matching CAM Array word to the Status Register.

Each of the 256 words of the CAM Array has two additional bits of memory associated with it – A Skip bit and an Empty bit. These are shown in the CAM Word Block Diagram. The actual size of the CAM is therefore 256 X 50 (48+2). Both the Skip and the Empty bits can disable a match for their word. The Skip bit can be used in situations where there are multiple matches – it gives the user the ability to detect additional words that were matched other than the one with the lowest address. The Empty bit indicates available or empty addresses in the CAM into which data can be written.

The Empty bit is also used by the Priority Encoder. The Priority Encoder identifies the lowest address of an Empty CAM Array word if no match occurred in any of the 256 words. If a match operation did not result in a positive match (the  $\overline{MTCH}$  signal is HIGH) and if the CAM Array is not full (the  $\overline{FULL}$  signal is HIGH) the Priority Encoder will generate the lowest empty address. The 8 bit empty address is accessed by reading the Status Register.

### CAM Registers - Reading and Writing

The Am99C10 has 5 programmable registers involved in data transfers. The Command and Status registers are 16 bits wide, and the Comparand, Mask and CAM registers are 48 bits wide. Figure 3. is a model of the Am99C10 registers and their interaction with each other and the CAM Array. Table 1 lists the registers and their respective data sources and destinations.



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Figure 3. CAM Register Transfer Model

Table 1. Am99C10 Registers

Register	Type	Size	Direction	Data Source	Destination
Command	Cmd	16	Input	D-Bus	-
Status	Cmd	16	Output	-	D-Bus
Comparand	Data	48	In / Out	D-Bus, CAM Array Mask Register	D-Bus, CAM Array Mask Register
Mask	Data	48	Output	Comparand Register	D-Bus, Comparand Register
CAM	Data	48	Output	CAM Array	D-Bus

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## Data Bus Transfers

All data is transferred to and from the CAM over the 16-bit bidirectional Data Bus. Data transfer is controlled by a combination of 4 control signals ( $\bar{E}$ ,  $D/\bar{C}$ ,  $\bar{W}$ , and  $\bar{G}$ ), as described in the Pin Description section.

Data is written into the Am99C10 by placing the data on the Data Bus and activating  $\bar{W}$  and  $\bar{E}$ . When  $D/\bar{C}$  is low (Command Write cycle), the input data is loaded into the

Command Register. When  $D/\bar{C}$  is high (Data Write cycle), the input data is loaded into the Comparand Register.

Data is read from the Am99C10 (output drivers enabled) when  $\bar{G}$  and  $\bar{E}$  are low and  $\bar{W}$  is high. When  $D/\bar{C}$  is low (Status Read cycle) the Status register is gated onto the Data Bus. When  $D/\bar{C}$  is high (Data Read cycle) one of the data registers is gated onto the Data Bus. This register is selected by the contents of the Command register.



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Prior to reading, a command is loaded into the Command Register to select which of the internal registers is to be read.

Data can be read from any register by loading the appropriate command into the Command register; however, data can be written only to the Comparand register. Data to be written to the Mask register or to the CAM array must first be written into the Comparand register and transferred to the Mask register or CAM array word by writing the appropriate transfer command to the Command register.

### 48-bit Data Transfers

Data is transferred to and from the Am99C10 in 16-bit words. Data for the 16-bit Command and Status registers are transferred in one read or write cycle. Data for the 48-bit Comparand, Mask and CAM registers are transferred to and from the chip in three cycles. Data transfer to and from each 48-bit register is done by dividing each register into three 16-bit segments. A two-bit counter, the Segment Counter is used to select which segment of a 48-bit register is to be loaded or read.

The Segment Counter is a two-bit binary counter that counts from 0 to 2 (modulo-three). It can be preset by writing a command code of "B", "C" or "D" to the Command register. In all three commands bits 10 and 11 (S0, S1) define the binary value (0, 1 or 2) to be preset into the counter. Note that a value of 3 (S1, S0 = 11) in these bits will result in a value of 0 in the counter. The counter is also reset to 0 by the Initialize command, command code "0".

The Segment Counter is incremented after each data read or write cycle if the CAM is in the 48-bit mode. This allows a 48-bit register to be loaded or read in three successive cycles. The counter is clocked by the LOW-to-HIGH transition of  $\overline{W}$  in case of a Data Write cycle and by the LOW-to-HIGH transition of  $\overline{R}$  in case of a Data Read cycle.

When the Am99C10 is set to 48-bit mode, the user will normally execute 3 Data Write cycles or 3 Data Read cycles in sequence to transfer a 48 bit data word. At the end of such sequence the state of the Segment Counter is equal to its initial state before the data transfer began. This allows continuous 48-bit transfers without having to preset the Segment Counter between words. This is useful in the CAM's normal operating mode of checking a stream of 48-bit words for a match.

Note that reading a 16-bit State word requires only one cycle. If the CAM is in the 48-bit mode, this data read operation will increment the Segment Counter. Any subsequent cycles that use the Segment Counter have to take this into account.

### 16-bit Mode Data Transfers

In 16 bit mode the Segment Counter is not incremented and it points to one of the three segments of the Com-

parand, Mask and CAM Registers. Writing and reading the selected segment of those registers is achieved in one cycle. However, internal transfers between the registers and the CAM Array as well as the Match operation are done on all 48 bits.

### CAM Array-Reading and Writing

To write a word into the CAM Array, the data is first loaded into the Comparand register and then transferred from the Comparand register to the register in the selected CAM word by executing a transfer command. The transfer command is executed by writing a command word (command code = 6 or E) into the Command register. The transfer command contains the address of the CAM word to be written.

To read a word from the CAM Array, data is transferred from the CAM array to either the Comparand or CAM registers by writing the appropriate command (command code = 7 or D, respectively) into the Command register. The transfer command contains the address of the CAM word to be read. The CAM Array word is then read from the register selected by the command.

Writing into the Skip or Empty bit in a CAM word is done directly by writing the appropriate command code (command code = 9 or A, respectively) into the Command register. The command word contains the value of the Skip or Empty bit to be written and the address of the CAM word containing the bit.

The same command codes (9 or A) which are used to set a specific Skip or Empty bit can also be used to set all Skip or Empty bits in the CAM array. If bit 11 of these command words is a one, the address portion of the command is ignored and the value of the Skip or Empty bit is written into all words of the CAM array. This is useful in clearing all Skip and Empty bits.

The Skip and Empty bits of a CAM word are also cleared to zero when data is written into the CAM using command code E. This allows writing a new word of data into an empty CAM word without requiring an extra cycle to clear the Skip and Empty bits.

The Skip and Empty bits of all CAM words can be preset to the empty state by writing an Initialize command (command code = 0) to the Command register. Initialize clears all Skip bits to zero and sets all Empty bits to one, corresponding to an empty CAM condition.

To read the Skip and Empty bits of a word from the CAM Array, the State Memory is selected as the source of data driving the Data Bus by writing the appropriate command (command code = 5) into the Command register. That command contains the address of the CAM word whose state is to be read. The State word (i.e., the Skip and Empty bits of the CAM Array word) are then read directly. Reading the State word requires only one Data Read cycle.

## Match Operations

Comparison of data in the Comparand against the 256 words of data in the CAM array is called a match operation. The result of a match operation is a match address which appears in the Status register and the activation of the  $\overline{MTCH}$  and  $\overline{FULL}$  flags. Match operations require one cycle (100 ns) for valid flags and two cycles (200 ns) before status read operations can be started.

A match operation can be initiated by writing a command into the Command register or by writing data into the Comparand register. A match operation begins after a single data write to the Comparand Register in 16-bit mode or after three data write cycles to the Comparand Register in 48-bit mode. Note that the  $\overline{E}$  line must be kept low for the match time,  $t_{MPE}$  (200 ns) after the write to allow the match to occur.

If a match occurs, the  $\overline{MTC}$  bit is set in the Status register and the  $\overline{MTCH}$  pin is activated if it has been enabled. The address of the word that matched appears in the lower 8 bits of the Status register. If more than one match occurs, the  $\overline{MUL}$  flag is set in the status register, indicating a multiple match. In this case, the match address is that of the match word with the lowest numerical address. If no match occurs, the  $\overline{MTC}$  bit and  $\overline{MTCH}$  flag are not set, and the address is that of the first empty word, i.e. the empty word with the lowest address.

$\overline{MTC}$  is the same flag as  $\overline{MTCH}$ . The match flag  $\overline{MTC}$  and multiple match flag  $\overline{MUL}$  cannot be disabled by the Command Write. These flags respond each time new data is written into the Comparand Register.

In 48-bit mode, the match output  $\overline{MTCH}$  is disabled and held HIGH until the Segment Counter reaches zero, ( $S1 = L$  and  $S0 = L$ ) even if the match output has been enabled by the Command Write operation. In the 16-bit mode, the Segment Counter state does not affect the match output  $\overline{MTCH}$ .

The match flag access time is measured from a low-to-high transition of  $\overline{W}$  to high-to-low transition of  $\overline{MTCH}$  flag.

## Match and Full Flags

The Am99C10 has two output signals that indicate its status - Full,  $\overline{FULL}$  and Match,  $\overline{MTCH}$ .

The Full signal,  $\overline{FULL}$ , indicates whether the CAM Array is full or not. A low level on  $\overline{FULL}$  indicates that all 256 words of the CAM Array are full. A high on this output indicates that one or more words in the CAM Array are still available or that the  $\overline{FULL}$  output is disabled. The  $\overline{FULL}$  output can be disabled (= HIGH) under program control or when the chip is disabled (Chip Enable  $\overline{E}$  is high).

The Match signal,  $\overline{MTCH}$ , indicates whether a match has been detected, i.e. that the masked data of the Comparand Register and one or more words in the CAM Array are matched. A high on this output indicates that a mismatch has taken place or that the match output is disabled. The  $\overline{MTCH}$  output can be disabled (= HIGH) under program control or when the chip is disabled (Chip Enable  $\overline{E}$  is high).

## Status Register Format

The Status register shows the results of match operations and the contents of the Segment Counter. The State Register is read onto the Data Bus by executing a Status Read cycle. Since it takes time to encode a match address ( $t_{MPE}$ ), the Status Read cannot immediately follow a Command Write cycle or a Data Write cycle if a valid match address is sought. A time delay of ( $t_{MPE}$ ) after the last command or data write before reading the Status register will guarantee proper address encoding. A Status Read operation does not affect the state of the flags or other register contents.

The Status Register has 3 fields - the Address field ( $A_0 - A_7$ ), the Segment Counter State ( $S0 - S1$ ) and the Flags field ( $\overline{MTC}$ ,  $\overline{MUL}$  and  $\overline{FUL}$ ), as shown in Figure 4.

### $\overline{MTC}$

A LOW on  $\overline{MTC}$  ( $D_{15}$ ) indicates that at least one word in the CAM Array and the masked data of the Comparand Register are matched. A HIGH indicates that no word in the CAM Array found a match. The  $\overline{MTC}$  flag is the same as the match output signal  $\overline{MTCH}$  except the  $\overline{MTC}$  flag cannot be disabled.

### $\overline{MUL}$

A LOW on  $\overline{MUL}$  ( $D_{14}$ ) indicates that two or more words in the CAM Array match the masked data of the Comparand Register. It is activated during a Match operation and latched by an internal clock at the end of the Match cycle.

### $\overline{FUL}$

A LOW on  $\overline{FUL}$  ( $D_{13}$ ) indicates that the CAM Array is full. The  $\overline{FUL}$  flag is the same as the full output signal  $\overline{FULL}$  except the  $\overline{FUL}$  flag cannot be disabled. It is activated during a Match operation and latched by an internal clock at the end of the Match cycle.

### $S1, S0$

The Segment Counter bits ( $S0 - S1$ ) are driven by the two flip-flops that comprise the Segment Counter. These two bits ( $D_{10}$  and  $D_{11}$ ) reflect the current state of the Segment Counter.

15	14	13	12	11	10	9	8	7	0
$\overline{MTC}$	$\overline{MUL}$	$\overline{FUL}$	0	S1	S0	0	0	Address	

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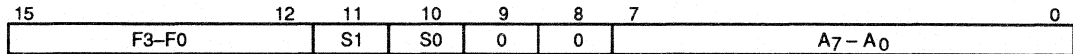
Figure 4: Status Word Bit Assignment

### A<sub>7</sub>-A<sub>0</sub>

Lowest address of the matched word in the CAM when data in the Comparand Register and the data in the CAM are matched (MTCH = L, MTC = L and FULL = don't care). Lowest address of empty 48-bit word in the CAM when data is mismatched and the CAM is not full (FULL = H). Address is undefined when data is mismatched and CAM is full.

### Command Register Format

The Am99C10 can execute a variety of commands. Each command is executed by writing the appropriate command word to the Command register. All commands are executed during the write pulse applied to the write clock,  $\overline{W}$ . The format of the Command Register is shown in Figure 5, and a summary of the commands is shown in Table 2.



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- F3-F0: A 4 bit Instruction Code which defines one of sixteen commands.  
 S0 - S1: Modifier bits for the various commands.  
 A<sub>0</sub> - A<sub>7</sub>: An Address field which selects one of the 256 CAM Array data or State words.

**Figure 5: Command Register Bit Assignment**

**Table 2. 99C10 Command Summary**

Op Code	Operation		S1	S0	A <sub>0</sub> -A <sub>7</sub>	Start Match
0	Initialize		X	X	X	X
1	Flag Output control enable/disable		MTCH	FULL	X	X
2	16/48 bit Mode Select		48-bit	X	X	X
3	Comparand Reg. --> Mask Reg		X	X	X	Start
4	Mask Reg. --> Comparand Reg.		X	X	X	Start
5	SIM --> Data Bus		X	X	CAM State	X
6	Comparand Reg. --> CAM Array		X	X	CAM Data	Start
7	CAM Array --> Comparand Reg.		X	X	CAM Data	Start
8	Reserved		X	X	X	X
9	Skip Control	Per Word All Words	0 1	Skip Skip	CAM State X	Start
A	Empty control	Per Word All Words	0 1	Empty Empty	CAM State X	Start
B	Comparand Reg. --> Data Bus		Segment Counter		X	X
C	Mask Reg. --> Data Bus		Segment Counter		X	X
D	CAM Array --> CAM Reg. --> Data Bus		Segment Counter		CAM Data	X
E	Comparand Reg. --> CAM Array, clear S + E		X	X	CAM Data	Start
F	Reserved		X	X	X	X

## Am99C10 COMMAND DESCRIPTIONS

### Op Code 0 Initialization

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0												
Not Used															

08125-019A

All Skip-bits are set to "0" (LOW level) meaning—don't skip, and all Empty-bits are set to "1" (HIGH level) meaning—empty. This is equivalent to resetting the CAM Array. The MTCH and FULL outputs are enabled. The mode is

set to 48-bit mode. The Mask Register and Segment Counter are reset to zero. Subsequent data writes and reads are to and from the Comparand Register.

### Op Code 1 Flag Output Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	S1	S0										
Not Used															

08125-020A

This command controls the enable and disable of the  $\overline{\text{FULL}}$  and  $\overline{\text{MTCH}}$  status output pins. The S0 and S1 fields of this command are latched into the control logic. Once loaded, they control the status output pins  $\overline{\text{FULL}}$  and  $\overline{\text{MTCH}}$  as follows: When S0 is 0, the  $\overline{\text{FULL}}$  output is disabled and remains unconditionally HIGH. When S0

is 1, the  $\overline{\text{FULL}}$  output is enabled and may be asserted when  $\overline{\text{E}}$  is low. When S1 is 0, the  $\overline{\text{MTCH}}$  output is disabled and remains unconditionally high. When S1 is 1, the  $\overline{\text{MTCH}}$  output is enabled and may be asserted if  $\overline{\text{E}}$  is low.

### Op Code 2 Mode Select

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	S1											
Not Used															

08125-021A

This command sets the 99C10 into the 16-bit or 48-bit mode. The S1 bit in the command is loaded into the 16/48-bit mode control register. The 16-bit mode is enabled when S1 is 0, and the 48-bit mode is enabled

when S1 is 1. The Am99C10 will remain in the mode selected until another Command Write is executed with Op Code "0" or "2".

### Op Code 3 Move Comparand Register to Mask Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1												
Not Used															

08125-022A

The 48-bit contents of the Comparand Register is loaded into the Mask Register. The Segment Counter is

not affected. A Match cycle will begin automatically following this command.

### Op Code 4

#### Move Mask Register to Comparand Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	Not Used											

08125-023A

The 48-bit contents of the Mask Register is loaded into the Comparand Register. The Segment Counter is not

changed. A Match cycle will begin automatically following this command.

### Op Code 5

#### Enable Output from State Memory to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	Not Used				A <sub>7</sub> - A <sub>0</sub>							

08125-024A

This command selects a State word in the CAM Array as the source of data to be read. The Skip-bit and Empty-bit appear on bits D<sub>14</sub> and D<sub>15</sub> of the Data Bus, all other bits

of the bus are driven LOW. The Segment Counter is not changed.

### Op Code 6

#### Move Comparand Register to CAM Array

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1		1	Not Used				A <sub>7</sub> - A <sub>0</sub>							

08125-025A

The 48-bit contents of the Comparand Register are written into the CAM Array data word. The 16/48 bit mode select setting does not affect this instruction. The Empty-bit and Skip-bit in the State Memory are not

changed. The CAM Array address is specified by the Command Register address field. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

### Op Code 7

#### Move CAM Array to Comparand Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	Not Used				A <sub>7</sub> - A <sub>0</sub>							

08125-026A

The 48-bit contents of the CAM Array data word specified by the address field are loaded into the Comparand Register. The Segment Counter is not changed. The

State Memory is not changed. The 16/48 bit mode select setting does not affect this instruction. A Match cycle will begin automatically following this command.

### Op Code 8

#### Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	Not Used											

08125-027A

**Op Code 9**  
Skip-bit Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	S0	Not Used		A <sub>7</sub> -A <sub>0</sub>							

08125-028A

When bit 11 in the Command Register is LOW, S0 is loaded into the Skip-bit within the State word location specified by the Command Register address field.

A Match cycle will begin automatically following this command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	S0	Not Used									

08125-029A

When bit 11 in the Command Register is HIGH, S0 is loaded into all skip-bit memory locations. The Segment

Counter is not changed. A Match cycle will begin automatically following this command.

**Op Code A**  
Empty-bit Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	S0	Not Used		A <sub>7</sub> -A <sub>0</sub>							

08125-030A

When bit 11 in the Command Register is LOW, S0 is loaded into the Empty-bit within the State word location specified by the Command Register address field. A

Match cycle will begin automatically following this command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	1	S0	Not Used									

08125-031A

When bit 11 in the Command Register is HIGH, S0 is loaded into all Empty-bit memory locations. The Segment

Counter is not changed. A Match cycle will begin automatically following this command

**Op Code B**  
Enable Output from Comparand Register to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	S1	S0	Not Used									

08125-032A

This command selects the Comparand Register as the source of data to be read. The S0 and S1 data in the Command Register are clocked into the Segment Counter at the end of this Command Write cycle. When S0 and S1 are 11, the Segment Counter is reset to zero.

Subsequent Data Read operations result in data flowing from the Comparand Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle will automatically increment the modulo-three Segment Counter.

### Op Code C

#### Enable Output from Mask Register to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	S1	S0	Not Used									

08125-033A

This command selects the Mask Register as the source of data to be read. The S0 and S1 data in the Command Register are clocked into the Segment Counter at the end of this Command Write cycle. When S0 and S1 are 11, the Segment Counter is reset to zero. Subsequent

Data Read operations result in data flowing from the Mask Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle will automatically increment the modulo-three Segment Counter.

### Op Code D

#### Move CAM to CAM Register, Enable Output from CAM Register to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	S1	S0	Not Used	A <sub>7</sub> - A <sub>0</sub>								

08125-034A

This command selects the CAM Register as the source of data to be read. The S0 and S1 data in the Command Register are moved to the Segment Counter. When S0 and S1 are 11, the Segment Counter is reset to zero. The CAM Array word specified by the address field is transferred to the CAM Register. Subsequent Data

Read operations result in data flowing from the CAM Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle automatically increments the modulo-three Segment Counter.

### Op Code E

#### Move Comparand Register to CAM (Set Empty-bit and Skip-bit LOW)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	Not Used				A <sub>7</sub> - A <sub>0</sub>							

08125-035A

The 48-bit contents of the Comparand Register is written into the CAM Array data word specified by the address field. The 16/48 bit mode select setting does not affect this instruction. Both the Empty-bit and the Skip-bit in the State Memory address specified by the Com-

mand Register address field are set cleared to zero (Not Empty and Don't Skip). The Segment Counter is not changed. A Match cycle will begin automatically following this command.

### Op Code F

#### Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	Not Used											

08125-036A

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## Typical Command Sequences

The following are examples of some common sequences of commands.

### Power-up Initialization

After power-up, the CAM must be initialized. This is done by executing the Initialize command. All the CAM words are reset to the empty state, and the device is set

up in the 48-bit mode. Another command is needed if the 16-bit mode is desired.

#### For 48-bit mode:

Command Write 0000 = Initialize (16/48 mode is set automatically to 48 bit mode)

#### For 16-bit mode:

Command Write 0000 = Initialize (16/48 mode is set automatically to 48 bit mode)

Command Write 2000 = Mode Select (S1=0, Set mode to 16 bit)

### Loading CAM Array with Data

After initialization, the CAM must be loaded with data in order to be used. Since all locations are initialized to the empty state, the CAM can be loaded starting from address zero. This is done by loading the Comparand reg-

ister and writing a command with an op code of E, which will transfer the data to a specified CAM word and clear the Skip and Empty bits of that word.

Filling the CAM in the 48-bit mode is normally done using the following command sequence:

Data Write (D<sub>15</sub> -- D<sub>0</sub> --> Comparand Register (15-0))

Data Write (D<sub>15</sub> -- D<sub>0</sub> --> Comparand Register (31-16))

Data Write (D<sub>15</sub> -- D<sub>0</sub> --> Comparand Register (47-32))

Command Write E0XX = Comparand Register --> CAM Array + Clear S+E  
(Repeat for every CAM Array word to be loaded.)

Filling the CAM in the 16-bit mode is done using the following command sequence:

Command Write BX00 = Comparand Register --> Data Bus (Load Segment Counter)

Data Write (D<sub>15</sub> -- D<sub>0</sub> --> Comparand Register) (segment selected by counter)

Command Write E0XX = Comparand Register --> CAM Array + Clear S+E (all 48 bits are written).

Repeat the last two steps for every CAM Array word to be loaded.

Repeat all three steps when a different 16 bit segment is to be loaded.

### Load Mask Register

The mask register is loaded by writing the data into the Comparand Register and then writing a command to

transfer the data from the Comparand register to the Mask register.

Data Write (D<sub>15</sub> -- D<sub>0</sub> --> Comparand Register (15-0))

Data Write (D<sub>15</sub> -- D<sub>0</sub> --> Comparand Register (31-16))

Data Write (D<sub>15</sub> -- D<sub>0</sub> --> Comparand Register (47-32))

Command Write 3000 = Comparand Register --> Mask Register



---

## 48 bit Compare for Match (48-bit Mode)

To perform a match operation on new data, the data to be tested is written into the Comparand register, time is allowed for the match operation to be performed, and then the match flag and match address are read from the

Data Write (D<sub>15</sub> -- D<sub>0</sub> -->Comparand Register (15-0))

Data Write (D<sub>15</sub> -- D<sub>0</sub> -->Comparand Register (31-16))

Data Write (D<sub>15</sub> -- D<sub>0</sub> -->Comparand Register (47-32))

Wait one cycle (allow time for Match operation - 2 cycles if Status read)

Check  $\overline{MTC}$  output pin, or Status Read, check bits 15, 14 and 13 ( $\overline{MTC}$ ,  $\overline{MUL}$ ,  $\overline{FUL}$ )

Status register. Note that no special command is required to start the match: it begins after the last word is loaded into the Comparand register.

## Check for Multiple Matches

Typical match operations yield a single match. Some applications, however may yield multiple matches. In this case, the addresses of each match may be read by

successively reading the current lowest address, setting its Skip bit, and reading the next lowest address, etc., until no matches are left.

Status Read, bit 15 ( $\overline{MTC}$ ) = 0, bit 14 ( $\overline{MUL}$ ) = 0

Status bits 7-0 contain the address of the lowest word in the CAM that found a match.

Read and save the match address, use it to form the next command

Command Write 94XX = Skip Control - F(9), set bit 11(S1) = 0, set bit 10 (S0) = 1(Skip),

Set the Skip bit: Command bits 7-0 to the lowest matching word address.

Wait two cycles for the next Match operation to complete and the Status register to settle  
Status Read

Check  $\overline{MTC}$  for match, save the address if  $\overline{MTC}$  =0

Status bits 7-0 contain the address of the lowest word in the CAM that found a match.

Read and save the match address, use it to form the next command

Repeat the last three steps until there are no more matches

## Finding and Loading an Empty Location

A CAM word may be empty since initialization or it can be declared empty by setting its Empty bit. Data is added to the CAM by finding an empty location and writing into it. This is done by loading the data to be written into the Comparand register and checking for a match. If the

data is not already stored in the CAM, the match operation will respond with the address of the lowest empty word. (If a match was found, a copy of the data already exists in the CAM.) The address of the empty word is used to write the new data into the empty word.

Data Write (D<sub>15</sub> -- D<sub>0</sub> -->Comparand Register (15-0))

Data Write (D<sub>15</sub> -- D<sub>0</sub> -->Comparand Register (31-16))

Data Write (D<sub>15</sub> -- D<sub>0</sub> -->Comparand Register (47-32))

Wait two cycles (allow time for Match operation and priority encode)

Status Read, check bits 15 ( $\overline{MTC}$ ) should be 1, and 13 ( $\overline{FUL}$ ) should be 1,

Bits 0-7 contain the address of the lowest empty word in the CAM.

Command Write E0XX = Comparand Register -->CAM Array + Flags,

Bits 0-7 should have the address of the empty word from the Status Read.

## Reading Data

To read the contents of a word in the CAM Array

Command Write D0XX = CAM Array -->CAM Register -->Data Bus,

Bits 0-7 indicate the address of the word to be read.

Data Read - (CAM Register (15-0) -->D<sub>15</sub>- D<sub>0</sub>)

Data Read - (CAM Register (31-16) -->D<sub>15</sub>- D<sub>0</sub>)

Data Read - (CAM Register (47-32) -->D<sub>15</sub>- D<sub>0</sub>)

## Example of a Command Sequence

Table 3 shows the control signals, data bus contents and Segment Counter contents for a typical command sequence. The sequence consists of initialization, filling the CAM Array, and loading the Mask Register. A data

pattern is then loaded into the Comparand Register, a match is executed and the sequence terminates with the reading of the Status Register.

Table 3. Command Sequence Example

Cycle Type	Instruction	E	D/C	W	G	Data Bus (Hex)		Segment Counter		Operation
						Before	After	Before	After	
Command Write	Initialize	L	L	C	H	0 X X X	XX	00		Set default conditions
Data Write	—	L	H	C	H	3 2 1 0	00	01		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (15-0)
Data Write	—	L	H	C	H	7 6 5 4	01	10		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (31-16)
Data Write	—	L	H	C	H	B A 9 8	10	00		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (47-32)
Command Write	Comparand Reg. → CAM	L	L	C	H	E 0 0 0	00	00		"BA9876543210" into CAM word 0
⋮	⋮					⋮		⋮		⋮
Data Write	—	L	H	C	H	1 1 1 1	00	01		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (15-0)
Data Write	—	L	H	C	H	2 2 2 2	01	10		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (31-16)
Data Write	—	L	H	C	H	4 4 4 4	10	00		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (47-32)
Command Write	Comparand Reg. → CAM	L	L	C	H	E 0 F F	00	00		"444422221111" into CAM word 255
Data Write	—	L	H	C	H	0 0 F F	00	01		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (15-0)
Data Write	—	L	H	C	H	0 0 0 0	01	10		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (31-16)
Data Write	—	L	H	C	H	F F 0 0	10	00		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (47-32)
Command Write	Comparand Reg. → Mask Reg.	L	L	C	H	3 0 0 0	00	00		"FF00000000FF" into Mask Register
Data Write	—	L	H	C	H	7 6 5 4	00	01		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (15-0)
Data Write	—	L	H	C	H	B A 9 8	01	10		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (31-16)
Data Write	—	L	H	C	H	F E D C	10	00		D <sub>15</sub> -D <sub>0</sub> → Comparand Reg (47-32)
Wait (Match)	—	L	X	H	H	X X X X	00	00		Compare "XXDCBA9876XX" against CAM
Wait (Encode)	—	L	X	H	H	X X X X		00		Encode match address → Status reg
Status Read	—	L	L	H	C	Status	00	00		Check Flags

L = LOW  
H = HIGH  
C = LOW going pulse

08125-037A

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## CAM Applications

Content Addressable Memory (CAM) devices have many potential applications. The availability of high density CAM devices such as the Am99C010 will allow

many applications to be developed which were not practical in the past because of lack of CAM devices. Some of these application areas are:

Local Area Network (LAN) bridge address filtering  
Local Area Network (LAN) ring message insertion and removal

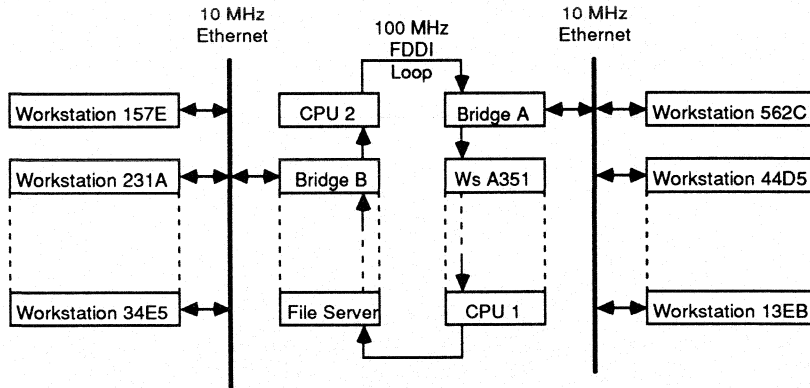
Data base machine support - Search and sort accelerators  
Pattern recognition - String search engines, etc.  
Image processing and machine vision - Pattern recognition, Image registration, etc.  
Neural net simulation  
AI language support - (LISP, etc.) garbage collection support, PROLOG accelerators, etc.

## Local Area Network Bridge Address Filtering

Bridges between high speed Local Area Networks (LAN) provide a good example of CAM use. A LAN bridge provides transparent communication between two networks. An example is a bridge between a

100MBit/second FDDI network and an Ethernet network. A block diagram of such a network system is shown in Figure 6, and a block diagram of the bridge is shown in Figure 7.

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08125-038A

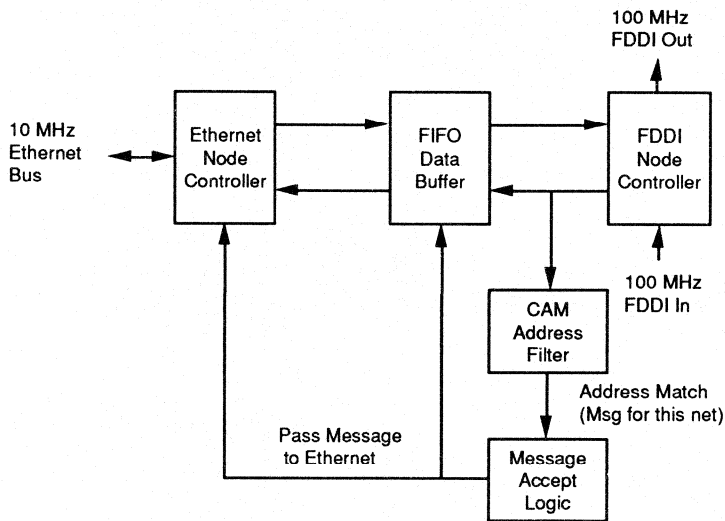
Figure 6: FDDI-Ethernet Network System

The function of the FDDI-Ethernet bridge is to pass messages between the two networks in order to allow the various workstations to communicate. Messages are sent according to unique 48-bit addresses assigned to each workstation. Each message contains the source address and the destination address. The notations shown in the workstation boxes in Figure 6 are assumed to be examples of these addresses: e.g. 157E, 231A, etc.. F

Let us assume that workstation 562C sends a message to workstation 231A. In order for this to occur, the first FDDI-Ethernet bridge must pass along the address to the FDDI loop. The second bridge must recognize that the message is for one of the workstations on its Ethernet LAN and pass it along to workstation 231A.

The problem for the FDDI-Ethernet bridge is to recognize-in time-that the message is for a station on its Ethernet LAN and no other. There could be 4000 workstations on the Ethernet LAN. This means that the bridge must check the message destination address against 4000 addresses in order to determine whether to accept the message and pass it on to the Ethernet.

Address identification must be done quickly. The message acceptance decision must be made before the arrival of the next message, i.e. within the minimum message time. If the minimum message length is 9 bytes on a 100 mbit/sec FDDI network, the decision must be made in 720 ns, including 480 ns to acquire the address. The Am99C10 can do the job in 480+100=580 ns. At these speeds, the Am99C10 is not only effective, it is the only practical, cost effective approach.



08125-039A

Figure 7: FDDI-Ethernet Bridge Block Diagram

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C  
Voltage on Any Pin with Respect to GND -0.5 to +7.0 V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

### Commercial (C) Devices

Case Temperature (T<sub>c</sub>) 0 to +85°C  
Supply Voltage (V<sub>CC</sub>) +4.75 to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS are valid over the operating range unless otherwise specified. All values are guaranteed maximum type limits.**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I <sub>OH</sub>	Output High current	V <sub>OH</sub> = 2.4 V, V <sub>CC</sub> = 4.5 V	-1.6		mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	+2.4		mA
V <sub>IH</sub>	Input High Voltage		2.2	V <sub>CC</sub> + .5	V
V <sub>IL</sub>	Input LOW Voltage	(Note 3)	-0.5	0.8	V
I <sub>Ix</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		2.0	μA
I <sub>Oz</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> $\bar{E} \geq V_{IH}$ or $\bar{G} \geq V_{IH}$		2.0	μA
I <sub>CC1</sub>	Static Operating Supply Current	$\bar{E} \geq V_{IL}$		70	mA
I <sub>CC2</sub>	Dynamic Operating Supply Current, 48-bit mode	Cycle = 48-bit Data Write $\bar{E} \geq V_{IL}$ , f = 1/t <sub>wc</sub>		110	mA
I <sub>CC3</sub>	Dynamic Operating Current, 16-bit mode	Cycle = 16-bit Data Write $\bar{E} \geq V_{IL}$ , f = 1/t <sub>wc</sub>		130	mA
I <sub>SB1</sub>	Standby Current TTL Input Levels	$\bar{E} \geq V_{IH}$ V <sub>CC</sub> = Max		10	mA
I <sub>SB2</sub>	Standby Current CMOS Input Levels	$\bar{E} \geq (V_{CC} - 0.2V)$ ; V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ (V <sub>CC</sub> - 0.2)		10	mA

## AC CHARACTERISTICS

Parameter Symbol	Parameter Description	Min.	Max.	Unit	Note
<b>Common Parameters</b>					
t <sub>DCS</sub>	D/C, E setup before read or write	0		ns	
t <sub>DCH</sub>	D/C, E hold time after read or write	5		ns	
<b>Read Cycle Parameters</b>					
t <sub>RC</sub>	Read cycle time	100		ns	
t <sub>RP</sub>	Read cycle pulse width	75			8
t <sub>RR</sub>	Read recovery time	25		ns	
t <sub>OLZ</sub>	Output enable time to low Z	10		ns	4,8
t <sub>OHZ</sub>	Output disable time to high Z	5	30	ns	4,6
t <sub>RA</sub>	Read access time		65	ns	
t <sub>FA</sub>	Flag enable time		30	ns	4
t <sub>FH</sub>	Flag disable time		30	ns	4
<b>Write Cycle Parameters</b>					
t <sub>WC</sub>	Write cycle time	100		ns	
t <sub>WP</sub>	Write pulse width	75			8
t <sub>WR</sub>	Write recovery time	25		ns	7
t <sub>DS</sub>	Data setup time before write	0		ns	
t <sub>DH</sub>	Data hold time after write	5		ns	
t <sub>MAF</sub>	Match time to flags after write		100	ns	7
t <sub>MPE</sub>	Match priority encode time after write		200	ns	7
t <sub>MA</sub>	Match access time to Status after write		t <sub>MPE</sub> + t <sub>RA</sub>		

### Notes:

1. Absolute maximum ratings are intended for user guidelines and are not tested.
2. Ambient temperature is defined as the instant-on case temperature.
3. Undershoot to -3.0 V for 10 ns maximum between the 50 amplitude points is permissible.
4. Parameter guaranteed by design and characterization data but not 100 tested.
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance (see test load A in switching test circuits) unless otherwise noted. Output timing reference is 1.5 V.
6. Test load B. Disable time is measured as the time to a +500 mV change from prior output level.
7.  $\overline{E}$  must be low and  $\overline{W}$  must be high for t<sub>MAF</sub> during the match cycle following command or data write for the internal circuitry to generate the match.
8.  $\overline{W}$  and  $\overline{G}$  may not overlap: i.e., may not both be low at the same time (while  $\overline{E}$  is low).

### CAPACITANCE\*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
CI	Input Capacitance	F = 1 MHz, V <sub>IN</sub> = 0 V		10	pF
CI/O	Input/Output Capacitance	F = 1 MHz, V <sub>IO</sub> = 0 V		10	pF

### Notes:

1. These parameters are guaranteed by characterization but not tested. Measurements performed at T<sub>A</sub> = +25°C.





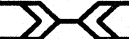
## Data Transfer Control Signals

OPERATION MODE	CONTROL SIGNALS				DATA BUS	SUPPLY CURRENT
	$\overline{E}$	$D/\overline{C}$	$\overline{W}$	$\overline{G}$		
Command Write	L	L	L	H	Data In	$I_{CC1}, I_{CC2}$
Data Write	L	H	L	H	Data In	$I_{CC1}, I_{CC2}, I_{CC3}$
Status Read	L	L	H	L	Data Out	$I_{CC1}, I_{CC2}$
Data Read	L	H	H	L	Data Out	$I_{CC1}, I_{CC2}$
Output Disabled	L	X	H	H	Hi - Z	$I_{CC1}$
Standby	H	X	X	X	Hi - Z	$I_{SB1}, I_{SB2}$
Invalid	L	X	L	L	Hi - Z	—

08125-003A

# SWITCHING WAVEFORMS

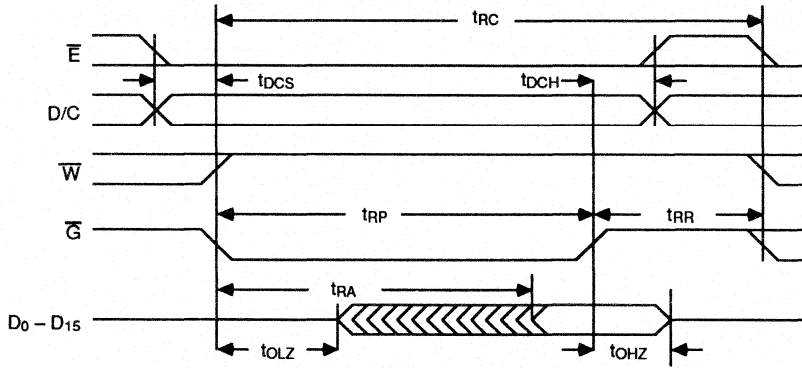
## Key To Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H TO L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care, any change permitted	Changing, state unknown
	Does not apply	Center line is high impedance "off" state

KS000010

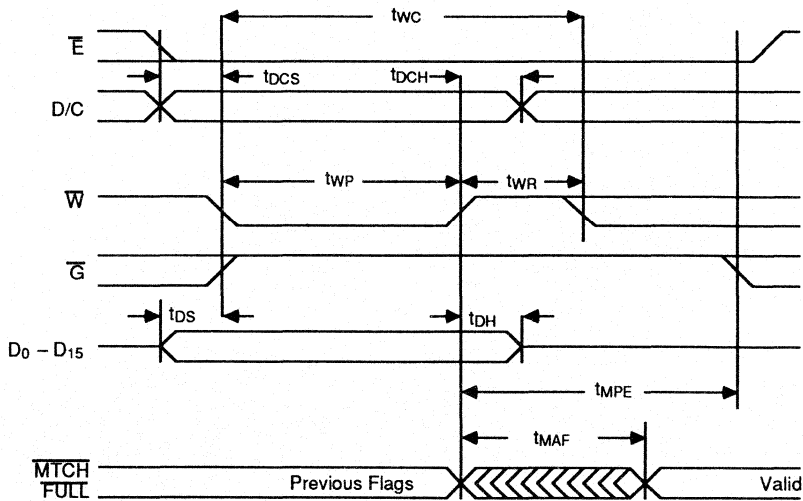


## Read Timing Diagram



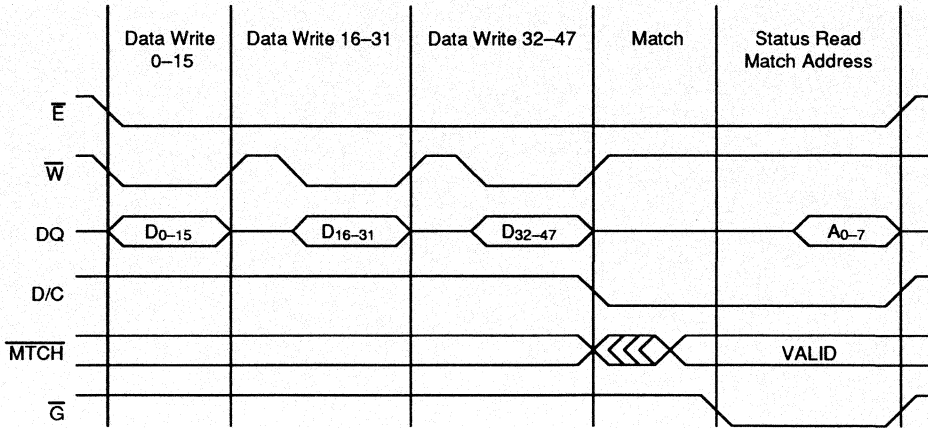
08125-008A

## Write Timing Diagram



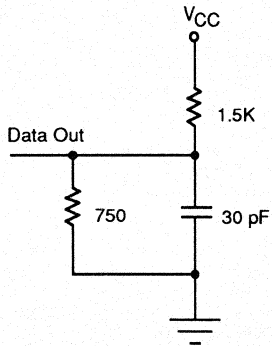
08125-009A

## Match Timing Diagram (Reference)



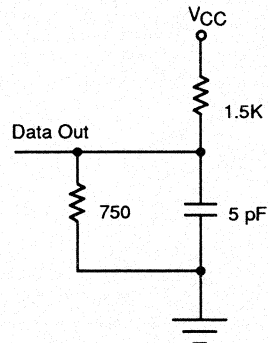
08125-010A

## SWITCHING TEST CIRCUITS



08125-011A

**Test Load A**

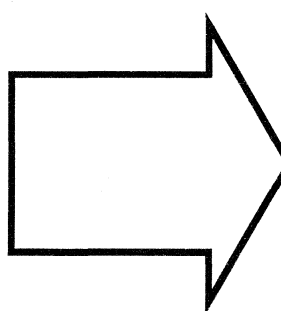


08125-012A

**Test Load B**



Advanced  
Micro  
Devices



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# Am27C43

## 32,768-Bit (4096 x 8) High-Performance CMOS PROM

### DISTINCTIVE CHARACTERISTICS

- High-speed (35 ns)/ Low-power (90 mA) CMOS EPROM Technology
- Direct plug-in replacement for Bipolar PROMS – JEDEC approved pin-out
- Slim 300-mil DIP
- 5-Volt  $\pm 10\%$  power supplies for both Commercial and Military
- UV-erasable and reprogrammable provides exceptionally high programming yields (Typ. >99.9%)
- ESD Immunity > 2000V

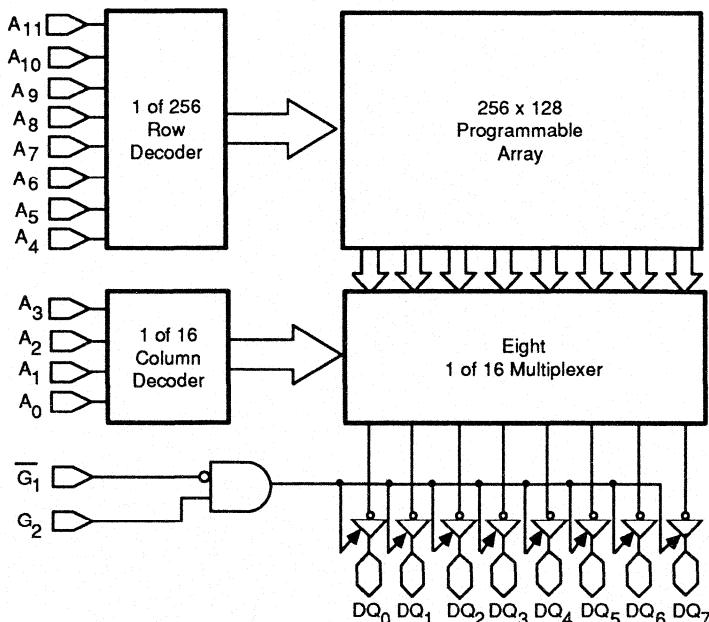
### GENERAL DESCRIPTION

The Am27C43 (4,096 words by 8 bits) is a high-speed CMOS programmable Read-only memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the

requirements of a variety of microprogrammable controls, mapping functions or code conversion. This device utilizes proven floating gate EPROM technology to ensure high reliability, ease of programming and exceptionally high programming yields.

### BLOCK DIAGRAM



5

11967-001A

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## PRODUCT SELECTOR GUIDE

<b>Part Number</b>	Am27C43–35	Am27C43–45
<b>Address Access Time</b>	35 ns	45 ns
<b>Operating Range</b>	COM'L/MIL	COM'L/MIL

---

### OPERATING RANGES

#### Commercial (C) Devices

Ambient Temperature ( $T_A$ )	0 to +75°C
Supply Voltage ( $V_{CC}$ )	+4.5 to +5.5 V

#### Military (M) Devices\*

Case Temperature ( $T_C$ )	-55 to +125°C
Supply Voltage ( $V_{CC}$ )	+4.5 to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

*\* Military product 100% tested at  $T_C = +25^\circ\text{C}$ ,  $+125^\circ\text{C}$  and  $-55^\circ\text{C}$ .*





# Am27C45

16,384-Bit (2048 x 8) High-Performance CMOS REGISTERED PROM

## DISTINCTIVE CHARACTERISTICS

- High-speed (20 ns) setup time (10 ns) clock-to-output/Low-Power (90 mA) CMOS EPROM Technology
- Direct plug-in replacement for Bipolar PROMs
- Slim 300-mil DIP & 28 pin square LCC packaging available
- 5-Volt  $\pm 10\%$  power supplies for both Commercial and Military
- UV-erasable and reprogrammable provides exceptionally high programming yields (Typ. > 99.9)
- ESD immunity > 2000 V

## GENERAL DESCRIPTION

The Am27C45 (2048 words by 8 bits) is a high performance CMOS Programmable Read-Only Memory (PROM), incorporating D-type master-slave data registers on chip. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of micro-programmable controls and state machines.

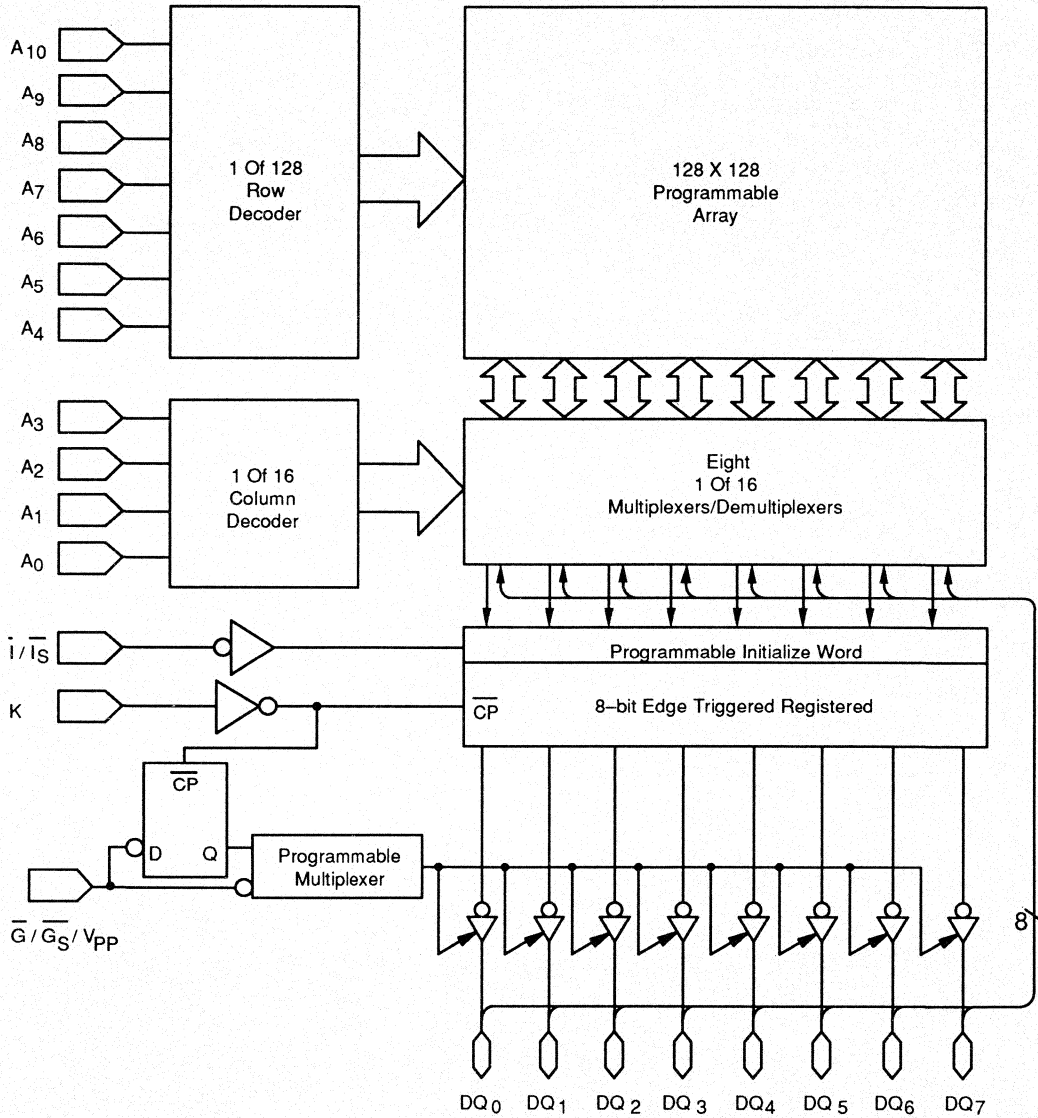
This device contains an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

This device contains a single pin initialize function capable of loading any arbitrary microinstruction for system interrupt or initialization.

To offer the system designer maximum flexibility, this device contains user-programmable architecture for output Enable & Initialize. The unprogrammed state of these pins operates as Asynchronous inputs ( $\bar{G}$ ) and ( $\bar{I}$ ) respectively. An architecture word permits the programming of the functionality of these pins to Synchronous Enable ( $\bar{G}_s$ ) and Synchronous Initialize ( $\bar{I}$ ).

If the architecture has been programmed to Synchronous Enable ( $\bar{G}_s$ ), upon power-up the outputs ( $DQ_0$ - $DQ_7$ ) will be in a floating or high impedance state.

# BLOCK DIAGRAM



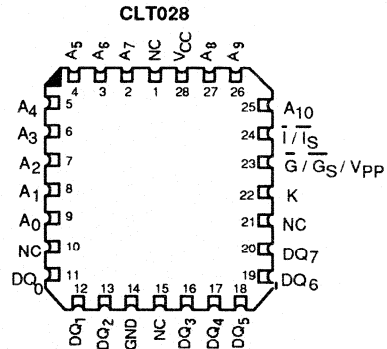
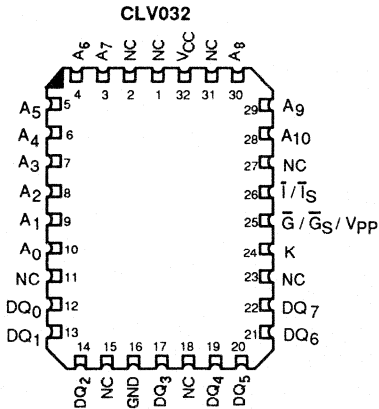
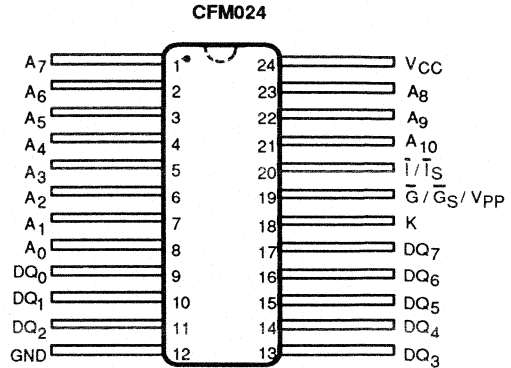
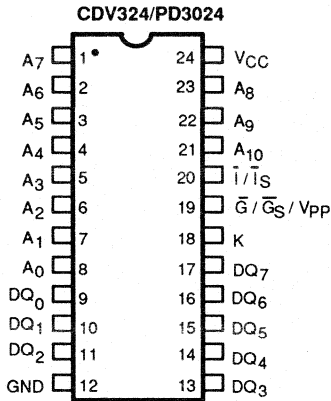
11945-001A

## PRODUCT SELECTOR GUIDE

Part Number	Am27C45-20	Am27C45-25	Am27C45-35
Address Set-up Time	20 ns	25 ns	35 ns
Clock-to-Output Delay	10 ns	12 ns	15 ns
Operating Range	COM'L	COM'L/MIL	COM'L/MIL

## CONNECTION DIAGRAMS

### Top View

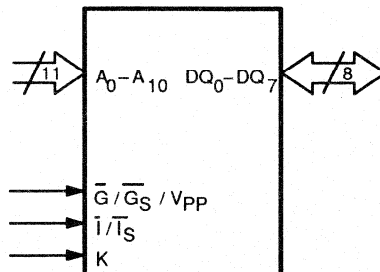


Note: Pin 1 is marked for orientation.

Note: Pin 1 is marked for orientation.

11945-002A

## LOGIC SYMBOL



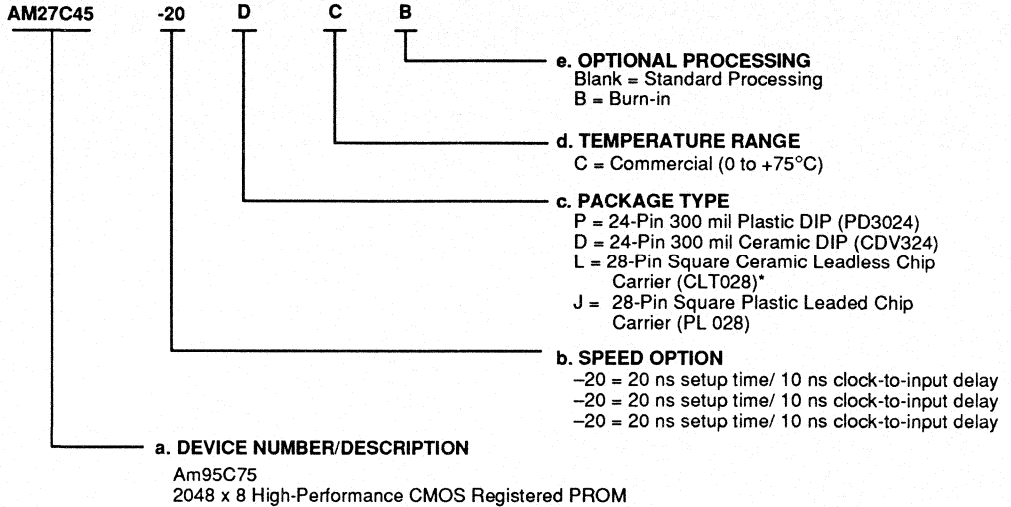
11945-003A

# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27C45-20 AM27C45-25 AM27C45-35	PC, PCB, DC, DCB, LC, LCB, JC, JCB

\*Preliminary; Package in Development

### Valid Combinations

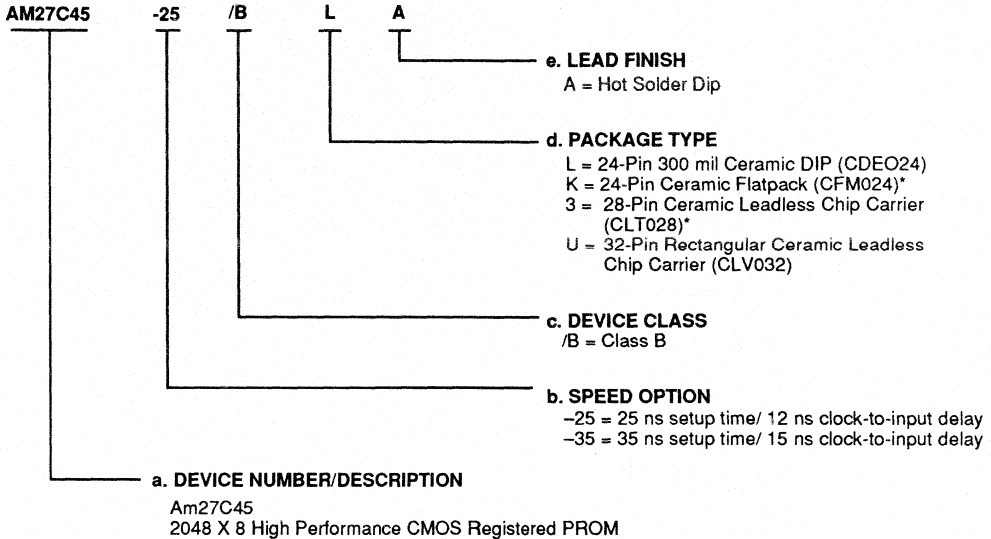
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliance with MIL-STD-883C requirements. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (If applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



**5**

Valid Combinations	
AM27C45-25 AM27C45-35	/BLA, /BKA, /B3A, /BUA

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

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## PIN DESCRIPTION

**A<sub>0</sub>-A<sub>10</sub>**

### Address Lines (Inputs)

The 11-bit field presented at the address inputs selects one of 2048 memory locations to be read from.

**K**

### Clock (Input)

The clock is used to load data into the parallel data registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

**DQ<sub>0</sub>-DQ<sub>7</sub>**

### Data Port (Input/Outputs; Three State)

The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which, when disabled, are in a floating or high-impedance state. These pins provide the data input for programming the memory array.

**$\bar{I}$**

### Asynchronous Initialize (Input)

Control pin used to initialize the output data registers from a programmable word independent of K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

**$\bar{I}_S$**

### Synchronous Initialize (Input)

Control pin used to initialize the output data registers from a programmable word in conjunction with K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

**$\bar{G}/V_{PP}$**

### Asynchronous Output Enable/(V<sub>PP</sub>) Programming Power (Input)

Provides direct control of the DQ output three-state buffers. When raised to a voltage > 12.0 V, the  $\bar{G}/V_{PP}$  pin provides the programming power to program the memory array.

**$\bar{G}_S$**

### Synchronous Output Enable (Input)

Control the state of the DQ output three-state buffers in conjunction with K. This is useful where more than one registered PROM is bussed together for word-depth expansion. In this case, the enable becomes the most significant address bit and as such, must be synchronized with the data.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient Temperature with Power Applied	-55 to +125°C
Supply Voltage	-0.5 V to +7.0 V
DC Voltage Applied to Outputs in High-Impedance State	-0.5 V to +7.0 V
DC Programming Voltage (V <sub>PP</sub> )	14 V
DC Input Voltage	-0.5 V to +7.0 V
Electrostatic Discharge Protection (per MIL-STD-883 Method 3015.2)	> 2000 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature (T <sub>A</sub> )	0 to +75°C
Supply Voltage (V <sub>CC</sub> )	+4.5 V to +5.5 V

### Military (M) Devices\*

Case Temperature (T <sub>C</sub> )	-55 to +125°C
Supply Voltage (V <sub>CC</sub> )	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\* Military product 100% tested at T<sub>C</sub> = +125°C, +125°C, and -55°C

## DC CHARACTERISTICS over operating range unless otherwise specified

(for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Descriptions	Test Conditions	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 1)	2.0		V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 1)		0.8	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		0.4	V
V <sub>CL</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>CL</sub> = -18.0 mA	-1.2		V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 5.5 V		10	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.0 V		-10	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = Max. V <sub>OUT</sub> = 0.0 V (Note 2)	-20	-90	mA
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 5.5 V V <sub>G/GS</sub> = 2.4 V V <sub>OUT</sub> = 0.0 V		40 -40	μA μA
I <sub>CC</sub>	Operating Supply Current	V <sub>CC</sub> = Max. (Note 3) All Inputs = V <sub>IH</sub> All Inputs = V <sub>IL</sub>		90	mA

### Notes:

- V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. **Do Not** attempt to test these values without suitable equipment and fixturing.
- Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
- Operating I<sub>CC</sub> is measured with all inputs except G/Gs switching between V<sub>IL</sub> and V<sub>IH</sub> at a timing interval equal to TAVKH. The outputs are disabled via G/Gs held at 3.0V.

## Capacitance\*

Parameter Symbol	Parameter Descriptions	Test Conditions	Typ.	Unit
C <sub>IN</sub>	Input Capacitance (G/V <sub>PP</sub> )	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C	9	
	Input Capacitance (All Others)		5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> /V <sub>OUT</sub> = 2.0 V @ f = 1 MHz	8	pF

\*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

(for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Number	Parameter Symbol	Parameter Description	Am27C45						Unit
			-20		-25		-35		
			COM'L Only Min.	COM'L Only Max.	COM'L Only Min.	COM'L Only Max.	COM'L Only Min.	COM'L Only Max.	
1	TAVKH	Address Valid to K HIGH Setup Time	20		25		35		ns
2	TKHAX	Address Valid to K HIGH Hold Time	0		0		0		ns
3	TKHDQV1	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW)		10		12		15	ns
4	TKHKL TKLKH	Clock Pulse Width (HIGH or LOW)	15		15		20		ns
5	TGLDQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (Notes 3 & 4)		15		15		20	ns
6	TGHDQZ	Asynchronous Output Enable HIGH to Output Hi-Z (Notes 2 & 4)		15		15		20	ns
7	TGSVKH	$\overline{G}_s$ Valid to K HIGH Setup Time (Note 5)	12		12		15		ns
8	TKHGSX	$\overline{G}_s$ to K HIGH Hold Time (Note 5)	5		5		5		ns
9	TKHDQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs (Notes 3 & 5)		15		15		20	ns
10	TKHDQZ	Delay from K HIGH to Output Hi-Z (Notes 2 & 5)		15		15		20	ns
11	TILDQV	Delay from I LOW to Output (HIGH or LOW) (Note 6)		20		20		20	ns
12	TIHKH	Asynchronous I Recovery Time (Note 6)	15		15		20		ns
13	TILIH	Asynchronous I Pulse Width (Note 6)	15		15		20		ns
14	TISVKH	$\overline{I}_s$ Valid to K HIGH Setup Time (Note 7)	15		20		30		ns
15	TKHISX	$\overline{I}_s$ to K HIGH Hold Time (Note 7)	5		5		5		ns

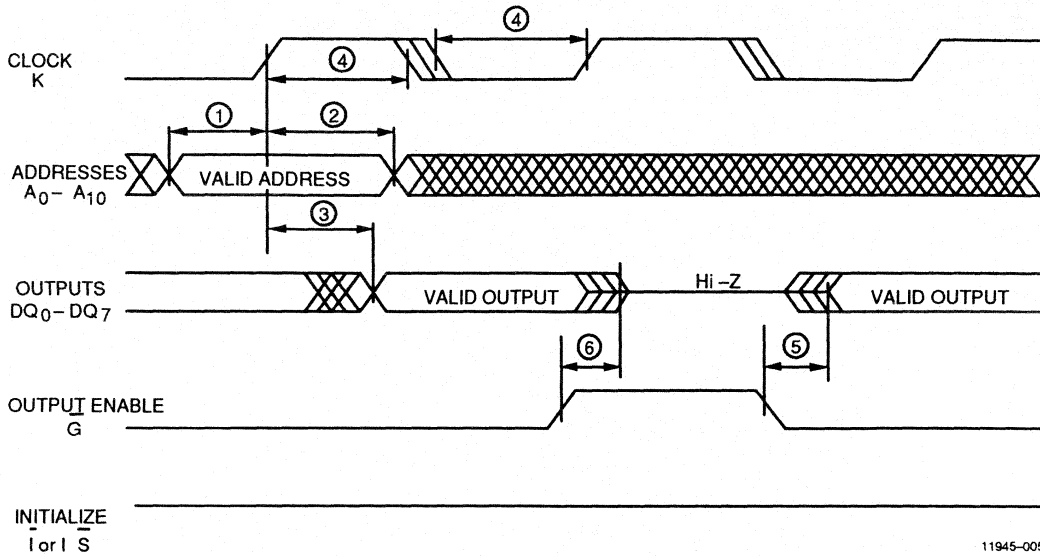
See also SWITCHING WAVEFORMS & SWITCHING TEST LOADS

### Notes:

1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in diagram A.
2. TGHDQZ and TKHDQZ are measured at steady-state HIGH output voltage minus 0.5 V and steady-state LOW output voltage plus 0.5 V output levels using the test load in diagram B.
3. TGLDQV & TKHDQV2 are measured at steady-state output voltage minus 0.5 V for Hi-Z to LOW and steady-state output voltage plus 0.5 V for Hi-Z to HIGH output levels using the test load in diagram A.
4. Applies only when Asynchronous Enable ( $\overline{G}$ ) function is used.
5. Applies only when Synchronous Enable  $\overline{G}_s$  function has been programmed.
6. Applies only when Asynchronous Initialize ( $\overline{I}_s$ ) function is used.
7. Applies only when Synchronous Initialize  $\overline{I}_s$  function has been programmed.



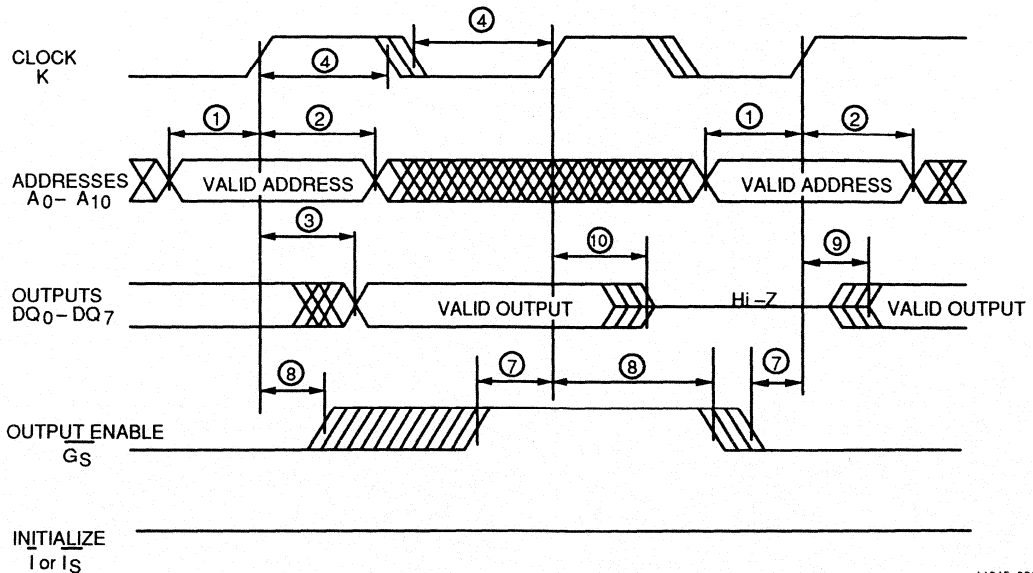
# SWITCHING WAVEFORMS



11945-005A

Timing Set 1. Operation using Asynchronous Enable

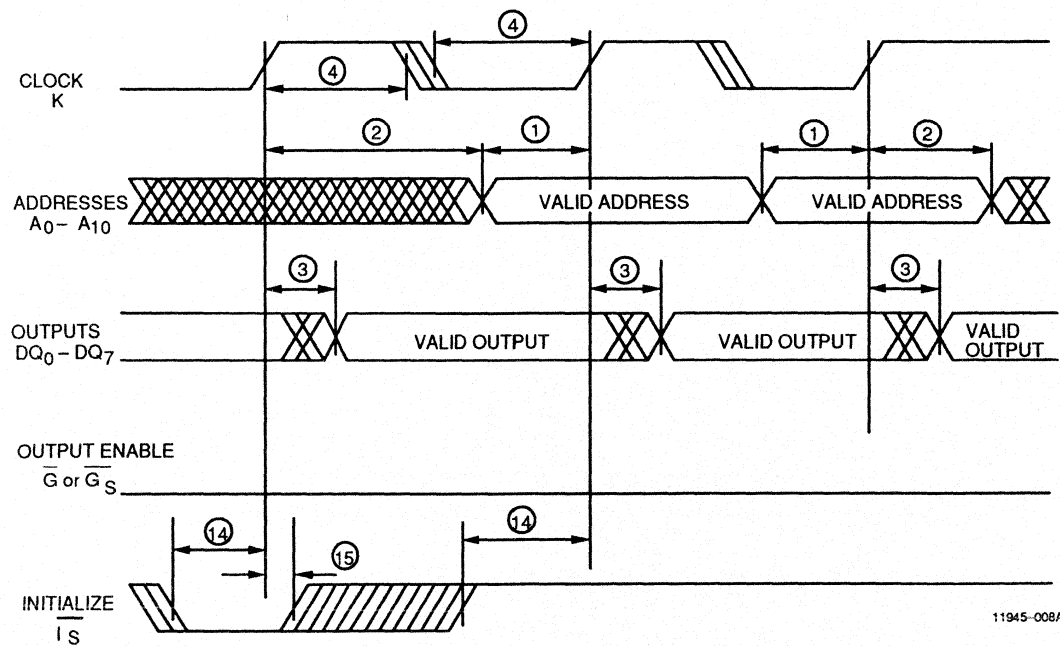
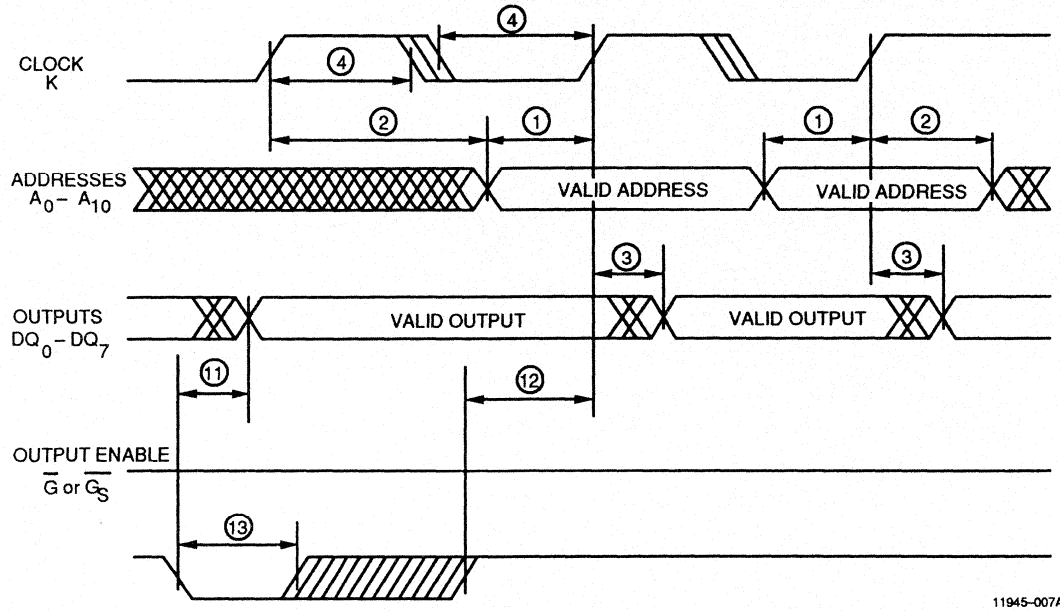
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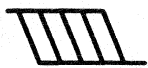


11945-006A

Timing Set 2. Operation using Synchronous Enable

## SWITCHING WAVEFORMS (Continued)

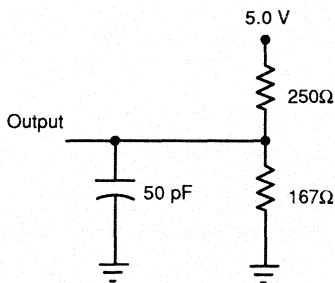


## KEY TO SWITCHING WAVEFORMS

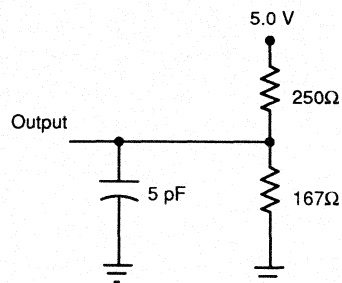
WAVEFORM	INPUTS	OUTPUTS
 	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN

KS000010

## SWITCHING TEST CIRCUITS



A. Output Load for all AC tests except TGHDQZ/TKHDQZ



B. Output Load for TGHDQZ/TKHDQZ

- Notes: 1. All device test loads should be located within 2" of device output pin.  
2. Load capacitance includes all stray and fixture capacitance.

11945-004A

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## PROGRAMMING the Am27C45

The Am27C45 registered PROM is programmed according to the same programming algorithm used for the Am27C49 & Am27C191/291. This algorithm is modified to provide a clock at the beginning of the programming cycle to establish output data states & enable register state. A second clock occurs prior to verification to bring programmed data to the outputs. The  $V_{PP}$  input is the enable ( $\overline{G}/\overline{G}_s$ ) input.

The Am27C45 has an additional 8-bit word which may be programmed to provide any arbitrary microinstruction for system initialization. The unprogrammed state of this word will initialize the data registers with all outputs HIGH.

This part uses the initialize ( $\overline{I}/\overline{I}_s$ ) pin as a select control between the array and the initialize/architecture word during programming.

Initialize ( $\overline{I}/\overline{I}_s$ ) HIGH enables the array for programming and disables the initialize/architecture word. Initialize ( $\overline{I}/\overline{I}_s$ ) LOW enables the initialize/architecture word for programming and disables the array.

An easy implementation for programming the initialize word would be to invert the next higher address input ( $A_n + 1$ ) from the PROM programmer and apply this signal to the initialize ( $\overline{I}/\overline{I}_s$ ) input.

The array and initialize/architecture word could then be programmed over a continuous address field according to Table 1.

The Am27C45 has a multifunctional output enable pin ( $\overline{G}/\overline{G}_s$ ) and initialize pin ( $\overline{I}/\overline{I}_s$ ). When these parts are shipped from the factory these pins function in an Asynchronous mode of operation ( $\overline{G}$ ) and ( $\overline{I}$ ). These pins may be programmed to a Synchronous mode of operation ( $\overline{G}_s$ ) and/or ( $\overline{I}_s$ ) by using the following procedure:

To program the  $\overline{G}/\overline{G}_s$  input for Synchronous Enable operation ( $\overline{G}_s$ ) the  $\overline{I}/\overline{I}_s$  input must be set to a logic LOW, with address input  $A_0$  in a logic HIGH state. The remaining address inputs must be held at a logic LOW. A standard programming cycle is performed with a data bit of "0" applied to output  $Q_0$ .

This is easily implemented on a PROM programmer by inverting the  $A_{11}$  address, applying this signal to the  $\overline{I}/\overline{I}_s$

input, and programming a  $FE_{16}$  data pattern at address  $801_{16}$ .

The initialize input  $\overline{I}/\overline{I}_s$  may be programmed to a Synchronous Initialize ( $\overline{I}_s$ ) operation in precisely the same manner using a data bit of "0" applied to the  $Q_1$  output. Using the programmer implementation described above this would require programming a  $FD_{16}$  data pattern at address  $801_{16}$ .

Unprogrammed cell on  $Q_0$  = Asynchronous Enable ( $\overline{G}$ ) =  $FF_{16}$  Output Data

Programmed cell on  $Q_0$  = Synchronous Enable ( $\overline{G}_s$ ) =  $FE_{16}$  Output Data

Unprogrammed cell on  $Q_1$  = Asynchronous Initialize ( $\overline{I}$ ) =  $FF_{16}$  Output Data

Programmed cell on  $Q_1$  = Synchronous Initialize ( $\overline{I}_s$ ) =  $FD_{16}$  Output Data

This two-bit architecture word will then program the functionality of the respective inputs according to Table 2.

It should be noted that when programming the  $\overline{G}/\overline{G}_s$  and/or  $\overline{I}/\overline{I}_s$  functionality, The operation of these pins is changing from an Asynchronous mode ( $\overline{G}$ ) and/or ( $\overline{I}$ ) input to a Synchronous mode ( $\overline{G}_s$ ) and/or ( $\overline{I}_s$ ) input. This is a functional change rather than a data change to the part. Therefore, verification that the programming event has taken place must be performed in a different manner. The Am27C45 contains on-chip circuitry which when enabled will cause the state the  $\overline{G}/\overline{G}_s$  and  $\overline{I}/\overline{I}_s$  cells to appear as data on  $Q_0$  &  $Q_1$  outputs:

This verification circuitry is enabled by taking the  $A_0$  input to a  $V_{IH}$  (13.0V to 14.0V) level. The  $V_{IH}$  input level should be used for read, programming, and verification cycles for the explicit address used for and data only (address  $801_{16}$  in the above example).

An alternative to using the on-chip verification circuitry would be for the programming equipment to use decision making capability in conjunction with clock, enable and initialize to determine in which functional mode the enable or initialize is operating.

Table 1.

Device	$\overline{I}/\overline{I}_s$ Pin	Array Programming Address Field (Hex)	Initialize Word Address (Hex)	Architecture Word Address (Hex)
Am27C45	$\overline{A}_{11}$	000 thru 7FF	800	801

Table 2.

Architecture Data Word (Hex)	$\overline{I}/\overline{I}_s$ Input	$\overline{G}/\overline{G}_s$ Input
FF	Asynchronous	Asynchronous
FE	Asynchronous	Synchronous
FD	Synchronous	Asynchronous
FC	Synchronous	Synchronous

## Programming Technique

Advanced Micro Devices' Am27C45 high-performance CMOS registered PROM has been designed to use a programming algorithm which minimizes the requirements on the programmer, yet allows the circuit to be programmed quickly and reliably. Specifically, the following sequence of events must take place:

- 1)  $V_{CC}$  power is applied to the device;
- 2) The  $\overline{G}/\overline{G}_s/V_{PP}$  pin is raised to  $V_{IHP}$  and the clock is cycled LOW-HIGH-LOW to disable the outputs;
- 3) The appropriate address is selected;
- 4) The appropriate byte-wide pattern is applied to all outputs;
- 5) The  $\overline{G}/\overline{G}_s/V_{PP}$  pin is pulsed to 13.5 V for 1 ms;
- 6) The  $\overline{G}/\overline{G}_s/V_{PP}$  pin is lowered to  $V_{LP}$  and the clock is cycled LOW-HIGH-LOW to enable the outputs and the byte sensed to verify that correct programming has occurred.
- 7) In the event that the data does not verify, the sequence of 4 through 6 could be repeated up to 25 times;
- 8) At the conclusion of initial programming, the sequence of 4 and 5 should be repeated for over-programming using a  $V_{CC} = 5.0$  V, and  $\overline{G}/\overline{G}_s/V_{PP}$  pulse width equal to twice the sum of initial programming pulse times;
- 9) The sequence of 2 through 6 must be repeated for each address to be programmed;
- 10) At the conclusion of programming, the device should be verified for correct data at all addresses

with two  $V_{CC}$  supply voltages ( $V_{CC} = 6.0$  and  $V_{CC} = 4.2$  V).

## Notes on Programming

- 1) The unprogrammed or erased state of all enabled outputs is HIGH.
- 2) All delays between edges are specified from the completion of the first edge to the beginning of the second edge; i.e., not the midpoints (10 or 90 of specified waveform).
- 3) During  $t_v$ , the output may be switched to appropriate loads for proper verification of specified  $V_{OL}$  and  $V_{OH}$  levels.
- 4) Due to the potential for fast voltage transitions of the outputs, it is advisable to provide low-impedance connections to the device's  $V_{CC}$  and ground pins and to ensure adequate decoupling at the device pins.

## Erasure Characteristics

In order to fully erase all memory locations, it is necessary to expose the memory array to an ultraviolet light source having a wavelength of 2537Å. The minimum recommended dose (UV intensity times exposure time) is 15 Wsec/cm<sup>2</sup>. For a UV lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure time would be approximately 30 minutes. The device should be located within 1 inch of the source in direct line.

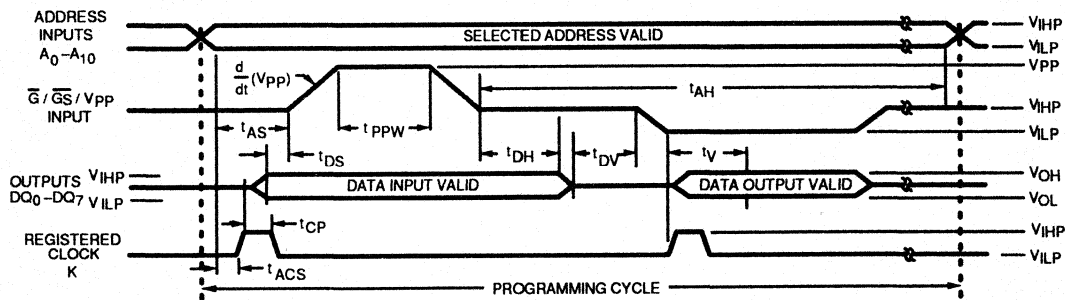
It should be noted that erasure may begin with exposure to light having wavelengths less than 4000Å. To prevent exposure to sunlight or fluorescent lighting from resulting in partial erasure, an opaque label should be affixed over the window after programming.

## PROGRAMMING PARAMETERS

( $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

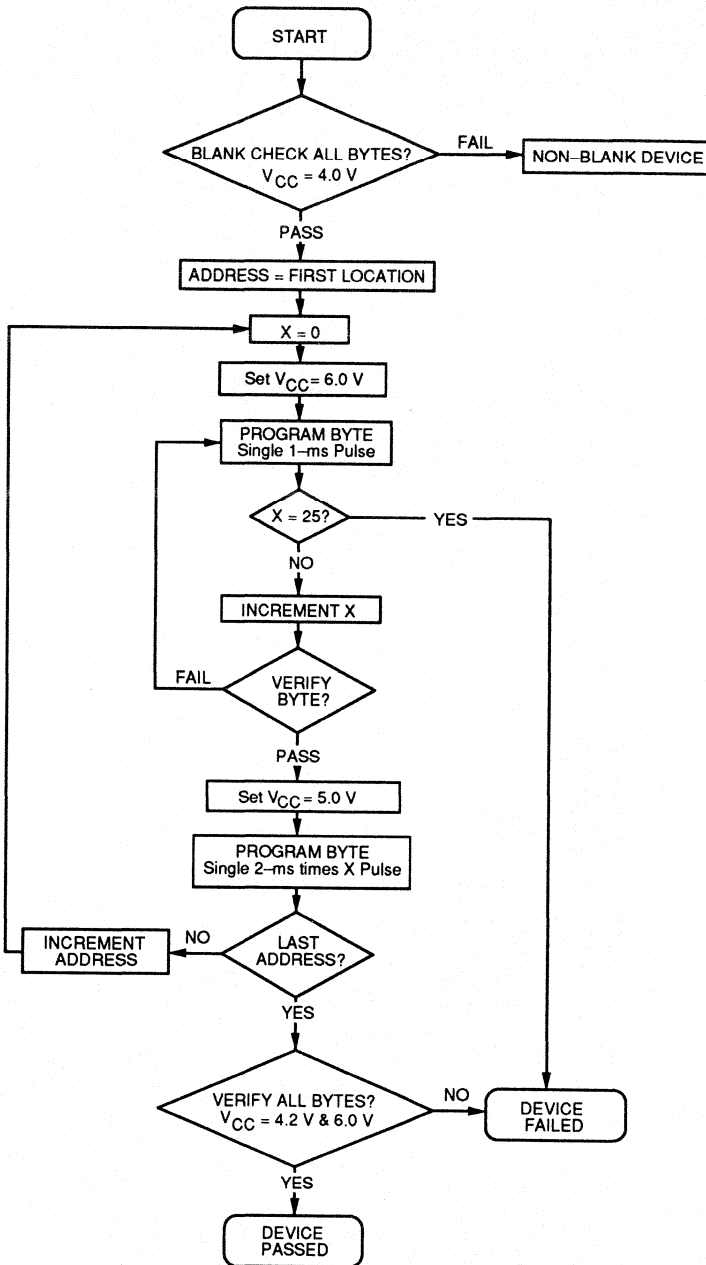
Parameter Symbol	Parameter Description	Min.	Max.	Unit
$V_{CCP}$	Power Supply during Programming	5.75	6.25 4.75	V 5.25
$I_{CCP}$	$V_{CC}$ Supply Current during Programming		90	mA
$V_{PP}$	Programming Voltage	13.0	14.0	V
$I_{PP}$	$V_{PP}$ Supply Current during Programming		30	mA
$V_{IHP}$	Input HIGH Level During Programming and Verify	2.4	5.5	V
$V_{ILP}$	Input LOW Level During Programming and Verify	0	0.45	V
$V_{OL}$	Output LOW Voltage during Verify		0.45	V
$V_{OH}$	Output HIGH Voltage during Verify	2.40		V
$dV_{PP}/dt$	Rate of $\bar{G}/V_{PP}$ Voltage Change (Rise and Fall Times)	5	10	V/ $\mu\text{s}$
$t_{PPW}$	$V_{PP}$ Programming Pulse Width, Initial Programming Pulse	0.95	1.05	ms
$t_{AS}$	Address Valid to $V_{PP}$ (HIGH) Setup Time	1.0		$\mu\text{s}$
$t_{AH}$	$V_{PP}$ (LOW) to Address Change Hold Time	1.0		$\mu\text{s}$
$t_{DS}$	Data Valid to $V_{PP}$ (HIGH) Setup Time	1.0		$\mu\text{s}$
$t_{DH}$	$V_{PP}$ (LOW) to Data Change Hold Time	1.0		$\mu\text{s}$
$t_{DV}$	Delay from Data to Output Enable (LOW) for Verification	1.0		$\mu\text{s}$
$t_{ACS}$	Address Valid to Clock (HIGH) Setup Time	100		$\mu\text{s}$
$t_{CP}$	Clock Pulse Width	50	1000	ns
$t_V$	Delay from Output Enable (LOW) to Verification Strobe	100		ns

## PROGRAMMING WAVEFORMS



11945-009A

# PROGRAMMING FLOW



5

11945-010A

# Am27C49

65,536-Bit (8192x8) High-Performance CMOS PROM

## DISTINCTIVE CHARACTERISTICS

- High-speed (35 ns)/Low-Power (90 mA) CMOS EPROM Technology
- Direct plug-in replacement for Bipolar PROMS — JEDEC-approved pinout
- 5-Volt  $\pm 10\%$  power supplies for both Commercial and Military
- UV-erasable and reprogrammable provides exceptionally high programming yields (Typ. > 99.9%)
- ESD immunity > 2000 V

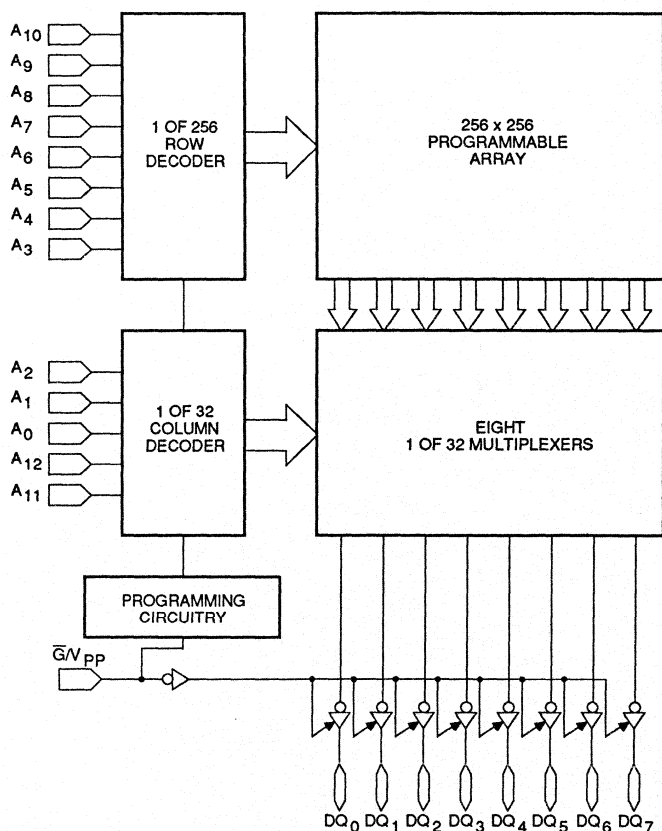
## GENERAL DESCRIPTION

The Am27C49 (8192 words by 8 bits) is a high-speed CMOS programmable read-only memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the

requirements of a variety of microprogrammable controls. This device utilizes proven floating-gate EPROM technology to ensure high reliability, ease of programming, and exceptionally high programming yields.

## BLOCK DIAGRAM



09890A-1



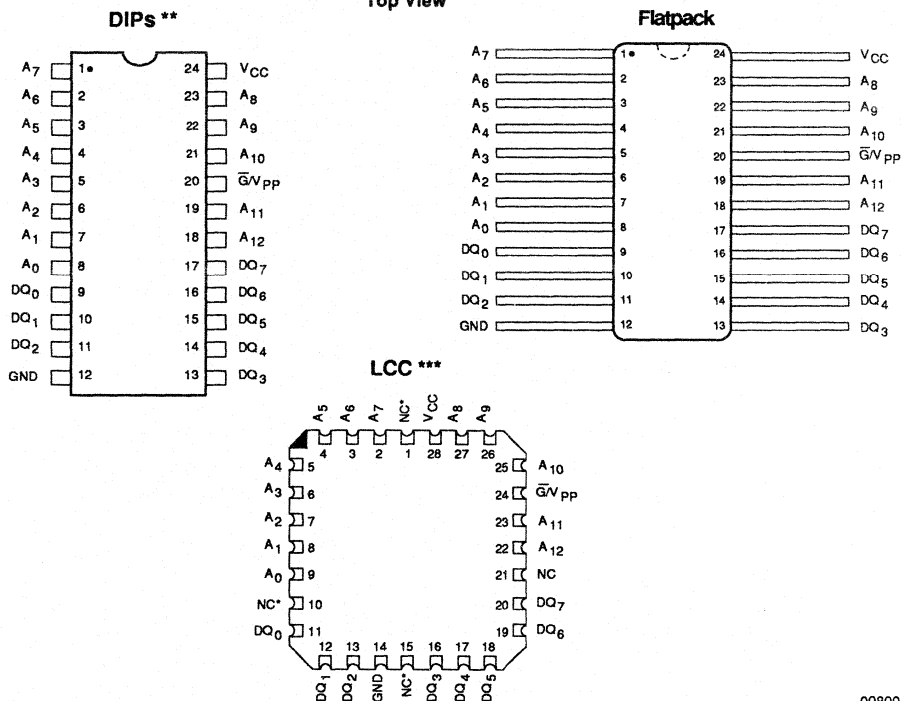
## PRODUCT SELECTOR GUIDE

Part Number	Am27C49-35	Am27C49-45	Am27C49-55
Address Access Time	35 ns	45 ns	55 ns
Operating Range	COM'L	COM'L/MIL*	COM'L/MIL*

\* Advance Information—Military Products Only.

### CONNECTION DIAGRAMS

Top View



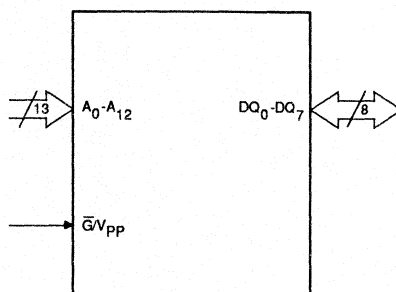
\*NC = No Connection

Note: Pin 1 is marked for orientation.

\*\* Also available in a 24-Pin ceramic windowed DIP. Pinout identical to DIPs.

\*\*\* Also available in a 28-Pin ceramic windowed LCC. Pinout identical to LCC.

### LOGIC SYMBOL



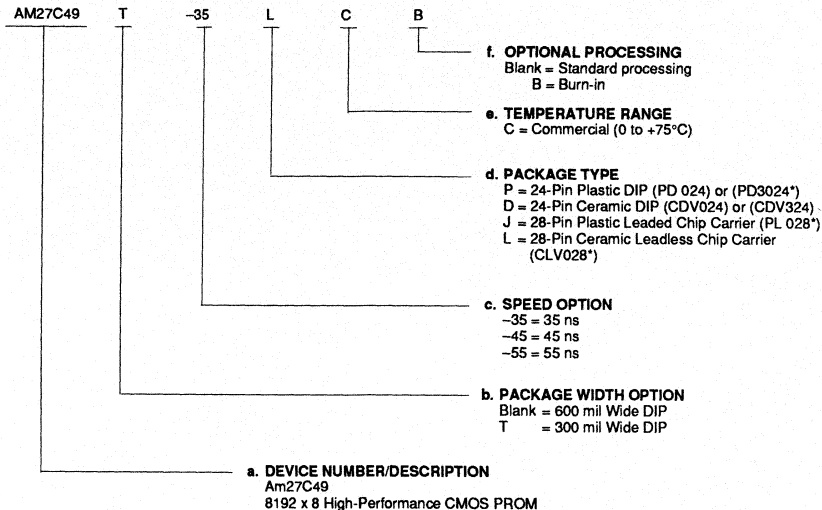
09890A-3

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Package Width Option
- c. Speed Option
- d. Package Type
- e. Temperature Range
- f. Optional Processing



\* Product version in Development, contact HPP Product Marketing.

Valid Combinations	
AM27C49-35	PC, PCB, DC,
AM27C49-45	DCB, LC, LCB
AM27C49-55	JC, JCB
AM27C49T-35	
AM27C49T-45	PC, PCB, DC,
AM27C49T-55	DCB

#### Valid Combinations

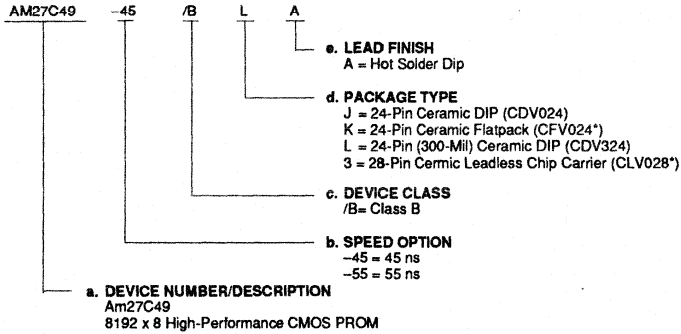
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM27C49-45	/BJA, /BLA,
AM27C49-55	/BKA, /B3A

\*Preliminary; Package in Development.

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.



### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

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## PIN DESCRIPTION

### **A<sub>0</sub>-A<sub>12</sub> Address Lines (Inputs)**

The 13-bit field presented at the address inputs selects one of 8192 memory locations to be read from.

### **DQ<sub>0</sub>-DQ<sub>7</sub> Data Port (Input/Outputs; Three State)**

The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which, when disabled, are in a floating or high-impedance state. These pins provide the data input for programming the memory array.

### **$\bar{G}/V_{pp}$ Output Enable/Programming Power**

Provides direct control of the DQ output three-state buffers. When raised to a voltage > 12.0 V, this pin provides the programming power to program the memory array.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs in High-Impedance State .....	-0.5 V to +7.0 V
DC Programming Voltage ( $V_{pp}$ ) .....	14 V
DC Input Voltage .....	-0.5 V to +7.0 V
Electrostatic Discharge Protection (per MIL-STD-883 Method 3015.2) .....	> 2000 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature ( $T_A$ ) .....	0 to +75°C
Supply Voltage ( $V_{cc}$ ) .....	+4.5 V to +5.5 V
Military (M) Devices*	
Case Temperature ( $T_c$ ) .....	-55 to +125°C
Supply Voltage ( $V_{cc}$ ) .....	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\* Military Product 100% tested at  $T_c = +25^\circ\text{C}$ ,  $+125^\circ\text{C}$ , and  $-55^\circ\text{C}$ .

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{IH}$	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 1)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 1)		0.8	V
$V_{OH}$	Output HIGH Voltage	$V_{cc} = \text{Min.}$ , $I_{OH} = -4.0 \text{ mA}$ $V_{IN} = V_{IH}$ or $V_{IL}$	2.4		V
$V_{OL}$	Output LOW Voltage	$V_{cc} = \text{Min.}$ , $I_{OL} = 16 \text{ mA}$ $V_{IN} = V_{IH}$ or $V_{IL}$		0.4	V
$V_{CL}$	Input Clamp Diode Voltage	$V_{cc} = \text{Min.}$ , $I_{IN} = -18 \text{ mA}$	-1.2		V
$I_{IH}$	Input HIGH Current	$V_{cc} = \text{Max.}$ , $V_{IN} = 5.5 \text{ V}$		10	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{cc} = \text{Max.}$ , $V_{IN} = 0.0 \text{ V}$		-10	$\mu\text{A}$
$I_{sc}$	Output Short-Circuit Current	$V_{cc} = \text{Max.}$ $V_{OUT} = 0.0 \text{ V}$ (Note 2)	-20	-90	mA
$I_{CEX}$	Output Leakage Current	$V_{cc} = \text{Max.}$ , $V_G = 2.4 \text{ V}$	$V_{OUT} = 5.5 \text{ V}$	40	$\mu\text{A}$
			$V_{OUT} = 0.4 \text{ V}$	-40	$\mu\text{A}$
$I_{cc}$	Operating Supply Current	$V_{cc} = \text{Max.}$ (Note 3)	All Inputs = $V_{IH}$	90	mA
			All Inputs = $V_{IL}$		

- Notes:
- $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
  - Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
  - Operating  $I_{cc}$  is measured with all inputs except  $\bar{G}$  switching between  $V_{IL}$  and  $V_{IH}$  at a timing interval equal to TAVDQV. The outputs are disabled via  $\bar{G}$  held at 3.0 V.

5

Capacitance*				
Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
$C_{IN}$	Input Capacitance ( $\overline{G}/V_{pp}$ )	$V_{CC} = 5.0 \text{ V}, T_A = 25^\circ\text{C}$	15	pF
	Input Capacitance (All Others)		5	
$C_{OUT}$	Output Capacitance	$V_{IN}/V_{OUT} = 2.0 \text{ V} @ f = 1 \text{ MHz}$	8	pF

\*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

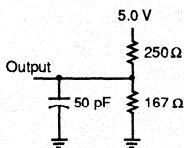
No.	Parameter Symbol	Parameter Description	Am27C49						Unit
			-35		-45		-55		
			COM'L Only		COM'L/MIL		COM'L/MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVDQV	Address Valid to Output Valid Access Time		35		45		55	ns
2	TGHDQZ	Delay from Output Enable HIGH to Output High Impedance		20		25		30	ns
3	TGLDQV	Delay from Output Enable LOW to Output Valid		20		25		30	ns

See Switching Test Circuits.

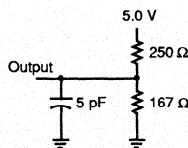
- Notes:
1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in diagram A.
  2. TGHDQZ is measured at steady-state HIGH output voltage  $-0.5 \text{ V}$  and steady-state LOW output voltage  $+0.5 \text{ V}$  output levels using the test load in diagram B.

\* Subgroups 7 and 8 apply to functional tests.

### SWITCHING TEST CIRCUITS



A. Output Load for all AC tests except TGVDQZ







B. Output Load for TGVDQZ

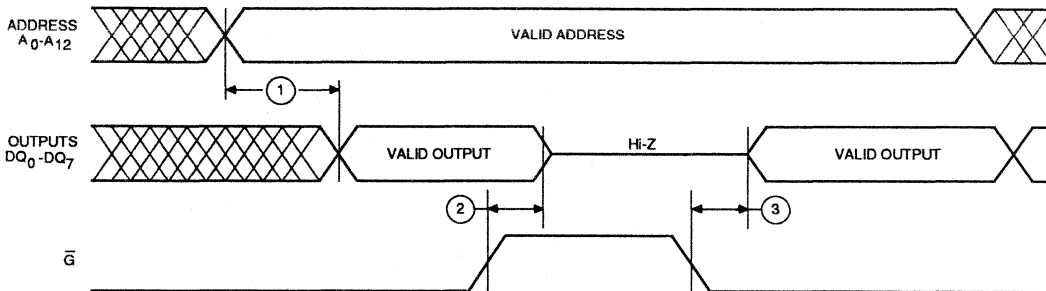
- Notes:
1. All device test loads should be located within 2" of device output pin.
  2. Load capacitance includes all stray and fixture capacitance.

09890A-4

## SWITCHING WAVEFORMS KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN

KS000010



09890A-5

## Am27C49 CMOS PROM PROGRAMMING PROCEDURE

### Programming Technique

Advanced Micro Devices' high-performance CMOS PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer, yet allows the circuit to be programmed quickly and reliably. Specifically, the following sequence of events must take place:

- 1)  $V_{cc}$  power is applied to the device;
- 2) The device outputs are disabled;
- 3) The appropriate address is selected;
- 4) The appropriate byte-wide pattern is applied to all outputs;
- 5) The  $\overline{G}/V_{pp}$  pin is pulsed to 13.5 V for 1 ms;
- 6) The device is enabled and the byte sensed to verify that correct programming has occurred.
- 7) In the event that the data does not verify, the sequence of 4 through 6 could be repeated up to 25 times;
- 8) At the conclusion of initial programming, the sequence of 4 and 5 should be repeated for overprogramming using a  $V_{cc} = 5.0$  V, and  $\overline{G}/V_{pp}$  pulse width equal to twice the sum of initial programming pulse times;
- 9) The sequence of 2 through 6 must be repeated for each address to be programmed;
- 10) At the conclusion of programming, the device should be verified for correct data at all addresses with two  $V_{cc}$  supply voltages ( $V_{cc} = 6.0$  and  $V_{cc} = 4.2$  V).

## Notes on Programming

- 1) The unprogrammed or erased state of all enabled outputs is HIGH.
- 2) All delays between edges are specified from the completion of the first edge to the beginning of the second edge; i.e., not the midpoints (10% or 90% of specified waveform).
- 3) During  $t_v$ , the output may be switched to appropriate loads for proper verification of specified  $V_{OL}$  and  $V_{OH}$  levels.
- 4) Due to the potential for fast voltage transitions of the outputs, it is advisable to provide low-impedance connections to the device's  $V_{CC}$  and ground pins and to ensure adequate decoupling at the device pins.

## Erase Characteristics

In order to fully erase all memory locations, it is necessary to expose the memory array to an ultraviolet light source having a wavelength of 2537 Angstroms. The minimum recommended dose (UV intensity times exposure time) is 15 Wsec/cm<sup>2</sup>. For a UV lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure time would be approximately 30 minutes. The device should be located within 1 inch of the source in direct line.

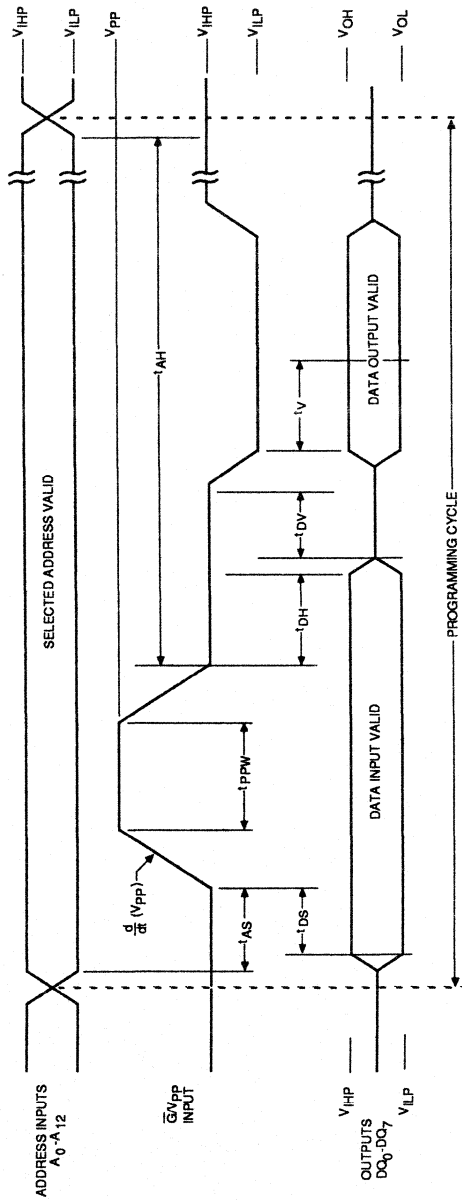
It should be noted that erasure may begin with exposure to light having wavelengths less than 4000 Angstroms. To prevent exposure to sunlight or fluorescent lighting from resulting in partial erasure, an opaque label should be affixed over the window after programming.

## PROGRAMMING PARAMETERS ( $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

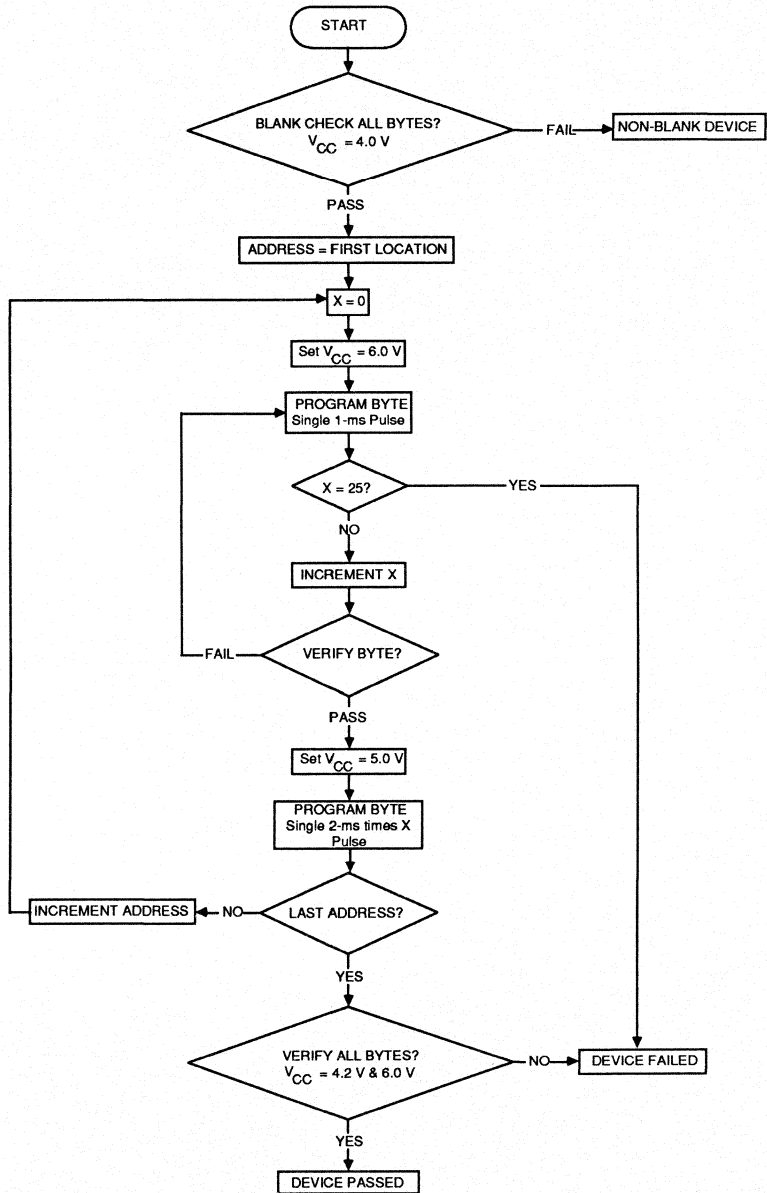
Parameter Symbol	Parameter Description		Min.	Max.	Unit	
$V_{CCP}$	Power Supply during Programming		Initial Programming	5.75	6.25	V
			Over-Programming	4.75	5.25	
$I_{CCP}$	$V_{CC}$ Supply Current during Programming			90	mA	
$V_{PP}$	Programming Voltage		13	14	V	
$I_{PP}$	$V_{PP}$ Supply Current during Programming			30	mA	
$V_{IHP}$	Input HIGH Level during Programming and Verify		2.4	5.5	V	
$V_{ILP}$	Input LOW Level during Programming and Verify		0	0.45	V	
$V_{OL}$	Output LOW Voltage during Verify			0.45	V	
$V_{OH}$	Output HIGH Voltage during Verify		2.40		V	
$dV_{PP}/dt$	Rate of $\bar{G}/V_{PP}$ Voltage Change (Rise and Fall Times)		5	10	V/ $\mu$ s	
$t_{PPW}$	$V_{PP}$ Programming Pulse Width	Initial Programming Pulse	0.95	1.05	ms	
$t_{AS}$	Address Valid to $V_{PP}$ (HIGH) Setup Time		1.0		$\mu$ s	
$t_{AH}$	$V_{PP}$ (LOW) to Address Change Hold Time		1.0		$\mu$ s	
$t_{DS}$	Data Valid to $V_{PP}$ (HIGH) Setup Time		1.0		$\mu$ s	
$t_{DH}$	$V_{PP}$ (LOW) to Data Change Hold Time		1.0		$\mu$ s	
$t_{DV}$	Delay from Data to Output Enable (LOW) for Verification		1.0		$\mu$ s	
$t_v$	Delay from Output Enable (LOW) to Verification Strobe		100		ns	



### PROGRAMMING WAVEFORMS



09890A-6



09890-002B

Figure 1. Programming Flow



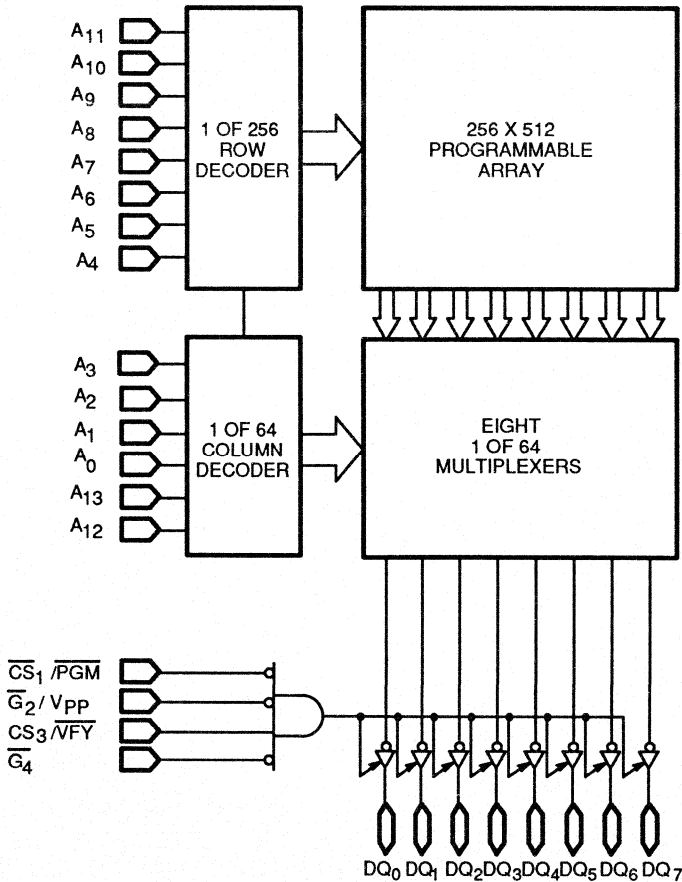
# Am27C51

## 131,072-Bit (16384 x 8) High-Performance CMOS PROM

### DISTINCTIVE CHARACTERISTICS

- High-speed (45 ns)/Low-Power (90 mA) CMOS EPROM Technology
- Direct plug-in replacement for Bipolar PROMs — JEDEC-approved pinout
- 5-Volt  $\pm 10\%$  power supplies for both Commercial and Military
- UV-erasable and reprogrammable provides exceptionally high programming yields (Typ. > 99.9%)
- ESD immunity > 2000 V

### BLOCK DIAGRAM



5

11344-001A

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## GENERAL DESCRIPTION

The Am27C51 (16,384 words by 8 bits) is a high-performance CMOS programmable read-only memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable con-

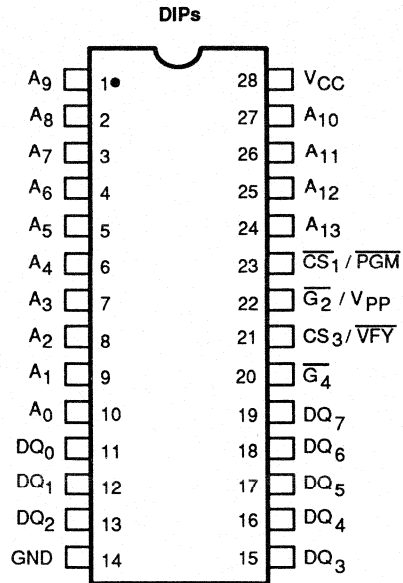
trols. Word-depth expansion is facilitated by both active LOW ( $\overline{CS}_1$ ,  $\overline{G}$ , and  $\overline{G}_2$ ) and active HIGH ( $CS_3$ ) output enables. This device utilizes proven floating-gate EPROM technology to ensure high reliability, ease of programming, and exceptionally high programming yields.

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## PRODUCT SELECTOR GUIDE

Part Number	Am27C51-45	Am27C51-55	Am27C51-65
Address Access Time	45 ns	55 ns	65ns
Operating Range	COM'L	COM'L/MIL	COM'L/MIL

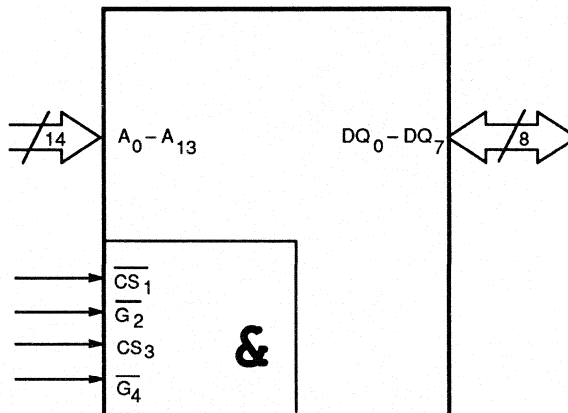
## CONNECTION DIAGRAM



11344-002A

Note: The ceramic DIP (CDV028) is offered in a window package.

## LOGIC SYMBOL



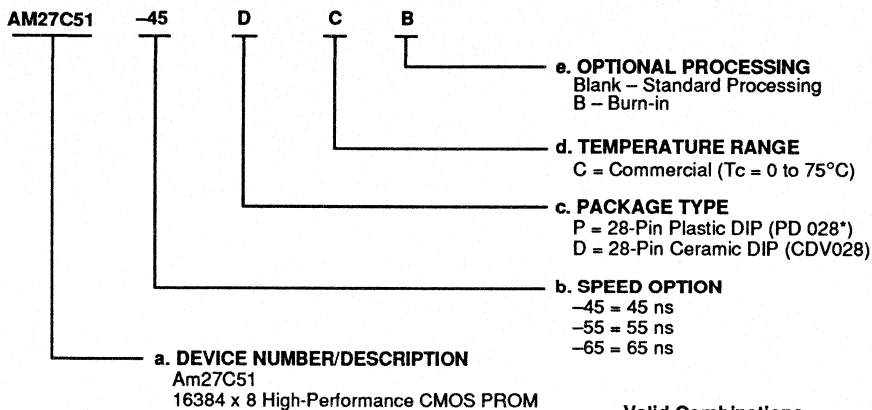
11344-003A

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM27C51-45	PC, PCB, DC, DCB
AM27C51-55	
AM27C51-65	

\* Preliminary; Package in Development

#### MILITARY BURN-IN

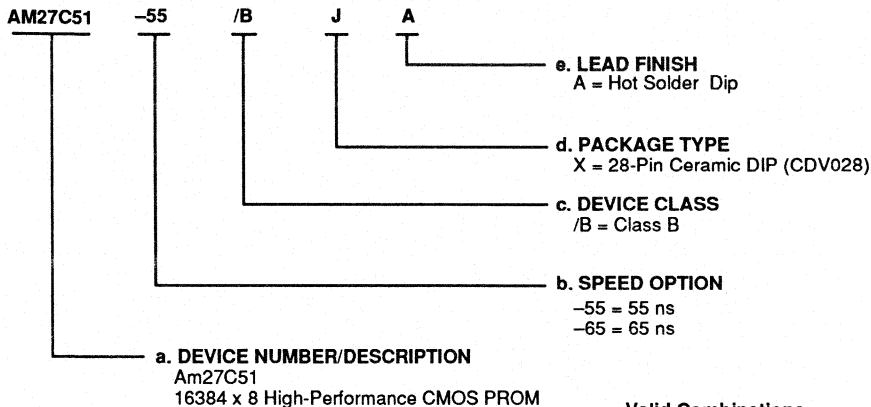
Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (If applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM27C51-55	/BXA
AM27C51-65	

#### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

#### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

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## PIN DESCRIPTION

**A<sub>0</sub> – A<sub>13</sub>**

### Address Lines (Inputs)

The 14-bit field presented at the address inputs selects one of 16384 memory locations to be read from.

**DQ<sub>0</sub> – DQ<sub>7</sub>**

### Data Port (Input/Outputs; Three State)

The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which, when disabled, are in a floating or high-impedance state. These pins provide the data input for programming the memory array.

**$\overline{CS}_1 \bullet \overline{G}_2 \bullet CS_3 \bullet \overline{G}_4$**

### Output Enables/(V<sub>PP</sub>) Programming Power

Provides direct control of the DQ output three-state buffers. When raised to a voltage > 12.0 V, the  $\overline{G}_2 / V_{PP}$  pin provides the programming power to program the memory array.

$$\text{Enable} = \overline{CS}_1 \bullet \overline{G}_2 \bullet CS_3 \bullet \overline{G}_4$$

$$\text{Disable} = \overline{\overline{CS}_1 \bullet \overline{G}_2 \bullet CS_3 \bullet \overline{G}_4}$$

$$= CS_1 + G_2 + \overline{CS}_3 + G_4$$



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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient Temperature with Power Applied	-55 to +125°C
Supply Voltage	-0.5 V to +7.0 V
DC Voltage Applied to Outputs in High-Impedance State	-0.5 V to +7.0 V
DC Programming Voltage ( $V_{PP}$ )	14 V
DC Input Voltage	-0.5 V to +7.0 V
Electrostatic Discharge Protection (per MIL-STD-883 Method 3015.2)	> 2000 V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature ( $T_A$ )	0 to +75°C
Supply Voltage ( $V_{CC}$ )	+4.5 to +5.5 V
Military (M) Devices*	
Case Temperature ( $T_C$ )	-55 to +125°C
Supply Voltage ( $V_{CC}$ )	+4.5 to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

*\* Military Products 100% tested at  $T_C = +25^\circ\text{C}$ ,  $+125^\circ\text{C}$ , and  $-55^\circ\text{C}$ .*

**DC CHARACTERISTICS over operating ranges unless otherwise specified**

(for APL Products, Group A Subgroups 1, 2, 3, are tested unless otherwise noted)

Parameter Symbol	Parameter Descriptions	Test Conditions	Min.	Max.	Unit
$V_{IH}$	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 1)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 1)		0.8	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ , $I_{OH} = -4.0 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ , $I_{OL} = 16 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$		0.4	V
$V_{CL}$	Input Clamp Diode Voltage	$V_{CC} = \text{Min.}$ , $I_{CL} = -18 \text{ mA}$	-1.2		V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$ , $V_{IN} = 5.5 \text{ V}$		10	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{CC} = \text{Max.}$ , $V_{IN} = 0.0 \text{ V}$		-10	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{CC} = \text{Max.}$ , $V_{OUT} = 0.0 \text{ V}$ (Note 2)	-20	-90	mA
$I_{CEX}$	Output Leakage Current	$V_{CC} = \text{Max.}$ , $V_{OUT} = 5.5 \text{ V}$ , $V_{CS} = 2.4 \text{ V}$ , $V_{OUT} = 0.4 \text{ V}$		40	$\mu\text{A}$
$I_{CC}$	Operating Supply Current	$V_{CC} = \text{Max.}$ , All Inputs = $V_{IH}$ (Note 3.) All Inputs = $V_{IL}$		90	mA

**Notes:**

- 1)  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and /or tester noise. Do Not attempt to test these values without suitable equipment.
- 2) Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
- 3) Operating  $I_{CC}$  is measured with all inputs except  $\overline{CS}_1$  switching between  $V_{IL}$  and  $V_{IH}$  at a timing interval equal to  $T_{AVDQV}$ . The outputs are disabled via  $\overline{CS}_1$  held at 3.0 V.

## CAPACITANCE\*

Parameter Symbol	Parameter Descriptions	Test Conditions	Typ.	Unit
C <sub>IN</sub>	Input Capacitance ( $\overline{G}_2 / V_{PP}$ & $\overline{CS}_1$ )	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C	9	pF
	Input Capacitance (All Others)		6	
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> / V <sub>OUT</sub> = 2.0 V @ f = 1MHz	8	pF

\*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified**  
 (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted \*).

Parameter Number & Symbol	Description	Am27C51 -45 COM'L Only Max	Am27C51 -55 COM'L /MIL .Max.	Am27C51 -65 COM'L/MIL Max.	Unit
1 TAVDQV	Address Valid to Output Valid Access Time	45	55	65	ns
2 TCSVDQZ TGHDQZ	Delay from Output Enables Valid to Output High Impedance	25	30	35	ns
3 TCSVDQV TGLDQV	Delay from Output Enable Valid to Output Valid	25	30	35	ns

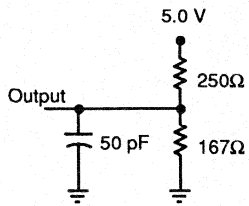
**Notes:**

See Switching Test Circuits.

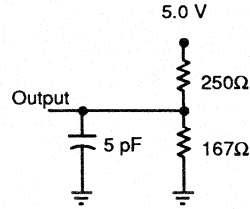
- 1) Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in diagram A.
- 2) TCSVDQZ/TGHDQZ is measured at steady-state HIGH output voltage minus 0.5 V and steady-state LOW output voltage plus 0.5 V output levels using the test load in diagram B.
- 3) TCSVDQV/TGLDQV is measured at steady-state output voltage minus 0.5 V for Hi-Z to LOW and steady-state output voltage plus 0.5 V for Hi-Z to HIGH output levels using the test load in diagram A.

\*Subgroups 7 and 8 apply to functional tests.

## SWITCHING TEST CIRCUITS



A. Output Load for all AC tests except TCSVDQZ/TGHDQZ



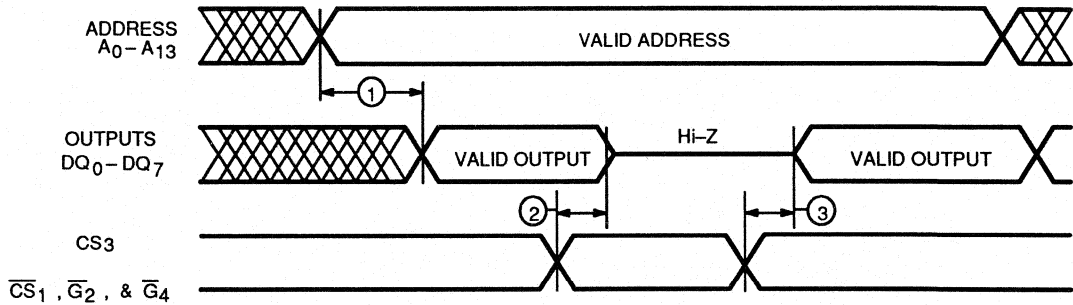
B. Output Load for TCSVDQZ/TGHDQZ

**Notes:**

1. All device test loads should be located within 2" of device output pin.
2. Load capacitance includes all stray and fixture capacitance.

11344-004A

## SWITCHING WAVEFORMS



11344-005A

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## Am27C51 CMOS PROM PROGRAMMING PROCEDURE

### Programming Technique

Advanced Micro Devices' high-performance CMOS PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer, yet allows the circuit to be programmed quickly and reliably. Specifically, the following sequence of events must take place:

- 1)  $V_{CC}$  power is applied to the device;
- 2) The  $\overline{CS}_1 / \overline{PGM}$ ,  $\overline{G}_2 / V_{PP}$ , and  $CS_3 / \overline{VFY}$  inputs are raised to  $V_{IHP}$ ;
- 3) The  $\overline{G}_2 / V_{PP}$  pin is raised to  $V_{PP}$  (13.5V.);
- 4) The appropriate address is selected;
- 5) The appropriate byte-wide pattern is applied to all outputs;
- 6) The  $\overline{CS}_1 / \overline{PGM}$  pin is pulsed to  $V_{ILP}$  for 1 ms;
- 7) The  $CS_3 / \overline{VFY}$  pin is pulsed to  $V_{ILP}$  and the byte sensed to verify that correct programming has occurred.
- 8) In the event that the data does not verify, the sequence of 5 through 7 could be repeated up to 25 times;
- 9) At the conclusion of initial programming, the sequence of 5 and 6 should be repeated for over-programming using a  $V_{CC} = 5.0$  V, and  $\overline{CS}_1 / \overline{PGM}$  pulse width equal to twice the sum of initial programming pulse times;
- 10) The sequence of 4 through 9 must be repeated for each address to be programmed;
- 11) At the conclusion of programming, the device should be verified for correct data at all addresses with two  $V_{CC}$  supply voltages ( $V_{CC} = 6.0$  and  $V_{CC} = 4.2$  V).
- 12) The  $\overline{G}_2 / V_{PP}$  pin is lowered back to  $V_{IHP}$ ;

### Notes on Programming

- 1) The unprogrammed or erased state of all enabled outputs is HIGH.
- 2) All delays between edges are specified from the completion of the first edge to the beginning of the second edge; i.e., not the midpoints (10% or 90% of specified waveform).
- 3) Delays between any two timing events unless otherwise specified should be a minimum of 1 $\mu$ s.
- 4) While  $V_{PP}$  voltage is present  $\overline{PGM}$  and  $\overline{VFY}$  inputs should **never** be LOW at the same time.
- 5) During  $t_V$ , the output may be switched to appropriate loads for proper verification of specified  $V_{OL}$  and  $V_{OH}$  levels.
- 6) Due to the potential for fast voltage transitions of the outputs, it is advisable to provide low-impedance connections to the device's  $V_{CC}$  and ground pins and to ensure adequate decoupling at the device pins.
- 7)  $\overline{G}_4$  should be held at  $V_{ILP}$  throughout programming and verification.

### Erase Characteristics

In order to fully erase all memory locations, it is necessary to expose the memory array to an ultraviolet light source having a wavelength of 2537 Å. The minimum recommended dose (UV intensity times exposure time) is 15 Wsec/cm<sup>2</sup>. For a UV lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure time would be approximately 30 minutes. The device should be located within 1 inch of the source in direct line.

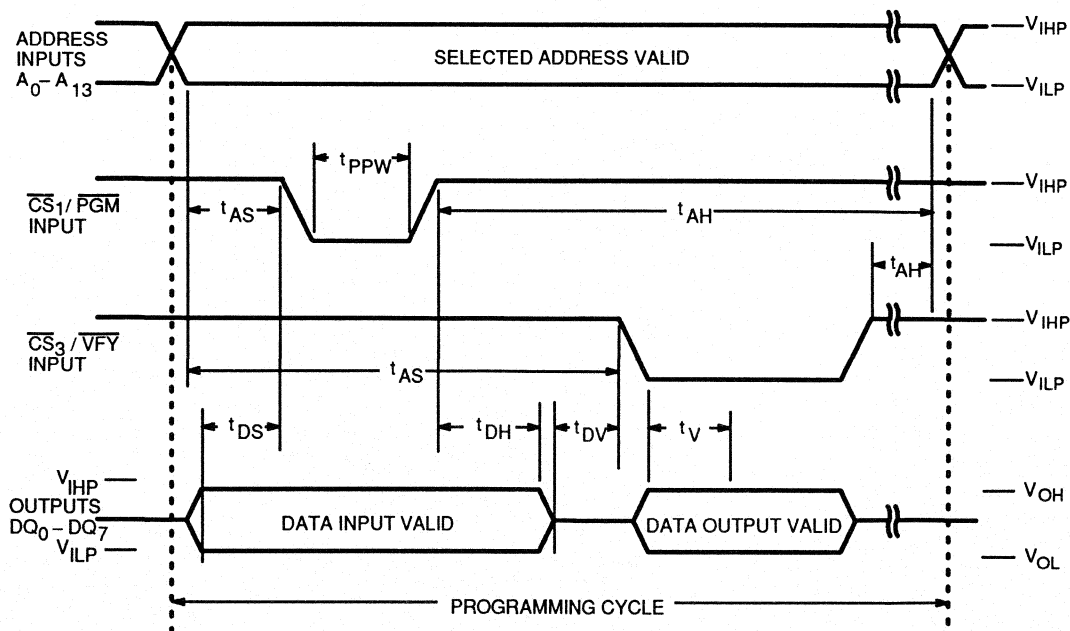
It should be noted that erasure may begin with exposure to light having wavelengths less than 4000 Å. To prevent exposure to sunlight or fluorescent lighting from resulting in partial erasure, an opaque label should be affixed over the window after programming.

## PROGRAMMING PARAMETERS

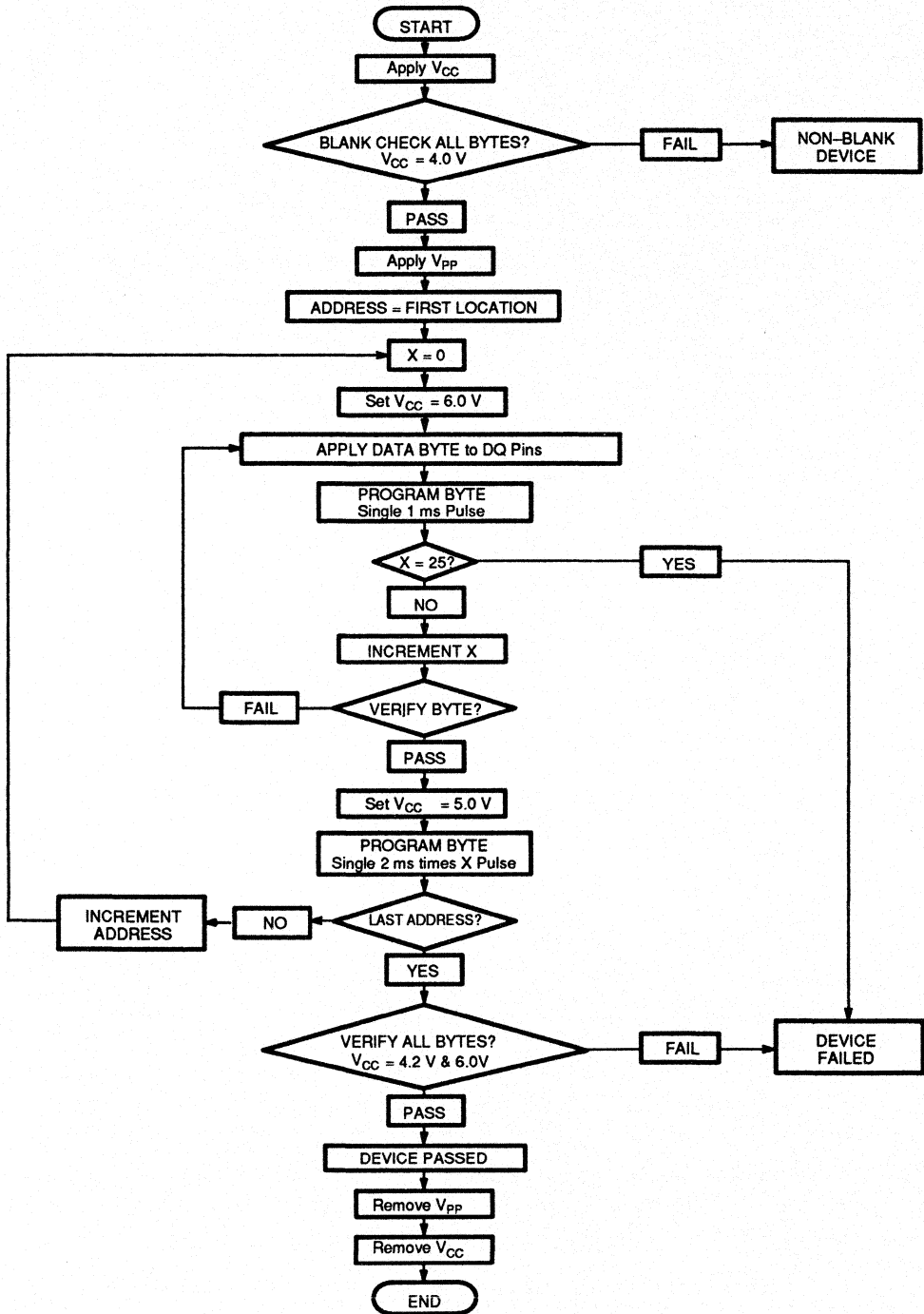
( $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

Parameter Symbol	Description	Min.	Max.	Unit
$V_{CCP}$	Power Supply during Programming Initial Programming	5.75	6.25	V
	Over-Programming	4.75	5.25	V
$I_{CCP}$	$V_{CC}$ Supply Current during Programming		90	mA
$V_{PP}$	Programming Voltage	13	14	V
$I_{PP}$	$V_{PP}$ Supply Current during Programming		30	mA
$V_{IHP}$	Input HIGH Level During Programming and Verify	3.0	5.5	V
$V_{ILP}$	Input LOW Level During Programming and Verify	0.0	0.4	V
$V_{OL}$	Output LOW Voltage during Verify		0.4	V
$V_{OH}$	Output HIGH Voltage during Verify	2.4		V
$dV_{PP}/dt$	Rate of $\overline{CS}_2 / V_{PP}$ Voltage Change (Rise and Fall Times)	5	10	V/ $\mu\text{s}$
$t_{PPW}$	$\overline{CS}_1 / \overline{PGM}$ Programming Pulse Width Initial Programming Pulse	0.95	1.05	ms
$t_{AS}$	Address Valid to $\overline{CS}_1 / \overline{PGM}$ or $CS_3 / \overline{VFY}$ (LOW) Setup Time	1.0		$\mu\text{s}$
$t_{AH}$	$\overline{CS}_1 / \overline{PGM}$ or $CS_3 / \overline{VFY}$ (HIGH) to Address Change Hold Time	1.0		$\mu\text{s}$
$t_{DS}$	Data Valid to $\overline{CS}_1 / \overline{PGM}$ (LOW) Setup Time	1.0		$\mu\text{s}$
$t_{DH}$	$\overline{CS}_1 / \overline{PGM}$ (HIGH) to Data Change Hold Time	1.0		$\mu\text{s}$
$t_{DV}$	Delay from Data to $CS_3 / \overline{VFY}$ (LOW) for Verification	1.0		$\mu\text{s}$
$t_V$	Delay from $CS_3 / \overline{VFY}$ (LOW) to Verification Strobe	100		ns

## PROGRAMMING WAVEFORMS



11344-006A



11344-007A

Figure 1. Programming Flow



# Am27C191/Am27C291

16,384-Bit (2048x8) High-Performance CMOS PROM



## DISTINCTIVE CHARACTERISTICS

- High-speed (25 ns)/Low-Power (60 mA) CMOS EPROM Technology
- Direct plug-in replacement for Bipolar PROMs — JEDEC-approved pinout
- Slim 300-mil DIP (Am27C291) or standard 600-mil DIP (Am27C191) packaging available
- 5-Volt  $\pm 10\%$  power supplies for both Commercial and Military
- UV-erasable and reprogrammable provides exceptionally high programming yields (Typ. > 99.9%)
- ESD immunity > 2000 V

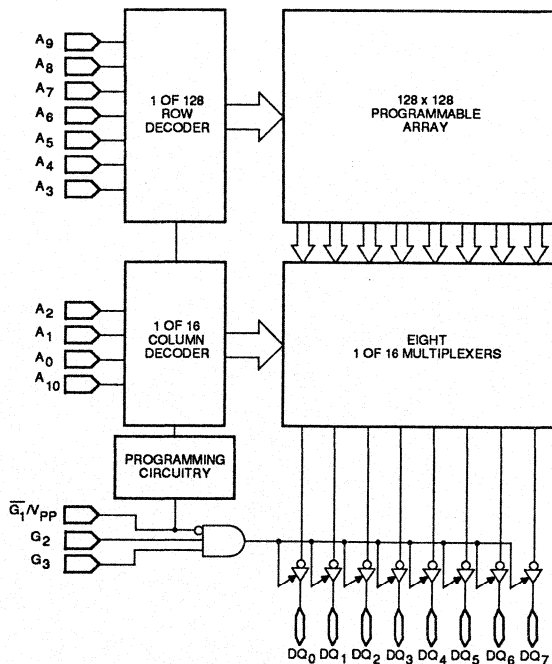
## GENERAL DESCRIPTION

The Am27C191 (2048 words by 8 bits) is a high-performance CMOS programmable read-only memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replace-

ment. Word-depth expansion is facilitated by both active LOW ( $\bar{G}_1$ ) and active HIGH ( $G_2$  and  $G_3$ ) output enables. This device utilizes proven floating-gate EPROM technology to ensure high reliability, ease of programming, and exceptionally high programming yields. This device is also available in 300-mil lateral center DIP (Am27C291).

## BLOCK DIAGRAM



10176A-1

5

Publication #	Rev.	Amendment
10176	B	/0
Issue Date: January 1989		

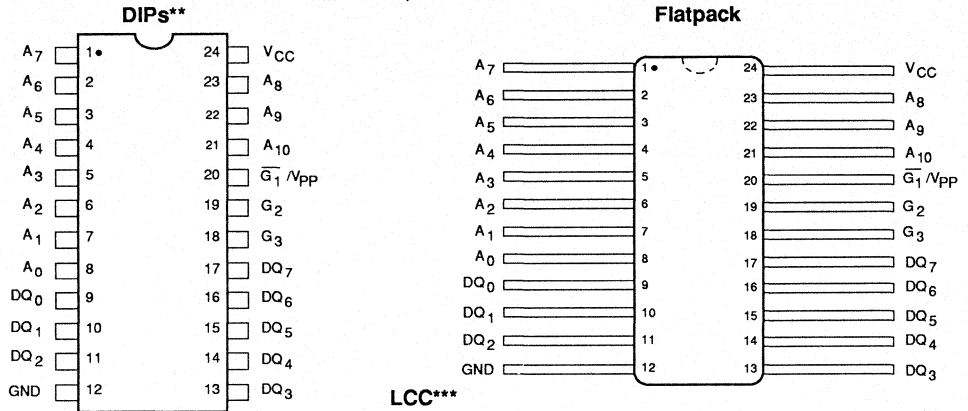
## PRODUCT SELECTOR GUIDE

Part Number	Am27C191-25 Am27C291-25	Am27C191-35 Am27C291-35	Am27C191-45 Am27C291-45
<b>Address Access Time</b>	25 ns	35 ns	45 ns
<b>Operating Range</b>	COM'L	COM'L/MIL*	COM'L/MIL*

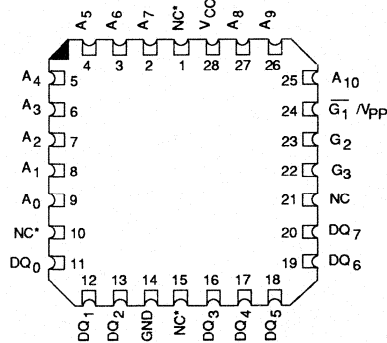
\* Advance Information—Military Products Only.

## CONNECTION DIAGRAMS

Top View



**LCC\*\*\***



\*NC = No Connection

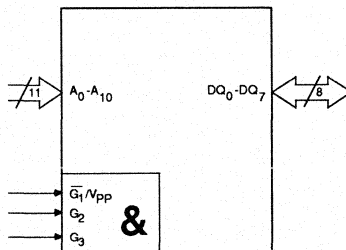
Note: Pin 1 is marked for orientation

\*\* Also available in a 24-Pin ceramic windowed DIP. Pinout identical to DIPs.

\*\*\* Also available in a 28-Pin ceramic windowed LCC. Pinout identical to LCC.

10176A-2

## LOGIC SYMBOL



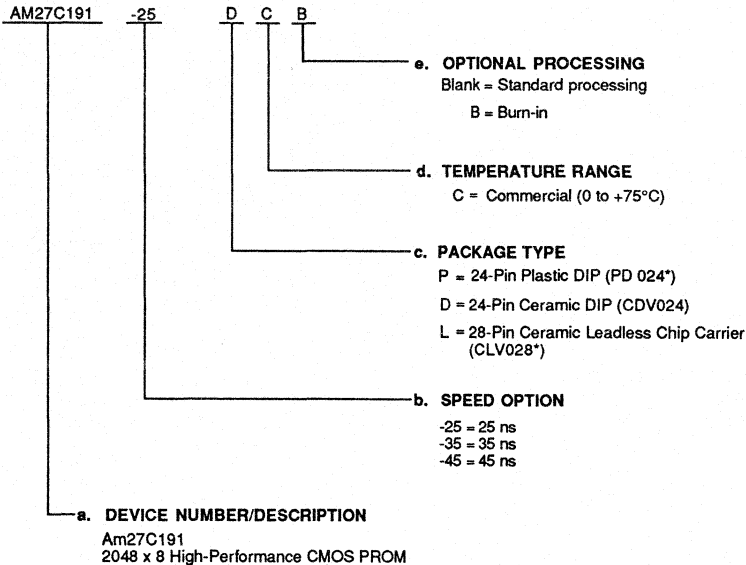
10176A-3

## ORDERING INFORMATION

### Am27C191 Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27C191-25	PC, PCB, DC, DCB, LC, LCB
AM27C191-35	
AM27C191-45	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

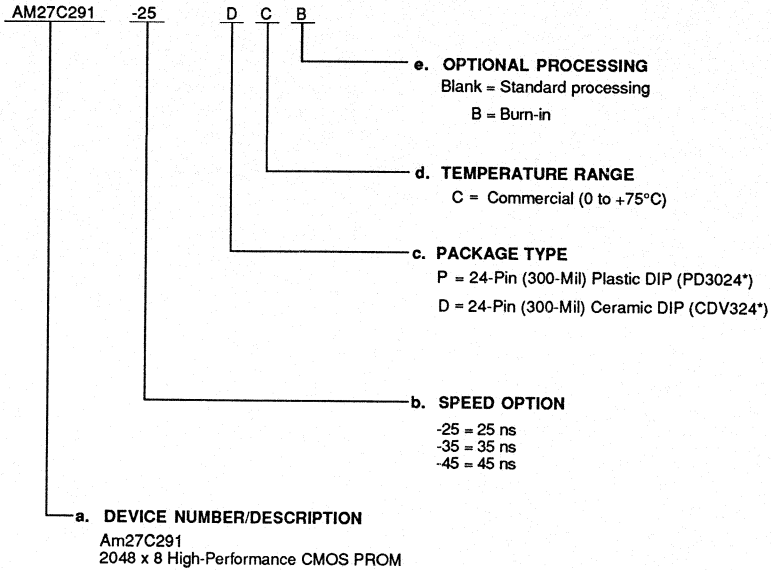
\* Product version in Development, contact HPP Product Marketing.

## ORDERING INFORMATION (Cont'd.)

### Am27C291 Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27C291-25	PC, PCB, DC, DCB
AM27C291-35	
AM27C291-45	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

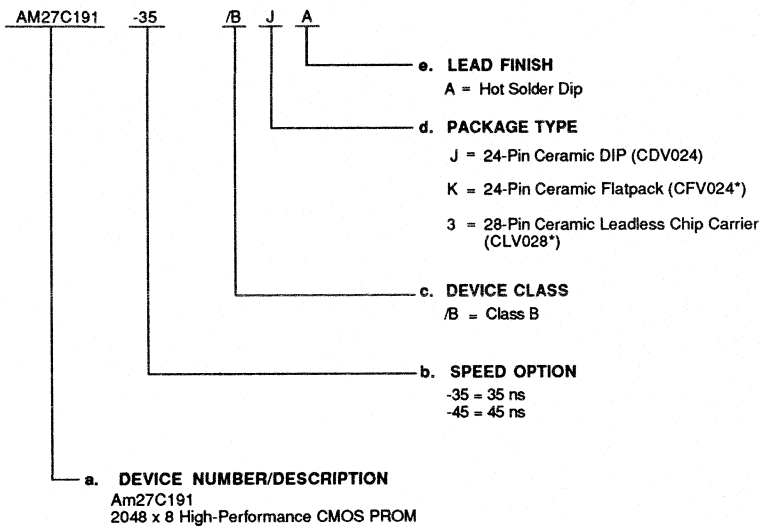
\*Product version in Development, contact HPP Product Marketing.

## MILITARY ORDERING INFORMATION

### Am27C191 APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27C191-35	/BJA, /BKA, /B3A
AM27C191-45	

\*Preliminary; Package in Development.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

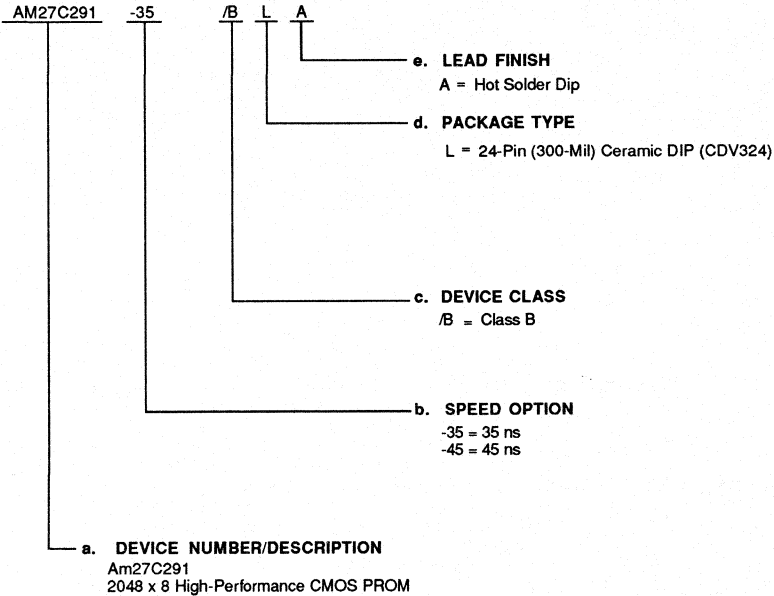
Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

**MILITARY ORDERING INFORMATION (Cont'd.)**

**Am27C291 APL Products**

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27C291-35	/BLA
AM27C291-45	

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

**Group A Tests**

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

**MILITARY BURN-IN**

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

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## PIN DESCRIPTION

### $A_0$ – $A_{10}$ Address Lines (Inputs)

The 11-bit field presented at the address inputs selects one of 2048 memory locations to be read from.

### $DQ_0$ – $DQ_7$ Data Port (Input/Outputs; Three State)

The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which, when disabled, are in a floating or high-impedance state. These pins provide the data input for programming the memory array.

### $\overline{G}_1/V_{pp}$ , $G_2$ , $G_3$ Output Enable/ $(V_{pp})$ Programming Power

Provides direct control of the DQ output three-state buffers. When raised to a voltage > 12.0 V, the  $\overline{G}_1/V_{pp}$  pin provides the programming power to program the memory array.

$$\text{Enable} = \overline{G}_1 \cdot G_2 \cdot G_3$$

$$\begin{aligned} \text{Disable} &= \overline{G}_1 \cdot \overline{G}_2 \cdot \overline{G}_3 \\ &= G_1 + \overline{G}_2 + \overline{G}_3 \end{aligned}$$

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs in High-Impedance State .....	-0.5 V to +7.0 V
DC Programming Voltage ( $V_{PP}$ ) .....	14 V
DC Input Voltage .....	-0.5 V to +7.0 V
Electrostatic Discharge Protection (per MIL-STD-883 Method 3015.2) .....	> 2000 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature ( $T_A$ ) .....	0 to +75°C
Supply Voltage ( $V_{CC}$ ) .....	+4.5 V to +5.5 V
Military (M) Devices*	
Case Temperature ( $T_C$ ) .....	-55 to +125°C
Supply Voltage ( $V_{CC}$ ) .....	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\* Military product 100% tested at  $T_C = +25^\circ\text{C}$ ,  $+125^\circ\text{C}$ , and  $-55^\circ\text{C}$ .

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{IH}$	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 1)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 1)		0.8	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ , $I_{OH} = -4.0 \text{ mA}$ $V_{IN} = V_{IH}$ or $V_{IL}$	2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ , $I_{OL} = 16 \text{ mA}$ $V_{IN} = V_{IH}$ or $V_{IL}$		0.4	V
$V_{CL}$	Input Clamp Diode Voltage	$V_{CC} = \text{Min.}$ , $I_{IN} = -18 \text{ mA}$	-1.2		V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$ , $V_{IN} = 5.5 \text{ V}$		10	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{CC} = \text{Max.}$ , $V_{IN} = 0.0 \text{ V}$		-10	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{CC} = \text{Max.}$ $V_{OUT} = 0.0 \text{ V}$ (Note 2)	-20	-90	mA
$I_{CEX}$	Output Leakage Current	$V_{CC} = \text{Max.}$ , $V_{G1} = 2.4 \text{ V}$	$V_{OUT} = 5.5 \text{ V}$	40	$\mu\text{A}$
			$V_{OUT} = 0.4 \text{ V}$	-40	$\mu\text{A}$
$I_{CC}$	Operating Supply Current	$V_{CC} = \text{Max.}$ (Note 3)	All Inputs = $V_{IH}$	60	mA
			All Inputs = $V_{IL}$		

- Notes:
- $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
  - Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
  - Operating  $I_{CC}$  is measured with all inputs except  $\bar{G}_1$  switching between  $V_{IL}$  and  $V_{IH}$  at a timing interval equal to TAVDQV. The outputs are disabled via  $\bar{G}_1$  held at 3.0 V.



## Capacitance\*

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C <sub>IN</sub>	Input Capacitance ( $\bar{G}_1/V_{PP}$ )	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C V <sub>IN</sub> /V <sub>OUT</sub> = 2.0 V @ f = 1 MHz	9	pF
	Input Capacitance (All Others)		5	
C <sub>OUT</sub>	Output Capacitance		8	pF

\*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

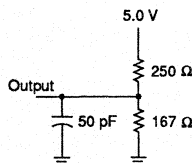
No.	Parameter Symbol	Parameter Description	Am27C191/Am27C291						Unit
			-25		-35		-45		
			COM'L Only		COM'L/MIL		COM'L/MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVDQV	Address Valid to Output Valid Access Time		25		35		45	ns
2	TGVDQZ	Delay from Output Enable Valid to Output High Impedance (Note 2)		20		20		25	ns
3	TGVDQV	Delay from Output Enable Valid to Output Valid (Note 3)		20		20		25	ns

See Switching Test Circuits.

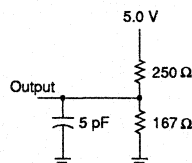
- Notes:
1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in diagram A.
  2. TGVDQZ is measured at steady-state HIGH output voltage -0.5 V and steady-state LOW output voltage +0.5 V output levels using the test load in diagram B.
  3. TGVDQV is measured at steady-state output voltage minus 0.5 V for Hi-Z to LOW and steady-state output voltage plus 0.5 V for Hi-Z to HIGH output levels using the test load in diagram A.

\* Subgroups 7 and 8 apply to functional tests.

## SWITCHING TEST CIRCUITS



A. Output Load for all AC tests except TGVDQZ



B. Output Load for TGVDQZ

10176A-4B

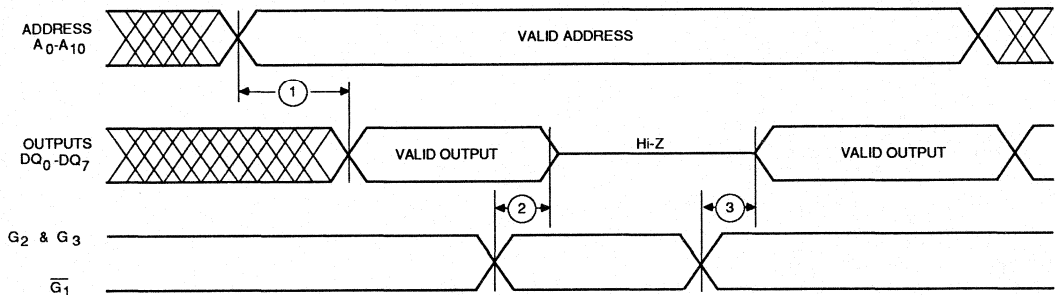
- Notes:
1. All device test loads should be located within 2" of device output pin.
  2. Load capacitance includes all stray and fixture capacitance.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN

KS000010



10176A-5

## Am27C191/Am27C291 CMOS PROM PROGRAMMING PROCEDURE

### Programming Technique

Advanced Micro Devices' high-performance CMOS PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer, yet allows the circuit to be programmed quickly and reliably. Specifically, the following sequence of events must take place:

- 1)  $V_{cc}$  power is applied to the device;
- 2) The device outputs are disabled;

- 3) The appropriate address is selected;
- 4) The appropriate byte-wide pattern is applied to all outputs;
- 5) The  $\overline{G}_1/V_{pp}$  pin is pulsed to 13.5 V for 1 ms;
- 6) The device is enabled and the byte sensed to verify that correct programming has occurred.
- 7) In the event that the data does not verify, the sequence of 4 through 6 could be repeated up to 25 times;
- 8) At the conclusion of initial programming, the sequence of 4 and 5 should be repeated for over-programming using a  $V_{cc} = 5.0$  V, and  $\overline{G}_1/V_{pp}$  pulse width equal to twice the sum of initial programming pulse times;
- 9) The sequence of 2 through 6 must be repeated for each address to be programmed;
- 10) At the conclusion of programming, the device should be verified for correct data at all addresses with two  $V_{cc}$  supply voltages ( $V_{cc} = 6.0$  and  $V_{cc} = 4.2$  V).

## Notes on Programming

- 1) The unprogrammed or erased state of all enabled outputs is HIGH.
- 2) All delays between edges are specified from the completion of the first edge to the beginning of the second edge; i.e., not the midpoints (10% or 90% of specified waveform).
- 3) During  $t_v$ , the output may be switched to appropriate loads for proper verification of specified  $V_{OL}$  and  $V_{OH}$  levels.
- 4) Due to the potential for fast voltage transitions of the outputs, it is advisable to provide low-impedance connections to the device's  $V_{CC}$  and ground pins and to ensure adequate decoupling at the device pins.

## Erasure Characteristics

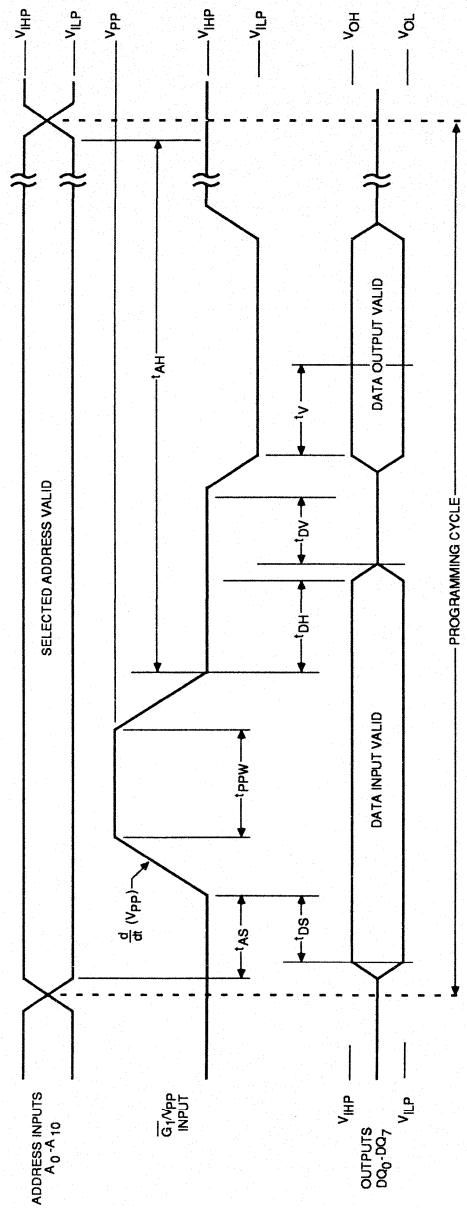
In order to fully erase all memory locations, it is necessary to expose the memory array to an ultraviolet light source having a wavelength of 2537Å. The minimum recommended dose (UV intensity times exposure time) is 15 Wsec/cm<sup>2</sup>. For a UV lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure time would be approximately 30 minutes. The device should be located within 1 inch of the source in direct line.

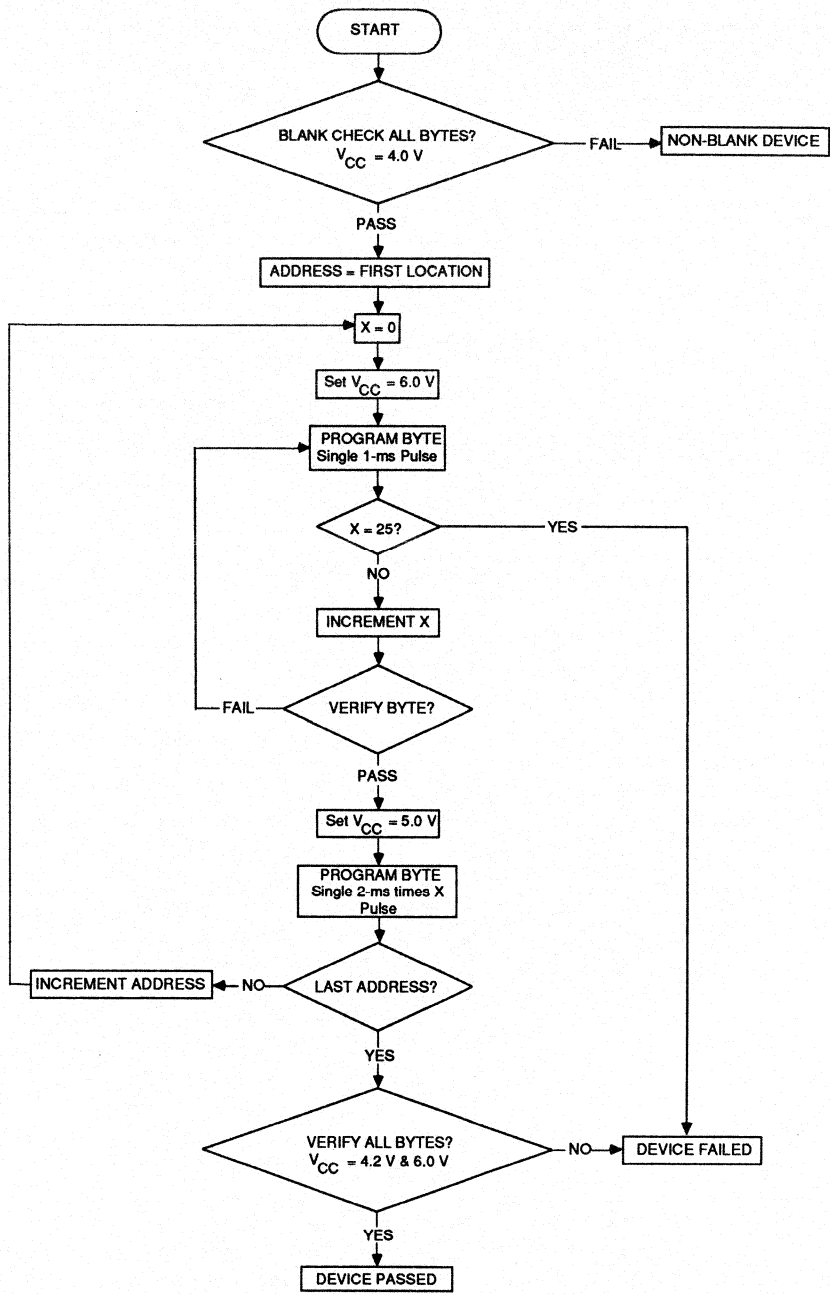
It should be noted that erasure may begin with exposure to light having wavelengths less than 4000Å. To prevent exposure to sunlight or fluorescent lighting from resulting in partial erasure, an opaque label should be affixed over the window after programming.

## PROGRAMMING PARAMETERS ( $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

Parameter Symbol	Parameter Description		Min.	Max.	Unit
$V_{CCP}$	Power Supply during Programming	Initial Programming	5.75	6.25	V
		Over-Programming	4.75	5.25	
$I_{CCP}$	$V_{CC}$ Supply Current during Programming			90	mA
$V_{PP}$	Programming Voltage		13.0	14.0	V
$I_{PP}$	$V_{PP}$ Supply Current during Programming			30	mA
$V_{IHP}$	Input HIGH Level during Programming and Verify		2.4	5.5	V
$V_{ILP}$	Input LOW Level during Programming and Verify		0	0.45	V
$V_{OL}$	Output LOW Voltage during Verify			0.45	V
$V_{OH}$	Output HIGH Voltage during Verify		2.40		V
$dV_{PP}/dt$	Rate of $\overline{Q}_1/V_{PP}$ Voltage Change (Rise and Fall Times)		5	10	V/ $\mu\text{s}$
$t_{PPW}$	$V_{PP}$ Programming Pulse Width	Initial Programming Pulse	0.95	1.05	ms
$t_{AS}$	Address Valid to $V_{PP}$ (HIGH) Setup Time		1.0		$\mu\text{s}$
$t_{AH}$	$V_{PP}$ (LOW) to Address Change Hold Time		1.0		$\mu\text{s}$
$t_{DS}$	Data Valid to $V_{PP}$ (HIGH) Setup Time		1.0		$\mu\text{s}$
$t_{DH}$	$V_{PP}$ (LOW) to Data Change Hold Time		1.0		$\mu\text{s}$
$t_{DV}$	Delay from Data to Output Enable (LOW) for Verification		1.0		$\mu\text{s}$
$t_v$	Delay from Output Enable (LOW) to Verification Strobe		100		ns

## PROGRAMMING WAVEFORMS





5

10176-7A

Figure 1. Programming Flow

# Am27S13/27S13A

## 2,048-Bit (512x4) Bipolar PROM



### DISTINCTIVE CHARACTERISTICS

- High speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

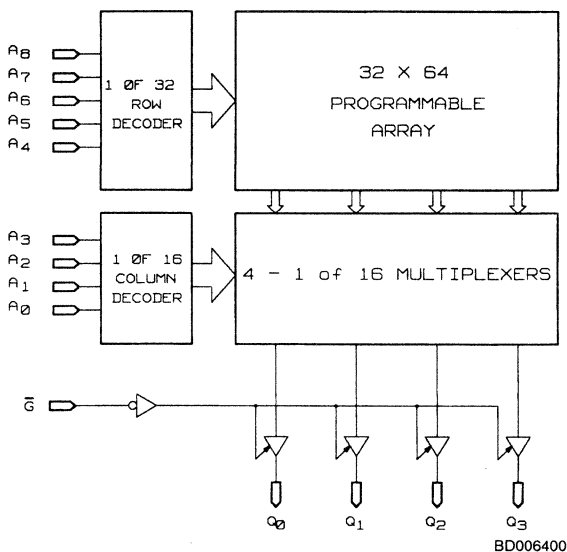
### GENERAL DESCRIPTION

The Am27S13 (512 words by 4 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state (Am27S13) outputs which are compatible with low-power Schottky bus standards capable

of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by an active LOW output enable ( $\bar{G}$ ).

### BLOCK DIAGRAM

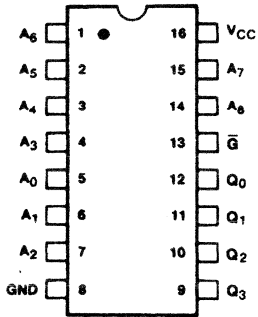


### PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S13A		Am27S13	
	30 ns	40 ns	50 ns	60 ns
Address Access Time				
Operating Range	C	M	C	M

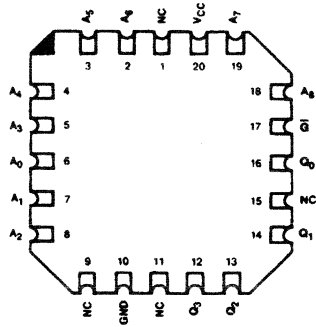
**CONNECTION DIAGRAMS**  
Top View

DIPs\*



CD000591

LCC\*\*



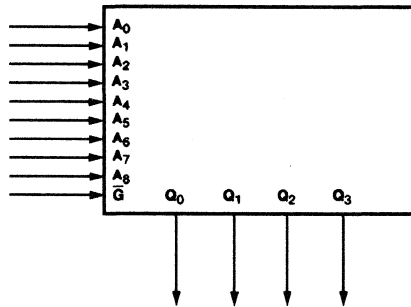
CD000601

\*Also available in 16-Pin Flatpacks; Pinout identical to DIPs.

\*\*Also available in 20-Pin PLCC; Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

**LOGIC SYMBOL**



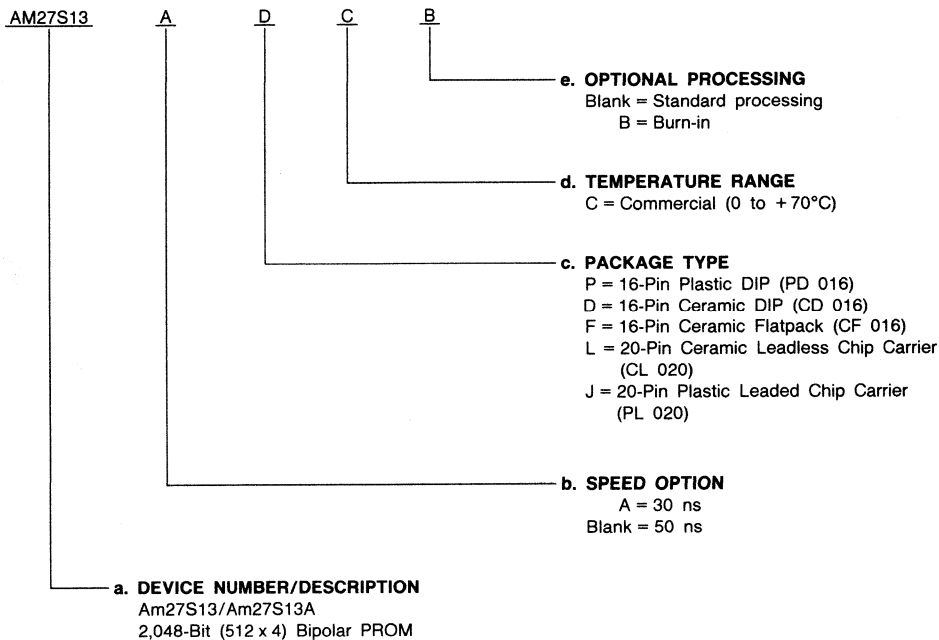
LS000091

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number**
- b. Speed Option** (if applicable)
- c. Package Type**
- d. Temperature Range**
- e. Optional Processing**



#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM27S13	DC, DCB, PC, PCB, LC, LCB, FC, FCB,
AM27S13A	JC, JCB

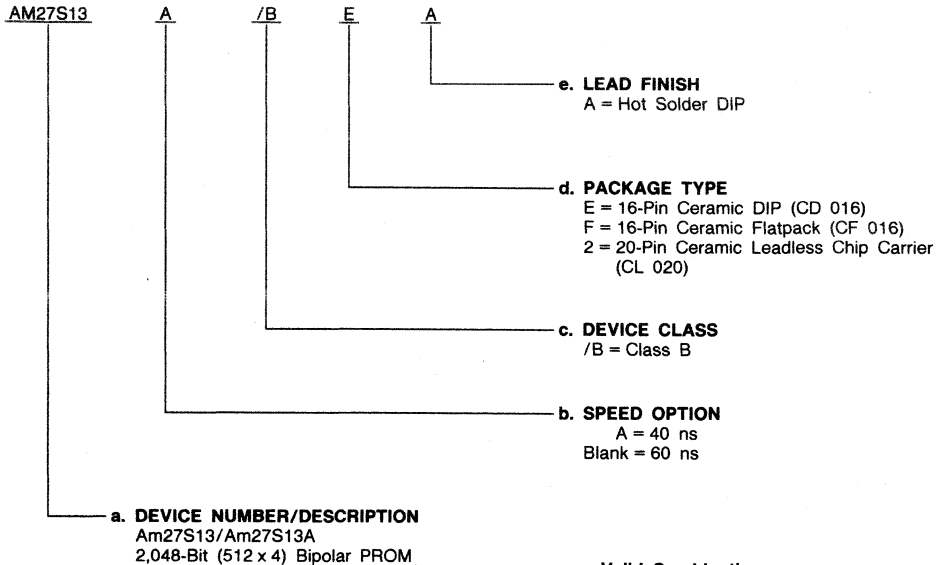


## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S13	/BEA, /BFA, /B2A
AM27S13A	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

## MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>8</sub> Address Inputs

The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

### Q<sub>0</sub> - Q<sub>3</sub> Data Output Port

The outputs whose state represents the data read from the selected memory locations.

### $\bar{G}$ Output Enable

Provides direct control of the Q output three-state buffers. Outputs disabled force all open-collector outputs to an OFF

state and all three-state outputs to a floating or high-impedance state.

Enable =  $\bar{G}$

Disable = G

### V<sub>CC</sub> Device Power Supply Pin

The most positive of the logic power supply pins.

### GND Device Power Supply Pin

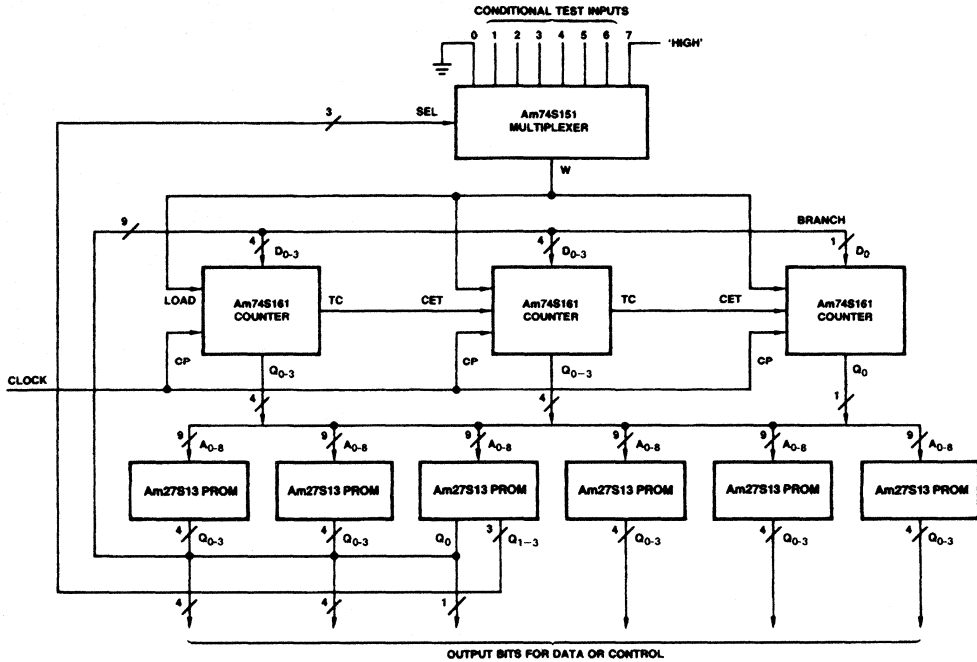
The most negative of the logic power supply pins.

## FUNCTIONAL DESCRIPTION

### Applying the Am27S13

The Am27S13 can be used with a high-speed counter to form a pico-controller for microprogrammed systems. A typical application is illustrated below wherein a multiplexer, under control of one of the PROMs, is continuously sensing the

CONDITIONAL TEST INPUTS. When the selected condition occurs, a HIGH signal will result at the multiplexer output, causing a predetermined branch address to be loaded into the parallel inputs of the counters on the next clock pulse. The counter then accesses the preprogrammed data or control information sequence from the Am27S12 or Am27S13 PROMs.



AF000242

Figure 1. Typical Application for Am27S13

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military Product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub> (Note 1)	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.45	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7 V			25	μA
I <sub>SC</sub> (Note 1)	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 3)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND V <sub>CC</sub> = Max.			130	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	Volts
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>G</sub> = 2.4 V	(Note 1)		40	μA
					-40	
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.00 V, T <sub>A</sub> = 25°C			4	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> /V <sub>OUT</sub> = 2.0 V. @ f = 1 MHz (Note 4)			8	

- Notes: 1. This applies to three-state devices only.  
 2. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.  
 4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

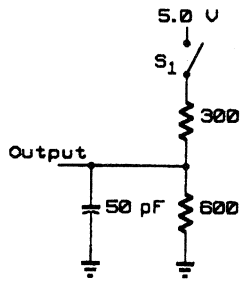
**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

No.	Parameter Symbol	Parameter Description	'A' Version				Standard Version				Unit
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		30		40		50		60	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		25		30	ns

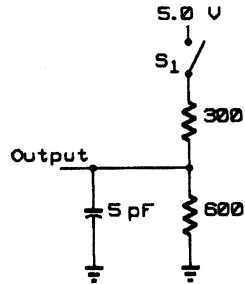
- See also Switching Test Circuits.  
 Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.  
 2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.

\*Subgroups 7 and 8 apply to functional tests.

## SWITCHING TEST CIRCUITS



TC003441



TC003451

### A. Output Load for all tests except TGVQZ

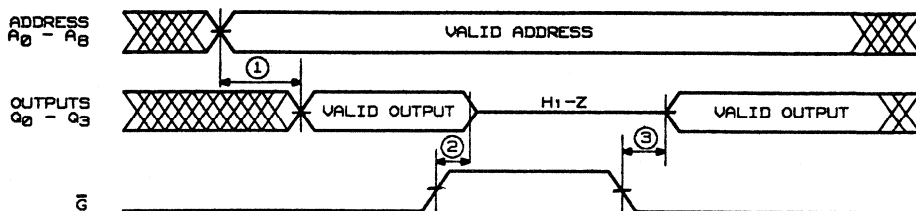
### B. Output Load for TGVQZ

- Notes: 1. All device test loads should be located within 2" of device output pin.  
 2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests.  
 S<sub>1</sub> is closed for all other AC tests.  
 3. Load capacitance includes all stray and fixture capacitance.

## SWITCHING WAVEFORMS KEY TO SWITCHING WAVEFORM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF021180

# Am27S19/27S19A

## Am27S19SA/27LS19

256-Bit (32x8) Bipolar PROM



### DISTINCTIVE CHARACTERISTICS

- Ultra high speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High-programming yield
- Low-current PNP inputs
- High-current open collector and three-state outputs
- Fast chip select

### GENERAL DESCRIPTION

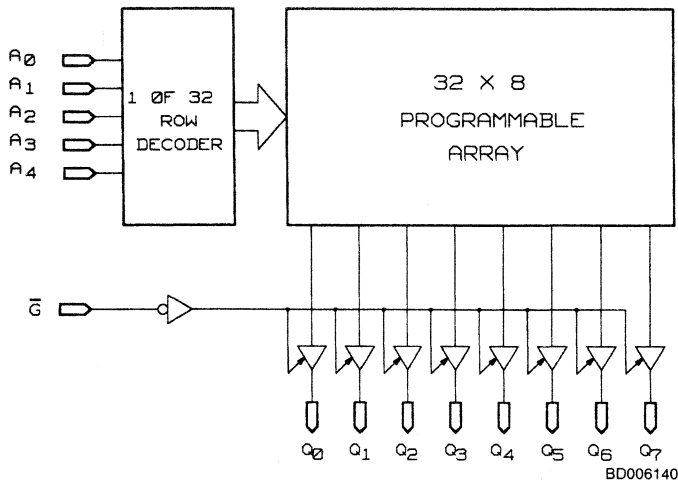
The Am27S19 (32 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in three-state (Am27S19) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping

functions, code conversions, or logic replacements. Easy word depth expansion is facilitated by an active LOW output enable ( $\bar{G}$ ).

This device is also available in a low-power version Am27LS19.

### BLOCK DIAGRAM

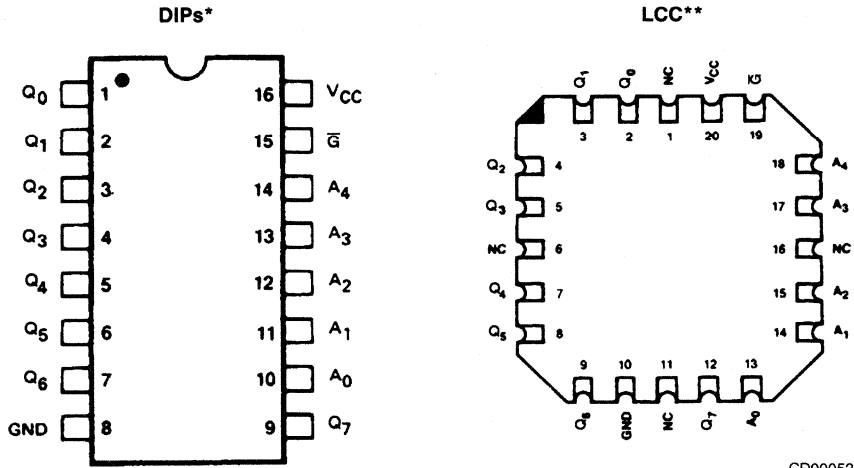


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### PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S19SA		Am27S19A		Am27S19		Am27LS19	
Address Access Time	15 ns	20 ns	25 ns	35 ns	40 ns	50 ns	55 ns	70 ns
Operating Range	C	M	C	M	C	M	C	M

**CONNECTION DIAGRAMS**  
Top View

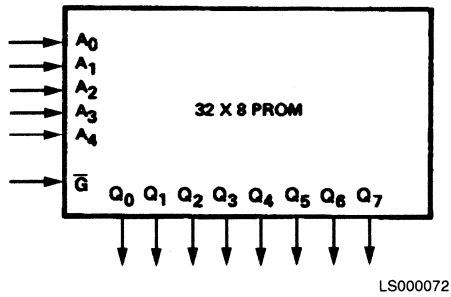


CD000521

CD000531

Note: Pin 1 is marked for orientation.  
 \*Also available in a 16-pin Flatpack. Pinout identical to DIPs.  
 \*\*Also available in a 16-pin Plastic Leaded Chip Carrier. Pinout identical to LCC.

**LOGIC SYMBOL**



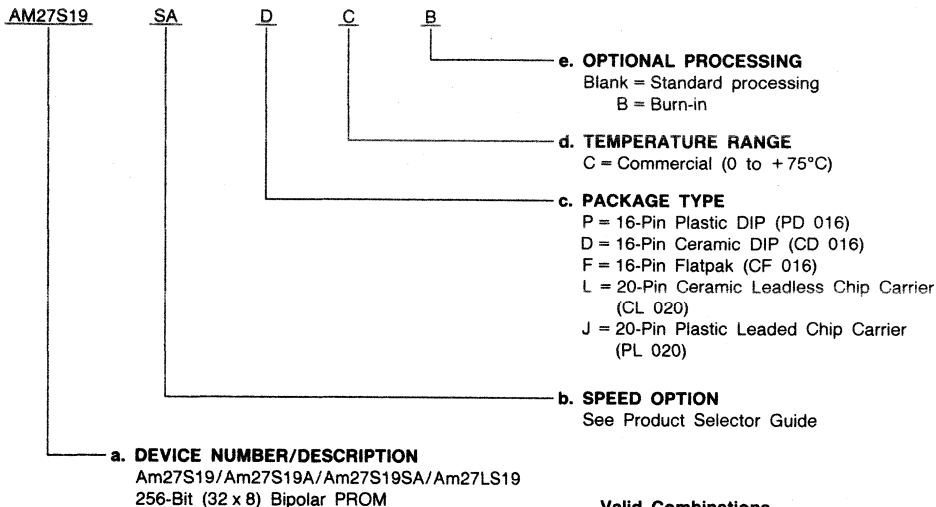
LS000072

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

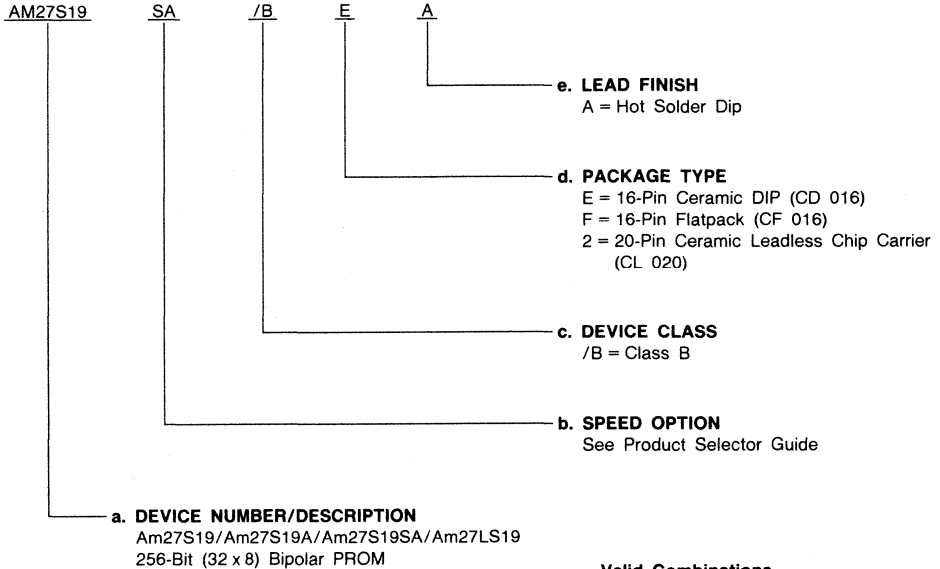
Valid Combinations	
AM27S19	PC, PCB,
AM27S19A	DC, DCB,
AM27S19SA	FC, FCB,
AM27LS19	LC, LCB,
	JC, JCB

# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S19	/BEA, /BFA, /B2A
AM27S19A	
AM27S19SA	
AM27LS19	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.



## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>4</sub> Address Inputs

The 5-bit field presented at the address inputs selects one of 32 memory locations to be read from.

### Q<sub>0</sub> - Q<sub>7</sub> Data Output Port

The outputs whose state represents the data read from the selected memory locations

### $\bar{G}$ Output Enable

Provides direct control of the Q output three-state buffers. Outputs disabled forces all open-collector outputs to an

OFF state and all three-state outputs to a floating or high-impedance state.

Enable =  $\bar{G}$

Disable = G

### V<sub>CC</sub> Device Power Supply Pin

The most positive of the logic power supply pins.

### GND Device Power Supply Pin

The most negative of the logic power supply pins.

## FUNCTIONAL DESCRIPTION

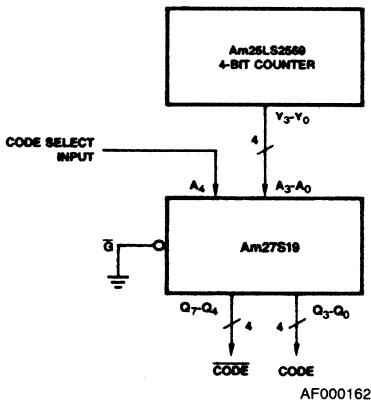
The Am27S19 PROM may be used as a code converter. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code

selector input. The use of a single Am27S19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.

### TRUTH TABLE

ADDRESS					COMPLEMENT				TRUE																		
A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Q <sub>7</sub>	Q <sub>6</sub>	Q <sub>5</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>															
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE														
0	0	0	0	1	1	0	1	1	0	1	0	0		EXCESS THREE CODE													
0	0	0	1	0	1	0	1	0	0	1	0	1			EXCESS THREE CODE												
0	0	0	1	1	1	0	0	1	0	1	1	0				EXCESS THREE CODE											
0	0	1	0	0	1	0	0	0	0	1	1	1					EXCESS THREE CODE										
0	0	1	0	1	0	1	1	1	1	1	0	0						EXCESS THREE CODE									
0	0	1	1	0	0	1	1	0	1	0	0	1							EXCESS THREE CODE								
0	0	1	1	1	0	1	0	1	0	1	1	0								EXCESS THREE CODE							
0	1	0	0	0	0	1	0	0	1	0	1	1									EXCESS THREE CODE						
0	1	0	0	1	0	0	1	1	1	1	1	0										EXCESS THREE CODE					
0	1	0	1	0	X	X	X	X	X	X	X	X											EXCESS THREE CODE				
0	1	0	1	1	X	X	X	X	X	X	X	X												EXCESS THREE CODE			
0	1	1	0	0	X	X	X	X	X	X	X	X													EXCESS THREE CODE		
0	1	1	0	1	X	X	X	X	X	X	X	X														EXCESS THREE CODE	
0	1	1	1	0	X	X	X	X	X	X	X	X															EXCESS THREE CODE
0	1	1	1	1	X	X	X	X	X	X	X	X															
1	0	0	0	0	1	1	1	1	1	0	0	0	GRAY CODE														
1	0	0	0	1	1	1	1	0	0	0	0	1		GRAY CODE													
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1	1	1	1	1	0	1	1	1	1	0	0	0															

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	- 65 to +150°C
Ambient Temperature with Power Applied .....	- 55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec.) .....	250 mA
DC Input Voltage .....	-0.5 V to 5.5 V
DC Input Current .....	- 30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	- 55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military products 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub> (Note 1)	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.45	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7 V			25	μA
I <sub>SC</sub> (Note 1)	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 3)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND, V <sub>CC</sub> = Max.	27S Devices		115	mA
			27LS Devices		80	
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>S</sub> = 2.4 V	(Note 1)	V <sub>O</sub> = V <sub>CC</sub> V <sub>O</sub> = 0.4 V	40 -40	μA
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.00 V., T <sub>A</sub> = 25°C		4		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> /V <sub>OUT</sub> = 2.0 V. @ f = 1 MHz (Note 4)		8		

- Notes: 1. This applies to three-state devices only.  
 2. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.  
 4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

No.	Parameter Symbol	Parameter Description	Version	COM'L		MIL		Unit
				Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time	SA		15		20	ns
			A		25		35	
			STD		40		50	
			LS		55		70	
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	SA		13		20	ns
			A		20		25	
			STD		25		30	
			LS		40		50	
3	TGVQV	Delay from Output Enable Valid to Output Valid	SA		13		20	ns
			A		20		25	
			STD		25		30	
			LS		40		50	

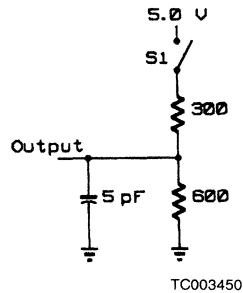
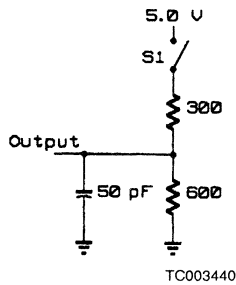
See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.

2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.

\*Subgroups 7 and 8 apply to functional tests.

**SWITCHING TEST CIRCUITS**








**A. Output Load for all tests except TGVQZ**

**B. Output Load for TGVQZ**

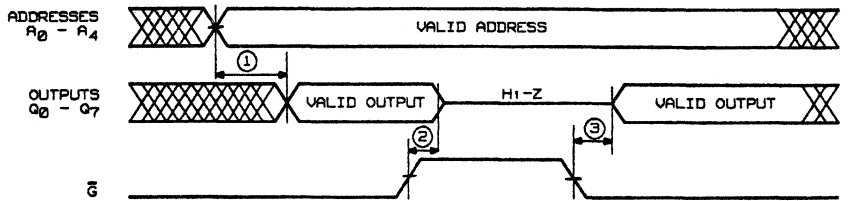
- Notes: 1. All device test loads should be located within 2" of device output pin.  
 2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S<sub>1</sub> is closed for all other AC tests.  
 3. Load capacitance includes all stray and fixture capacitance.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF021160

# Am27S21/27S21A

1,024-Bit (256x4) Bipolar PROM

## DISTINCTIVE CHARACTERISTICS

- High speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

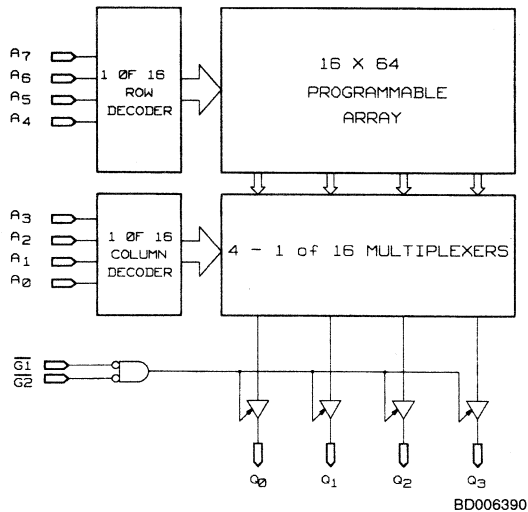
## GENERAL DESCRIPTION

The Am27S21 (256 words by 4-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is only available in a three-state (Am27S21) output version. These outputs are compatible with low-

power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code version, or logic replacement. Easy word-depth expansion is facilitated by active LOW ( $\overline{G}_1$  and  $\overline{G}_2$ ) output enables.

## BLOCK DIAGRAM

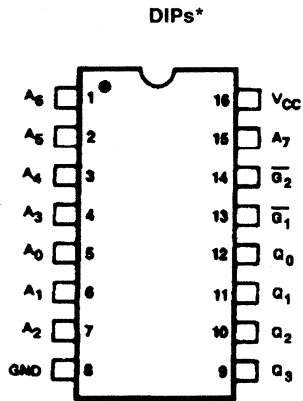


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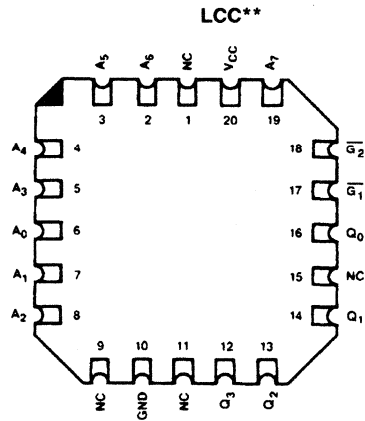
## PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S21A		Am27S21	
	Address Access Time	30 ns	40 ns	45 ns
Operating Range	C	M	C	M

**CONNECTION DIAGRAMS**  
**Top View**



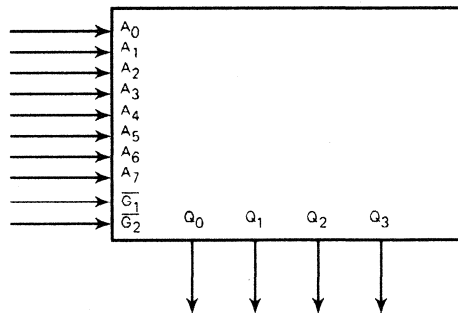
CD000571



CD000581

\*Also available in a 16-Pin Flatpack. Pinout identical to DIPs.  
 \*\*Also available in a 20-Pin Square PLCC. Pinout identical to LCC.  
 Note: Pin 1 is marked for orientation.

**LOGIC SYMBOL**



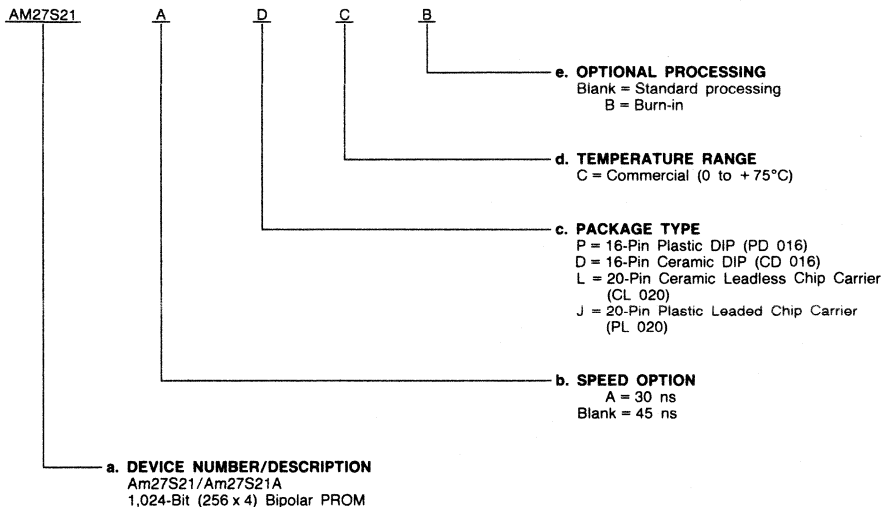
LS000081

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27S21	DC, DCB, PC, PCB,
AM27S21A	LC, LCB, JC, JCB

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

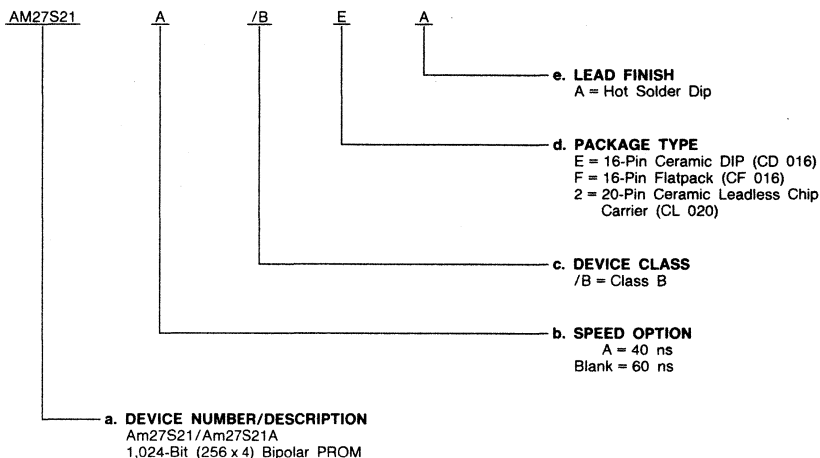
5

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM27S21	/BEA, /BFA, /B2A
AM27S21A	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.



## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>7</sub> Address Inputs (Inputs)

The 8-bit field presented at the address inputs selects one of 256 memory locations to be read from.

### Q<sub>0</sub> - Q<sub>3</sub> Data Output Port (Outputs)

The output whose state represents the data read from the selected memory locations.

### $\overline{G}_1$ , $\overline{G}_2$ Output Enable

Provides direct control of the Q output buffers. Outputs disabled force all open-collector outputs to an OFF state

and all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G}_1 \cdot \overline{G}_2$$

$$\begin{aligned} \text{Disable} &= \overline{G}_1 \cdot G_2 \\ &= G_1 + G_2 \end{aligned}$$

### V<sub>CC</sub> Device Power Supply Pin

The most positive of the logic power supply pins.

### GND Device Power Supply Pin

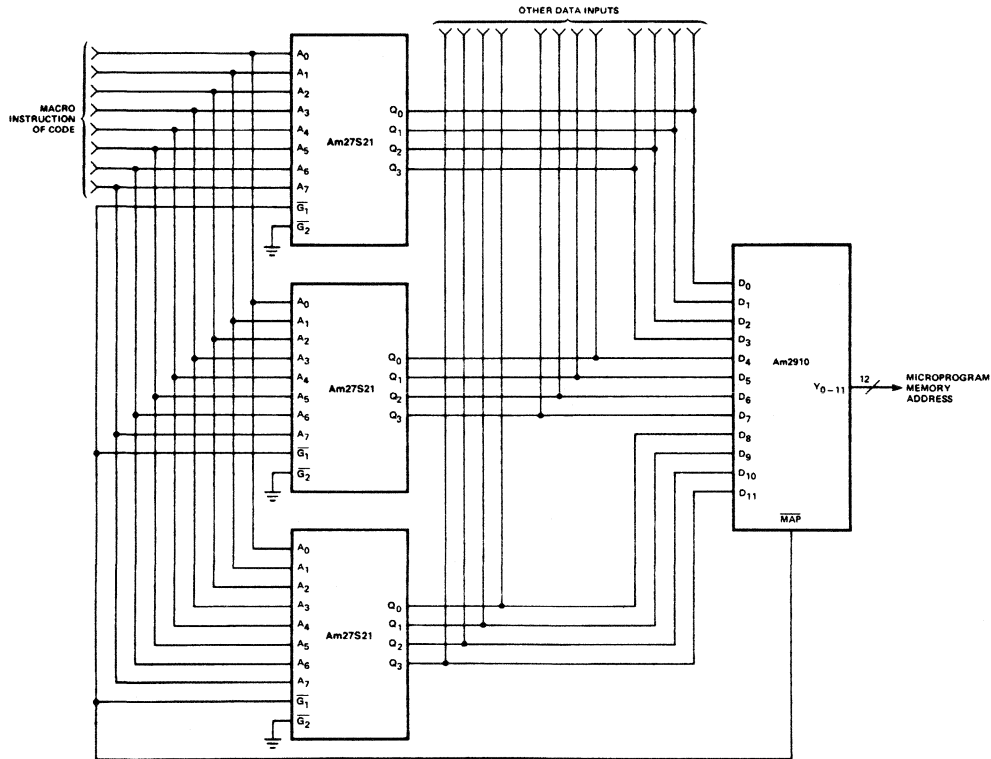
The most negative of the logic power supply pins.

## FUNCTIONAL DESCRIPTION

### Applying The Am27S21

Typical application of the Am27S21 is shown below. The Am27S21 is employed as mapping ROMs in a microprogram computer control unit. The eight-bit macroinstruction from main memory is brought into the A<sub>0</sub> - A<sub>7</sub> inputs of the mapping ROM array. The instruction is mapped into a 12-bit address

space with each PROM output supplying 4 bits. The 12 bits of address are then supplied to the "D" inputs of the Am2910 as a possible next address source for microprogram memory. The MAP output of the Am2910 is connected to the  $\overline{G}_1$  input of the Am27S21 such that when the  $\overline{G}_1$  input is HIGH, the outputs of the PROMs are in the three-state mode in the case of the Am27S21. The  $\overline{G}_2$  input is grounded; thus data from other sources are free to drive the D inputs of the Am2910 when  $\overline{MAP}$  is HIGH.



AF000232

Figure 1. Microprogramming Instruction Mapping

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military product 100% tested at T<sub>C</sub> +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub> (Note 1)	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.45	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7 V			25	μA
I <sub>SC</sub> (Note 1)	Output Short Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V (Note 3)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND, V <sub>CC</sub> = Max.			130	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max., V <sub>G1</sub> = 2.4 V (Note 1)			40	μA
		V <sub>O</sub> = V <sub>CC</sub> V <sub>O</sub> = 0.4 V			-40	
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.00 V., T <sub>A</sub> = 25°C		4		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> /V <sub>OUT</sub> = 2.0 V. @ f = 1 MHz (Note 4)		8		

Notes: 1. This applies to three-state devices only.

2. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

No.	Parameter Symbol	Parameter Description	Am27S21A				Am27S21				Unit
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		30		40		45		60	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		20		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		20		30	ns

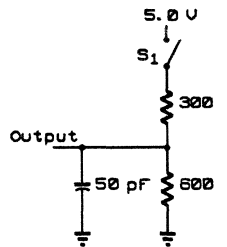
See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.

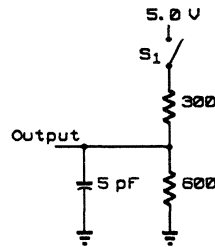
2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.

\*Subgroups 7 and 8 apply to functional tests.

**SWITCHING TEST CIRCUITS**



TC003460



TC003470

**A. Output Load for all tests except TGVQZ**






**B. Output Load for TGVQZ**

- Notes: 1. All device test loads should be located within 2" of device output pin.  
 2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S<sub>1</sub> is closed for all other AC tests.  
 3. Load capacitance includes all stray and fixture capacitance.

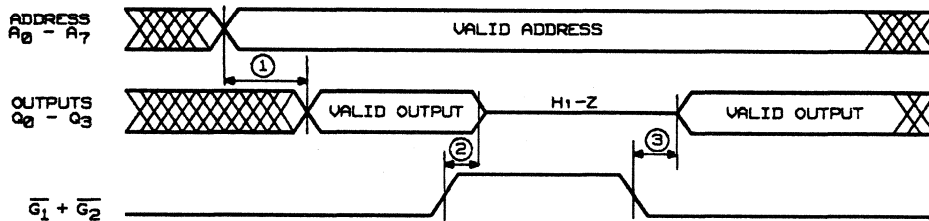


# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF021170

# Am27S25/27S25A/27S25SA

4096-Bit (512x8) Bipolar Registered PROM  
with Preset and Clear Inputs



## DISTINCTIVE CHARACTERISTICS

- 'SA' version offers ultrafast AC performance (25 ns set-up and 12 ns clock-to-output)
- On-chip edge-triggered registers — ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Buffered common Preset ( $\overline{PS}$ ) and Clear ( $\overline{CR}$ ) inputs
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ > 98%)

## GENERAL DESCRIPTION

The Am27S25 (512 words by 8 bits) is a fully decoded, Schottky array, TTL Programmable Read-Only Memory (PROM), incorporating D-type master-slave data registers on chip. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

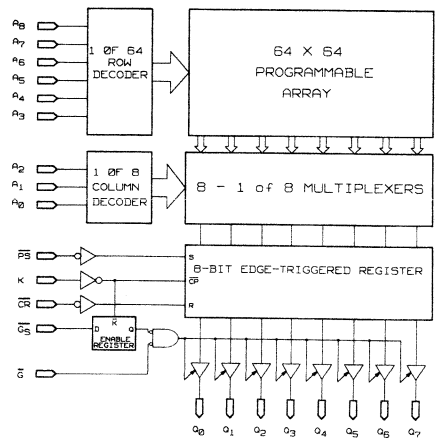
This device contains an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the

requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, this device contains both asynchronous and synchronous output enables as well as common asynchronous preset and clear register controls.

Upon power-up the outputs ( $Q_0 - Q_7$ ) will be in a floating or high-impedance state.

## BLOCK DIAGRAM



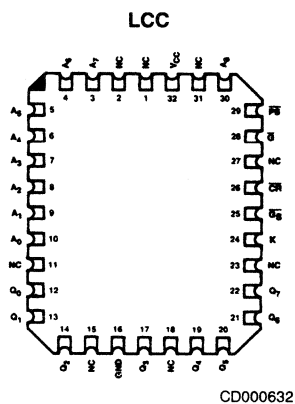
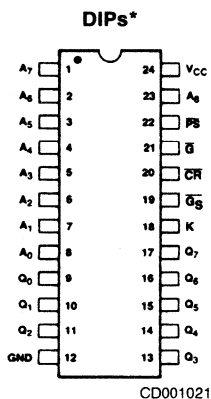
5

## PRODUCT SELECTOR GUIDE

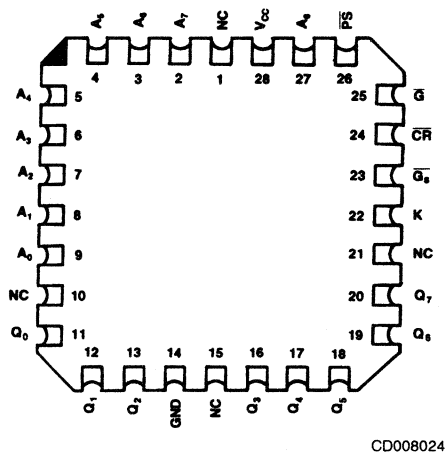
Part Number	Am27S25SA		Am27S25A		Am27S25	
Address Set-up Time (ns)	25	30	30	35	50	55
Clock-to-Ouput Delay (ns)	12	15	20	25	27	30
Operating Range	C	M	C	M	C	M

Publication # 03300 Rev. E Amendment /0  
Issue Date: January 1989

## CONNECTION DIAGRAMS Top View



### LCC\*\*

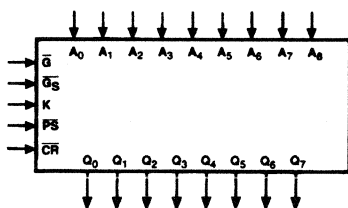


Note: Pin 1 is marked for orientation.

\*Also available in a 24-pin Flatpack. Pinout identical to DIPs.

\*\*Also available in a 28-pin square PLCC. Pinout identical to LCC.

## LOGIC SYMBOL



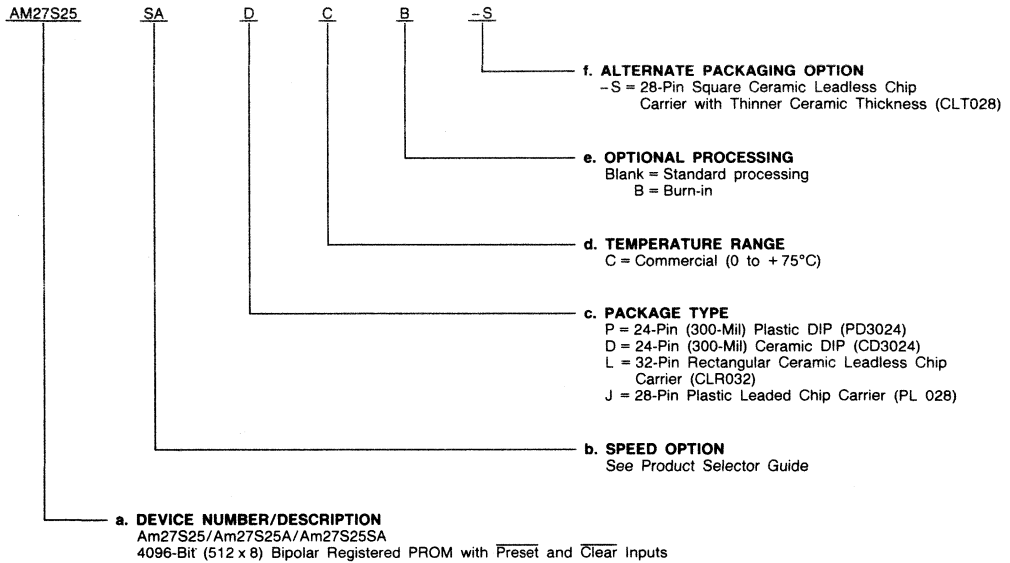
LS000113

# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number**
- b. Speed Option** (if applicable)
- c. Package Type**
- d. Temperature Range**
- e. Optional Processing**
- f. Alternate Packaging Option**



Valid Combinations	
AM27S25	DC, DCB, PC,
AM27S25A	PCB, LC, LCB,
Am27S25SA	LC-S, LCB-S JC, JCB

### Valid Combinations

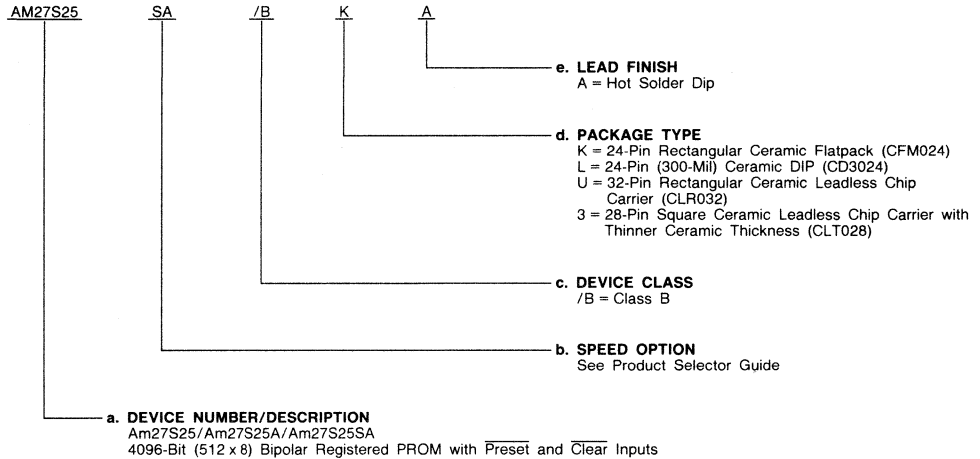
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
Am27S25	
Am27S25A	/BKA, /BLA, /BUA, /B3A
Am27S25SA	

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revisions of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.



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## PIN DESCRIPTION

### **A<sub>0</sub> – A<sub>8</sub> Address (Inputs)**

The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

### **K Clock**

CP is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of CP.

### **Q<sub>0</sub> – Q<sub>7</sub> Data Port (Outputs, Three-State)**

Parallel data output from the pipeline register. The disabled state of these outputs is floating or high-impedance.

### **$\overline{G}$ Asynchronous Output Enable**

Provides direct control of the Q<sub>n</sub> output three-state drivers, independent of CP.

### **$\overline{G_S}$ Synchronous Output Enable**

Controls the state of the Q<sub>n</sub> output three-state drivers, in conjunction with CP. This is useful where more than one

registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

### **$\overline{PS}$ Asynchronous Preset**

Control pin used to force the state of the output data registers HIGH, independent of CP. This can be used to generate a condition for system interrupt or initialization.

### **$\overline{CR}$ Asynchronous Clear**

Control pin used to force the state of the output data registers LOW, independent of CP. This can be used to generate a condition for system interrupt or initialization.

### **V<sub>CC</sub> Power Supply Pin**

The most positive of the logic power supply pins.

### **GND Power Supply Pin**

The most negative of the logic power supply pins.

---

## FUNCTIONAL DESCRIPTION

When V<sub>CC</sub> power is first applied, the synchronous enable ( $\overline{G_S}$ ) flip-flop will be in the set condition causing the outputs (Q<sub>0</sub> – Q<sub>7</sub>) to be in the OFF or high-impedance state. This occurs regardless of the state of the asynchronous enable input. A LOW-to-HIGH transition of the clock input (K) while  $\overline{G_S}$  input is LOW is required after power-up in order to enable the outputs to an active state. Reading data is accomplished by first applying the binary word address to the address inputs (A<sub>0</sub> – A<sub>8</sub>) and a logic LOW to the synchronous enable ( $\overline{G_S}$ ). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (K), data is transferred to the slave flip-flops which drive the output buffers. Provided that the asynchronous enable ( $\overline{G}$ ) is also LOW, stored data will appear on the outputs (Q<sub>0</sub> – Q<sub>7</sub>). If  $\overline{G_S}$  is HIGH when the positive clock edge occurs, outputs go to the OFF or high-impedance state regardless of the state of  $\overline{G}$ . The outputs may be disabled at any time by switching  $\overline{G}$  to a HIGH

level. Following the positive clock edge the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

The Am27S25 has buffered Asynchronous Preset ( $\overline{PS}$ ) and Clear ( $\overline{CR}$ ) inputs. These functions are common to all registers and are useful during power-up timeout sequences. With outputs enabled, the  $\overline{PS}$  input asserted LOW will cause all outputs to be set to a logic 1 (HIGH) state. When the  $\overline{CR}$  input is LOW, the internal flip-flops of the data register are reset and a logic 0 (LOW) will appear on all outputs. These functions will control the state of the data register, independent of all other inputs but exclusive of each other.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 to +5.5 V
DC Input Current .....	-30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>			40	μA
I <sub>SC</sub>	Output Short Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 2)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND, V <sub>CC</sub> = Max.			185	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>E</sub> = 2.4 V			40	μA
		V <sub>O</sub> = V <sub>CC</sub> V <sub>O</sub> = 0.4 V			-40	
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.00 V, T <sub>A</sub> = 25°C		4		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> /V <sub>OUT</sub> = 2.0 V. @ f = 1 MHz (Note 4)		8		

- Notes: 1. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 2. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.  
 3. These parameters are not 100% tested, but are periodically sampled at initial characterization and at any time the design is modified where capacitance may be affected.  
 4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55°C to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military products 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*) (Note 1)

No.	JEDEC Parameter Symbol	Parameter Description	Am27S25SA		Am27S25A		Am27S25		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
1	TAVKH	Address to K HIGH Setup Time	COM'L	25		30		50	ns	
			MIL	30		35		55		
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		0	ns	
			MIL	0		0		0		
3	TKHQV1	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW) (Note 3)	COM'L	4	12		20		27	ns
			MIL	4	15		25		30	
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	15		20		20	ns	
			MIL	20		20		20		
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW)	COM'L		20		25		35	ns
			MIL		25		30		45	
6	TGHQZ	Asynchronous Output Enable HIGH to Output Hi-Z (See Note 2)	COM'L		20		25		35	ns
			MIL		25		30		45	
7	TGSVKH	$\overline{GS}$ to K HIGH Setup Time	COM'L	10		10		15	ns	
			MIL	10		10		15		
8	TKHGSX	$\overline{GS}$ to K HIGH Hold Time	COM'L	0		5		5	ns	
			MIL	0		5		5		
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs	COM'L		20		25		35	ns
			MIL		25		30		45	
10	TKHQZ	Delay from K HIGH to Output Hi-Z (See Note 2)	COM'L		20		25		35	ns
			MIL		25		30		45	
11	TPSLQV TCRLQV	Delay from $\overline{PS}$ or $\overline{CR}$ LOW to Output Valid (HIGH or LOW)	COM'L		20		20		25	ns
			MIL		25		25		30	
12	TPSHKH TCRHHK	Asynchronous $\overline{PS}$ or $\overline{CR}$ Recovery Time	COM'L	15		20		20	ns	
			MIL	20		25		25		
13	TPSLPSH TCRLCRH	Asynchronous $\overline{PS}$ or $\overline{CR}$ Pulse Width (LOW)	COM'L	15		20		20	ns	
			MIL	20		25		25		

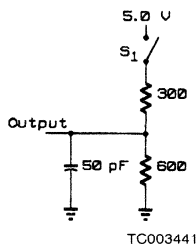
See also Switching Test Circuits.

- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A. under Switching Test Circuits.  
 2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage - 0.5 V and steady state LOW output voltage + 0.5 V output levels using the test load in B. under Switching Test Circuits.  
 3. Minimum delay is guaranteed by design and supported by characterization data.

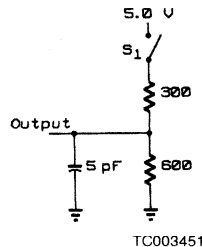
\*Subgroups 7 and 8 apply to functional tests.

**5**

**SWITCHING TEST CIRCUITS**



**A. Output Load for all tests except TGVQZ and TKHQZ**









**B. Output Load for TGVQZ and TKHQZ**

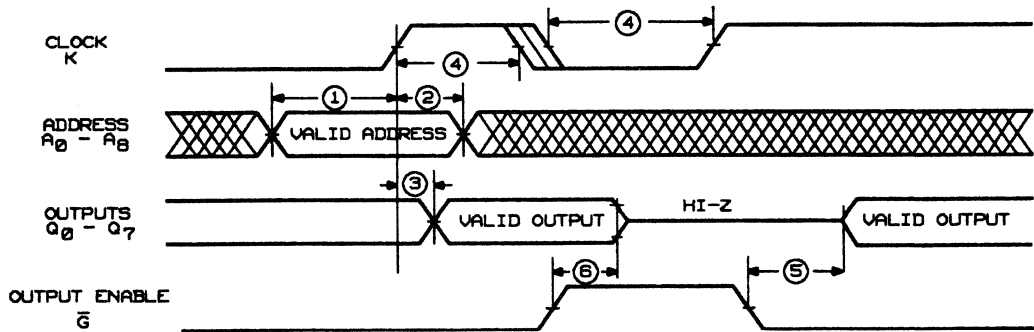
- Notes: 1. All device test loads should be located within 2" of device output pin.  
 2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S<sub>1</sub> is closed for all other AC tests.  
 3. Load capacitance includes all stray and fixture capacitance.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
 	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

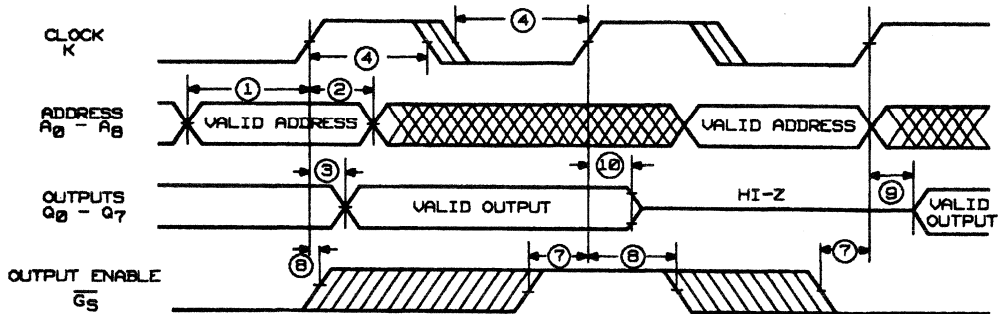
KS000010



WF021130

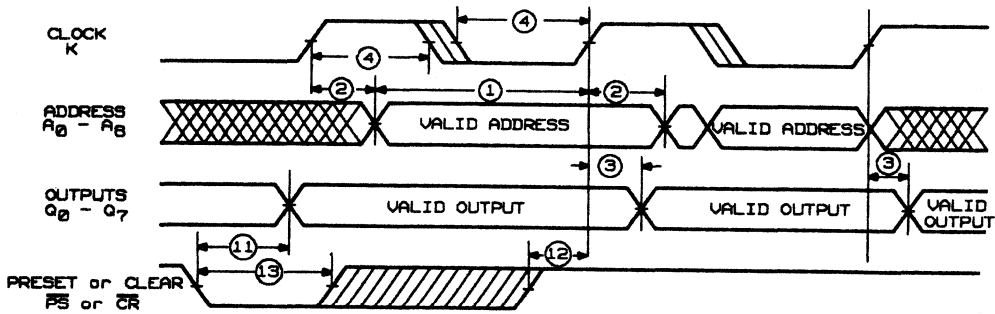
**Diagram A. Using Asynchronous Enable**

SWITCHING WAVEFORMS (Cont'd.)



WF021140

Diagram B. Using Synchronous Enable



WF021150

Diagram C. Using Asynchronous  $\overline{P}R\overline{E}S\overline{T}$  or  $\overline{C}L\overline{E}A\overline{R}$

# Am27S27/27S27A

4,096-Bit (512x8) Bipolar Registered PROM

## DISTINCTIVE CHARACTERISTICS

- On-chip, edge-triggered registers — ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up
- Fast 30 ns address setup and 17 ns clock to output times
- Excellent performance over the military range
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)

## GENERAL DESCRIPTION

The Am27S27 (512 words by 8 bits) is a fully decoded, Schottky array, TTL-Programmable Read-Only Memory (PROM), incorporating D-type master-slave data registers on chip. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

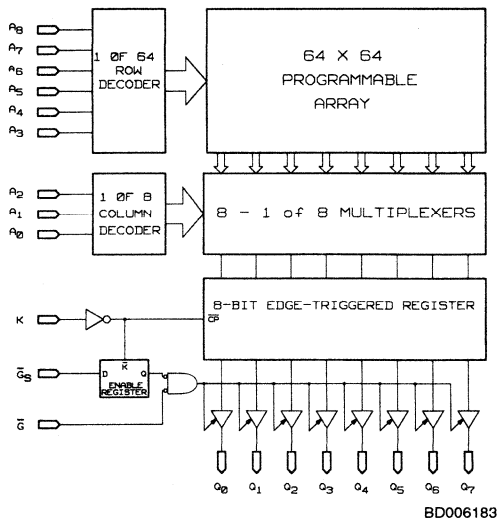
This device contains an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored

while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, this device contains both asynchronous and synchronous output enables.

Upon power-up the outputs (Q<sub>0</sub> – Q<sub>7</sub>) will be in a floating or high-impedance state.

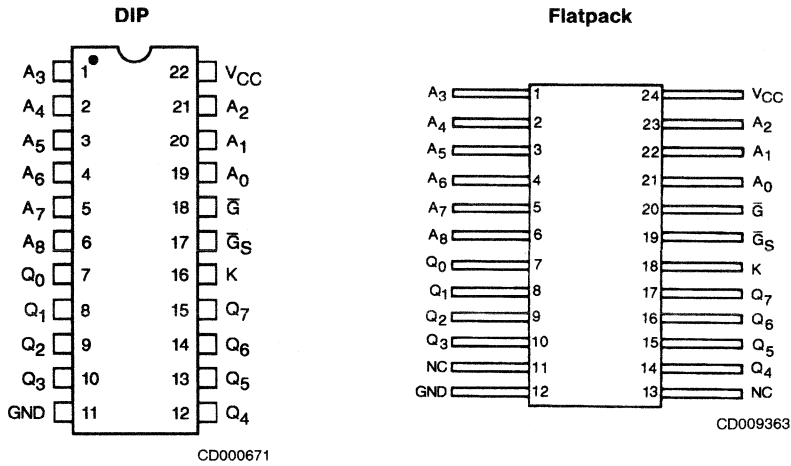
## BLOCK DIAGRAM



## PRODUCT SELECTOR GUIDE

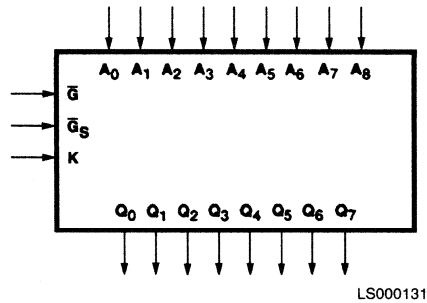
Part Number	Am27S27A		Am27S27	
	30 ns	35 ns	50 ns	55 ns
Address Setup Time	30 ns	35 ns	50 ns	55 ns
Clock-to-Output Delay	17 ns	20 ns	27 ns	30 ns
Operating Range	C	M	C	M

**CONNECTION DIAGRAMS**  
**Top View**



Note: Pin 1 is marked for orientation.

**LOGIC SYMBOL**

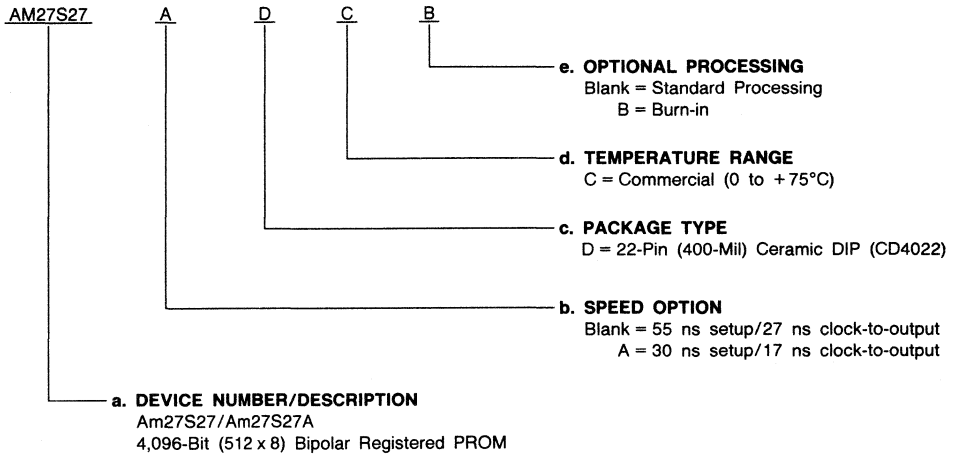


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number**
- b. Speed Option** (if applicable)
- c. Package Type**
- d. Temperature Range**
- e. Optional Processing**



#### Valid Combinations

Valid Combinations list configurations planned to supported in volume for this device. Consult the local AMD sales office to confirm availability of specific combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM27S27	DC, DCB
AM27S27A	



## MILITARY ORDERING INFORMATION

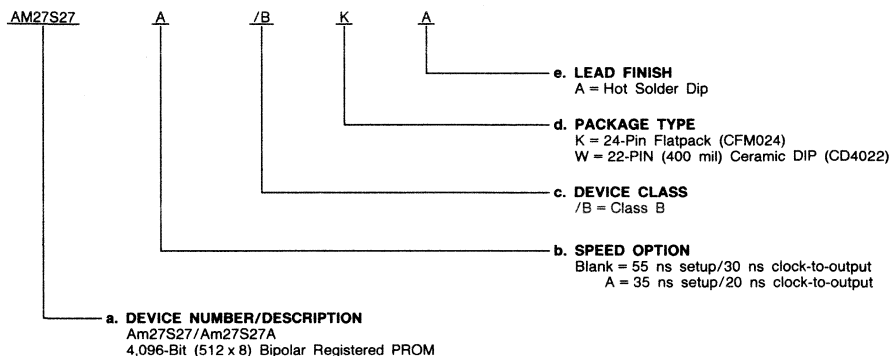
### APL and CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

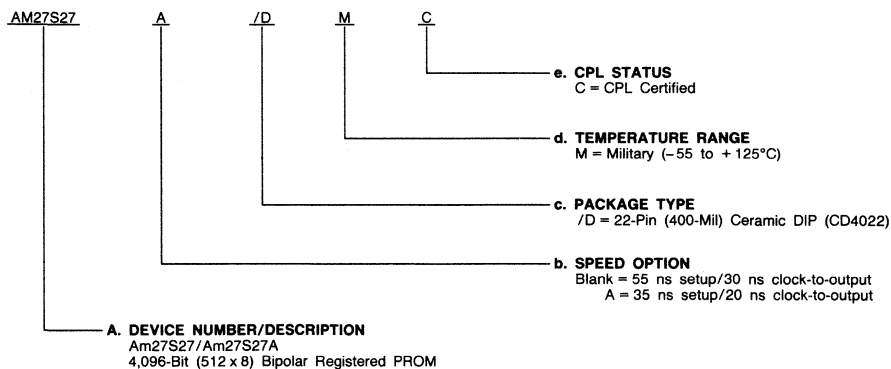
- APL Products:**
- a. Device Number
  - b. Speed Option (if applicable)
  - c. Device Class
  - d. Package Type
  - e. Lead Finish

- CPL Products:**
- a. Device Number
  - b. Speed Option (if applicable)
  - c. Package Type
  - d. Temperature Range
  - e. CPL Status

#### APL Products



#### CPL Products



Valid Combinations		
APL	AM27S27	/BKA, /BWA
	AM27S27A	
CPL	AM27S27	/DMC
	AM27S27A	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

## MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

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## PIN DESCRIPTION

### **A<sub>0</sub> – A<sub>8</sub> Address Inputs (Input)**

The 9-bit field presented at the address inputs selects one of the 512 memory locations to be read from.

### **K Clock (Input)**

The clock is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

### **Q<sub>0</sub> – Q<sub>7</sub> Data Output Port (Output)**

Parallel data output from the pipeline register. The disabled state of these outputs is floating or high impedance.

### **$\overline{G}_S$ Asynchronous Output Enable (Input)**

Provides direct control of the Q<sub>n</sub> output three-state drivers independent of K.

### **$\overline{G}_S$ Synchronous Output Enable (Input)**

Controls the state of the Q<sub>n</sub> output three-state drivers in conjunction with K. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

### **V<sub>CC</sub> Device Power Supply Pin**

The most positive of the logic power supply pins.

### **GND Device Power Supply Pin**

The most negative of the logic power supply pins.

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## FUNCTIONAL DESCRIPTION

When V<sub>CC</sub> power is first applied, the synchronous enable ( $\overline{G}_S$ ) flip-flop will be in the set condition causing the outputs, Q<sub>0</sub> – Q<sub>7</sub>, to be in the OFF or high-impedance state, eliminating the need for a register clear input. This occurs regardless of the state of the asynchronous enable input. A LOW-to-HIGH transition of the clock input (K) while  $\overline{G}_S$  input is LOW is required after power-up in order to enable the outputs to an active state. Reading data is accomplished by first applying the binary word address to the address inputs, A<sub>0</sub> – A<sub>8</sub>, and a logic LOW to the synchronous output enable,  $\overline{G}_S$ . During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, K, data is trans-

ferred to the slave flip-flops which drive the output buffers. Provided that the asynchronous enable,  $\overline{G}_A$ , is also LOW, stored data will appear on the outputs, Q<sub>0</sub> – Q<sub>7</sub>. If  $\overline{G}_S$  is HIGH when the positive clock edge occurs, outputs go to the OFF or high-impedance state. The outputs may be disabled at any time by switching  $\overline{G}_A$  to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with	
Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs	
(Except During Programming) .....	-0.5 to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs	
During Programming .....	21 V
Output Current into Outputs During	
Programming (Max Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

\*Military product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)			.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7 V			25	μA
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 5.5 V			40	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 2)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND V <sub>CC</sub> = Max.			185	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>E</sub> = 2.4 V			40	μA
		V <sub>O</sub> = 4.5 V V <sub>O</sub> = 0.4 V			-40	
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.00 V., T <sub>A</sub> = 25°C (Note 3)		5		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> /V <sub>OUT</sub> = 2.0 V. @ f = 1 MHz (Note 3)		12		

- Notes: 1. Typical limits are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.  
 2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.  
 3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.  
 4. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

5

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*) (see Note 1)

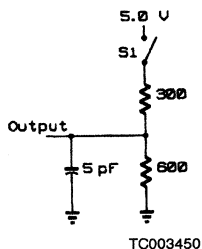
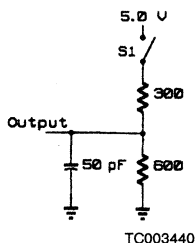
No.	Parameter Symbol	Parameter Description	Am27S27A		Am27S27		Unit	
			Min.	Max.	Min.	Max.		
1	TAVKH	Address to K HIGH Setup Time	COM'L	30		50		ns
			MIL	35		55		ns
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		ns
			MIL	0		0		ns
3	TKHQV1	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW)	COM'L		17		27	ns
			MIL		20		30	ns
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	20		20		ns
			MIL	20		20		ns
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW)	COM'L		25		35	ns
			MIL		30		45	ns
6	TGHQZ	Asynchronous Output Enable HIGH to Output High Z (see Note 2)	COM'L		25		30	ns
			MIL		30		40	ns
7	TGSVKH	$\overline{GS}$ to K HIGH Setup Time	COM'L	10		12		ns
			MIL	10		15		ns
8	TKHGSX	$\overline{GS}$ to K HIGH Hold Time	COM'L	0		0		ns
			MIL	0		0		ns
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs	COM'L		25		35	ns
			MIL		30		45	ns
10	TKHQZ	Delay from K HIGH to Output Hi-Z (see Note 2)	COM'L		25		35	ns
			MIL		30		45	ns

See also Switching Test Circuit Diagrams.

- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A,  
 2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B.

\*Subgroups 7 and 8 apply to functional tests.

**SWITCHING TEST CIRCUITS**








**A. Output Load for all tests except TGVQZ and TKHQZ**

**B. Output Load for TGVQZ and TKHQZ**

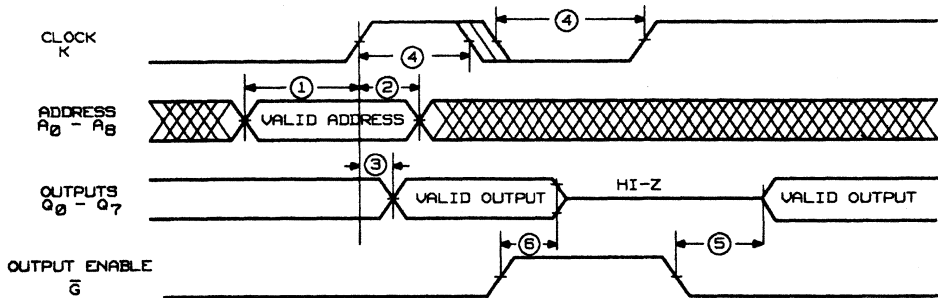
- Notes: 1. All device test loads should be located within 2" of device output pin.  
 2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests.  
 S<sub>1</sub> is closed for all other AC tests.  
 3. Load capacitance includes all stray and fixture capacitance.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

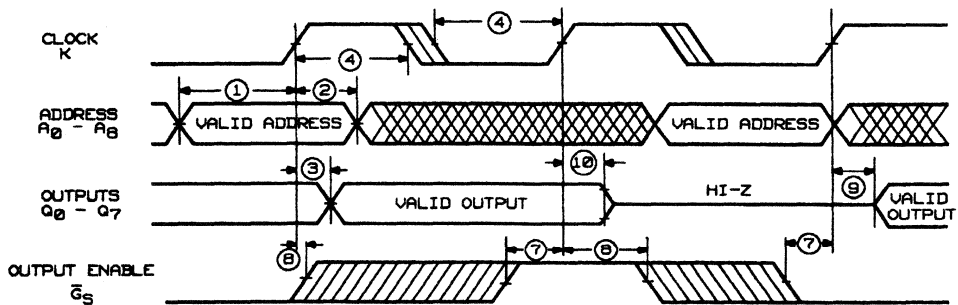
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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WF021110

**Diagram A. Using Asynchronous Enable**



WF021121

**Diagram B. Using Synchronous Enable**

5



# Am27S29/Am27S29A/Am27S29SA

4,096-Bit (512x8) Bipolar PROM

## DISTINCTIVE CHARACTERISTICS

- High Speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

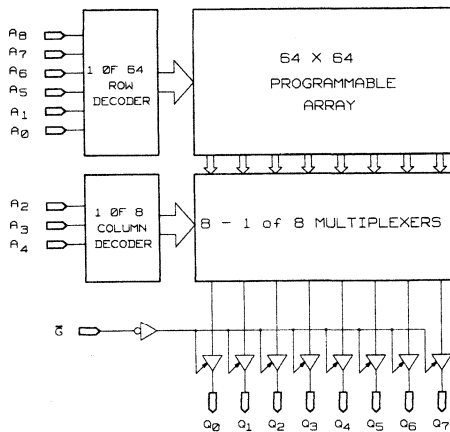
## GENERAL DESCRIPTION

The Am27S29 (512-words by 8-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs, compatible with low-power Schottky bus standards capable of satisfying the

requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word depth expansion is facilitated by an active LOW ( $\bar{G}$ ) output enable.

## FUNCTIONAL BLOCK DIAGRAM



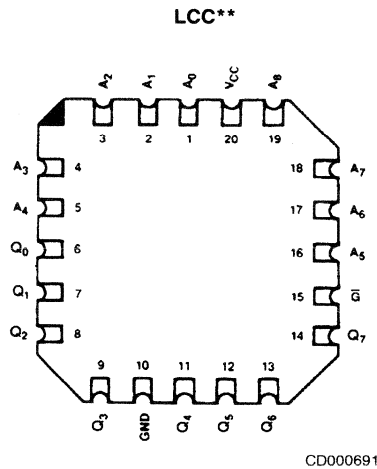
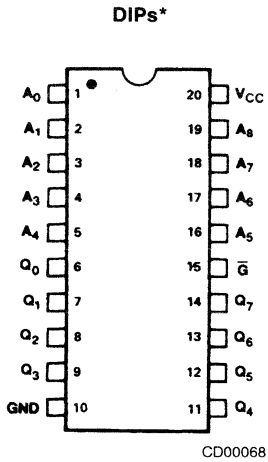
BD006182

## PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S29SA		Am27S29A		Am27S29	
Address Access Time	30 ns	40 ns	35 ns	45 ns	55 ns	70 ns
Operating Range	C	M	C	M	C	M

## CONNECTION DIAGRAMS

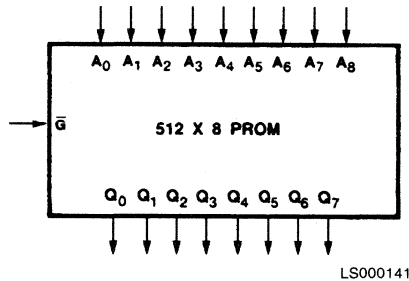
### Top View



\*Also available in a 20-pin Flatpack. Pinout identical to DIPs.  
 \*\*Also available in a 20-pin PLCC. Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL

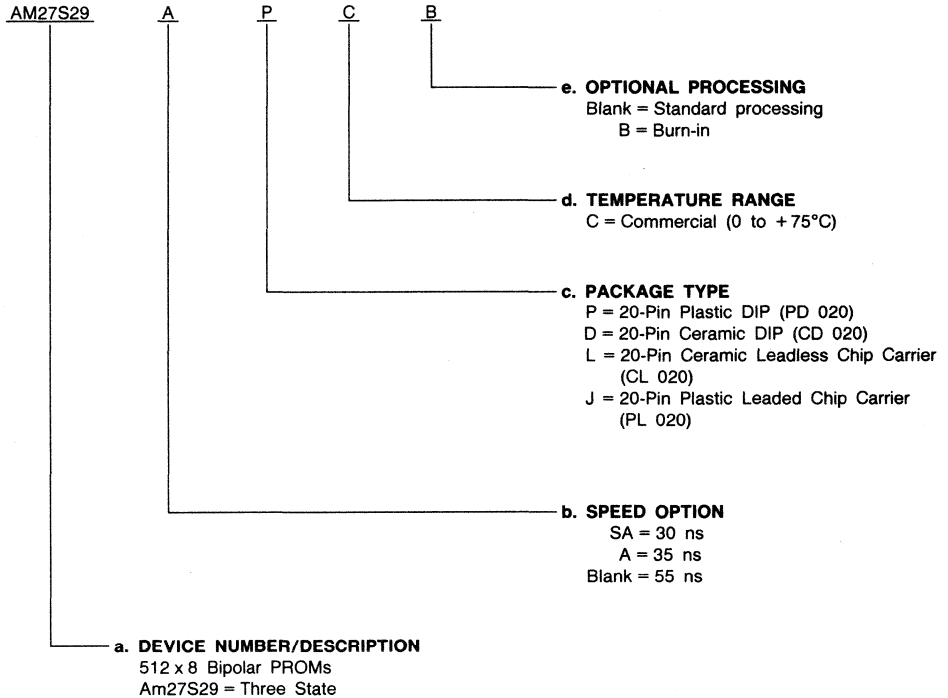


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number**
- b. Speed Option** (if applicable)
- c. Package Type**
- d. Temperature Range**
- e. Optional Processing**



Valid Combinations	
AM27S29	PC, PCB, DC, DCB, LC, LCB, JC, JCB
AM27S29A	
AM27S29SA	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

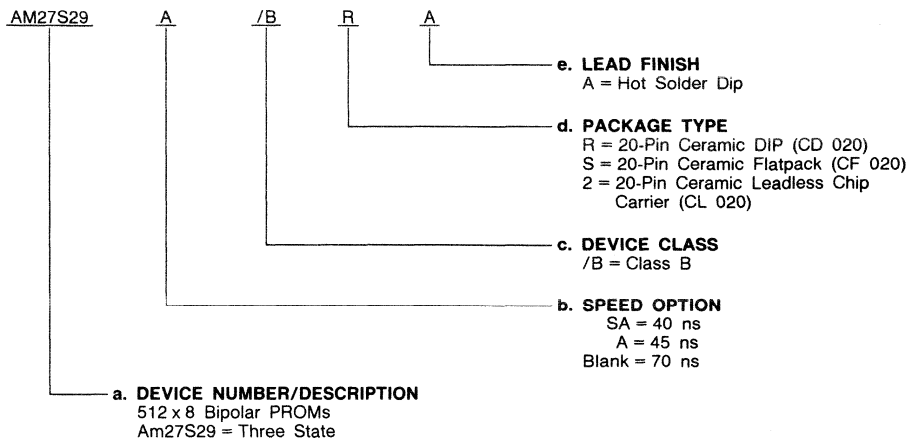


## ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM27S29	
AM27S29A	/BRA, /BSA, /B2A
AM27S29SA	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A Tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

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### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

### PIN DESCRIPTION

#### **A<sub>0</sub> - A<sub>8</sub> Address (Inputs)**

The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

#### **Q<sub>0</sub> - Q<sub>7</sub> Data Output Port**

The outputs whose state represents the data read from the selected memory locations.

#### **$\bar{G}$ Output Enable (Input)**

Provides direct control of the Q-output buffers. Outputs disabled forces all three-state outputs to a floating or high-impedance state.

Enable =  $\bar{G}$

Disable = G

#### **V<sub>CC</sub> Device Power Supply Pin**

The most positive of the logic power supply pins.

#### **GND Device Power Supply Pin**

The most negative of the logic power supply pins.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	- 65 to +150°C
Ambient Temperature with Power Applied .....	- 55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub> (Note 1)	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7 V			25	μA
I <sub>SC</sub> (Note 1)	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 3)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND V <sub>CC</sub> = Max.			160	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>C</sub> EX	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>G</sub> = 2.4 V (Note 1)			40	μA
		V <sub>O</sub> = V <sub>CC</sub> V <sub>OUT</sub> = 0.4 V			-40	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5 V; T <sub>A</sub> = 25°C		4		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5 V; T <sub>A</sub> = 25°C		8		

- Notes:
- This applies to three-state devices only.
  - V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
  - Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
  - These parameters are not 100% tested, but are periodically evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

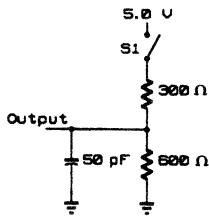
No.	Parameter Symbol	Parameter Description	"SA" Version				"A" Version				Standard Version				Units
			COM'L		MIL		COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		30		40		35		45		55		70	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		20		25		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		20		25		25		30	ns

See also Switching Test Circuits.

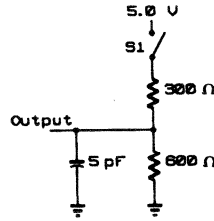
- Notes:
- Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in Figure A.
  - TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in Figure B.

\*Subgroups 7 and 8 apply to functional tests.

## SWITCHING TEST CIRCUITS



TC003442



TC003452

### A. Output Load for all A-C tests except TGVQZ

### B. Output Load for TGVQZ

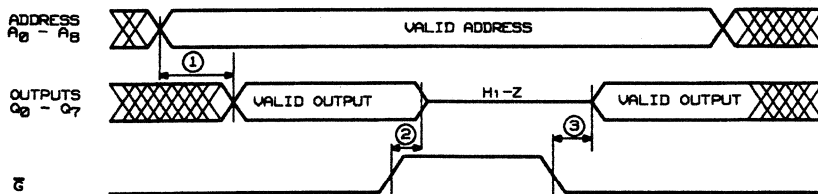
- Notes:
1. All device test loads should be located within 2" of device output pin.
  2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S<sub>1</sub> is closed for all other AC tests.
  3. Load capacitance includes all stray and fixture capacitance.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF021240

# Am27S31/27S31A

(512x8) Bipolar PROM

## DISTINCTIVE CHARACTERISTICS

- High speed — 35 ns max commercial range access time
- Excellent performance over full military and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current and three-state outputs
- Fast chip select

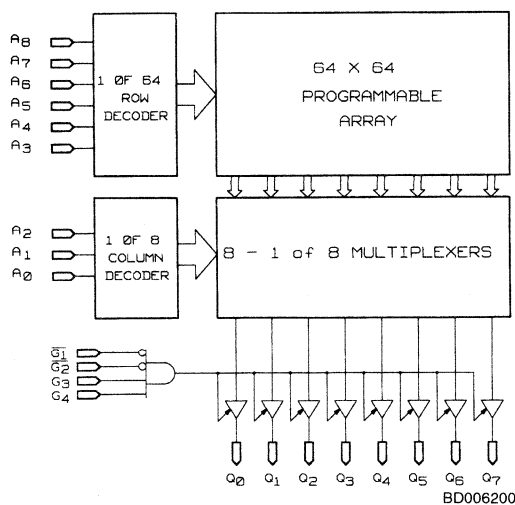
## GENERAL DESCRIPTION

The Am27S31 (512 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in three-state output version compatible with low-power Schottky bus standards capable

of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by both active LOW ( $\bar{G}_1$  and  $\bar{G}_2$ ) and active HIGH ( $G_3$  and  $G_4$ ) output enables.

## BLOCK DIAGRAM



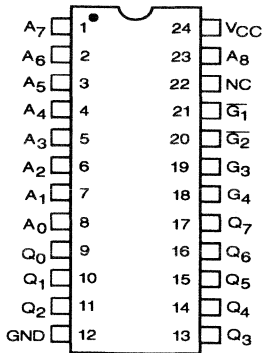
## PRODUCT SELECTOR GUIDE

Part Number	Am27S31A		Am27S31	
	35 ns	45 ns	55 ns	70 ns
Address Access Time	35 ns	45 ns	55 ns	70 ns
Operating Range	C	M	C	M

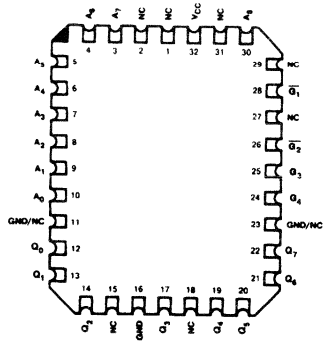
## CONNECTION DIAGRAMS Top View

DIPs\*

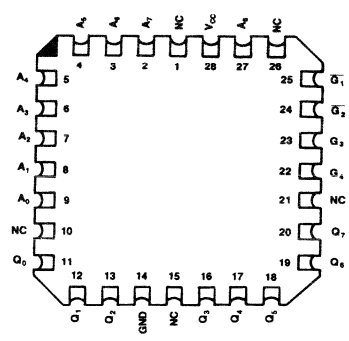
LCCs\*\*



CD000701



CD000711



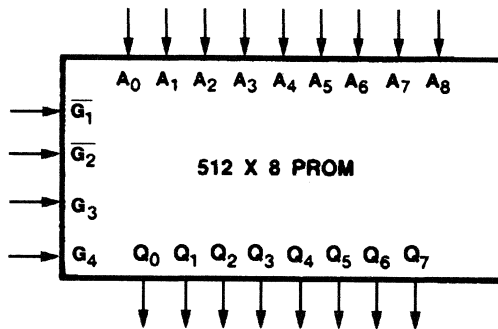
CD009461

\*Also available in a 24-Pin Flatpack. Pinout identical to DIPs.

\*\*Also available in a 28-Pin Square PLCC. Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



LS000151

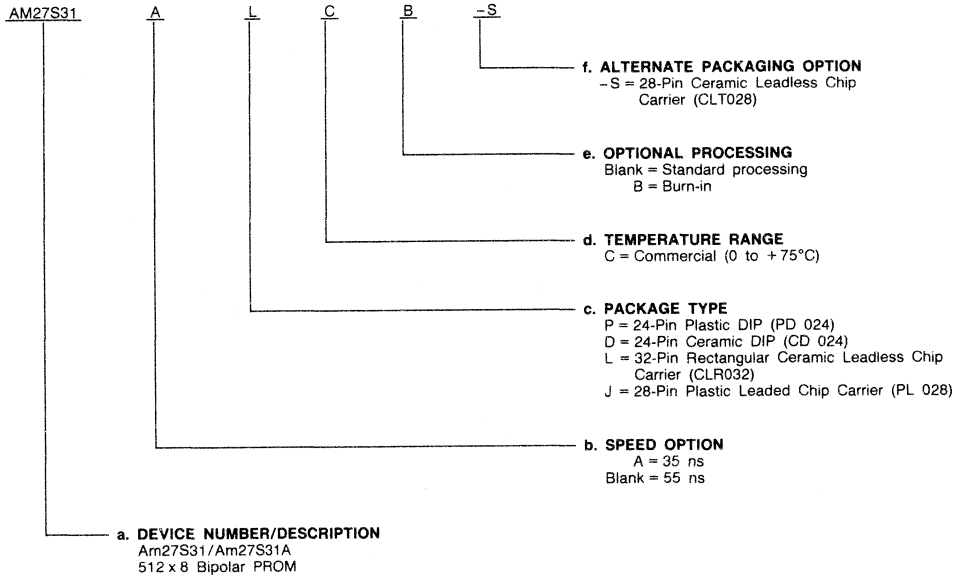
VCC/ = Power Supply  
GND/ = Ground

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing
- f. Alternate Packaging Option



Valid Combinations	
AM27S31	PC, PCB, DC, DCB, LC, LC-S, LCB, LCB-S, JC, JCB
AM27S31A	

#### Valid Combinations

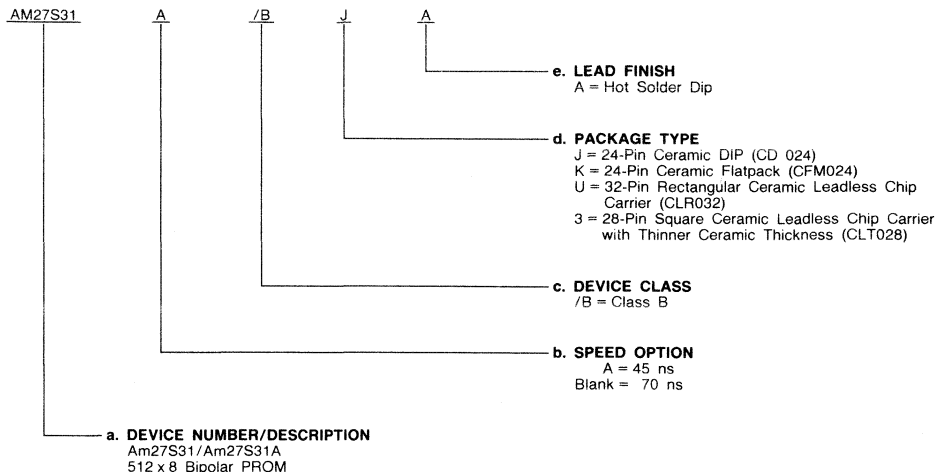
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM27S31	/BJA, /BKA, /BUA, /B3A
AM27S31A	

### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>8</sub> Address Inputs

The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

### Q<sub>0</sub> - Q<sub>7</sub> Data Output Port

The Outputs whose state represents the data read from the selected memory locations.

### $\overline{G}_1$ , $\overline{G}_2$ , G<sub>3</sub>, G<sub>4</sub> Output Enable

Provides direct control of the Q-output buffers. Outputs disabled forces all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G}_1 \cdot \overline{G}_2 \cdot G_3 \cdot G_4$$

$$\begin{aligned} \text{Disable} &= \overline{G}_1 \cdot \overline{G}_2 \cdot G_3 \cdot G_4 \\ &= G_1 + G_2 + \overline{G}_3 + \overline{G}_4 \end{aligned}$$

### V<sub>CC</sub> Device Power Supply Pin

The most positive of the logic power supply pins.

### GND Device Power Supply Pin

The most negative of the logic power supply pins.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military Product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub> (Note 1)	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7 V			25	μA
I <sub>SC</sub> (Note 1)	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 3)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND V <sub>CC</sub> = Max.			175	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>I</sub> = 2.4 V (Note 1)			40	μA
					40	
					-40	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		4		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		8		

Notes: 1. This applies to three-state devices only.

2. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.



**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

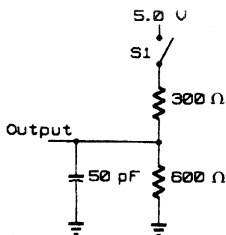
No.	Parameter Symbol	Parameter Description	Am27S31A				Am27S31				Unit
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		35		45		55		70	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		25		30	ns

See also Switching Test Circuits.

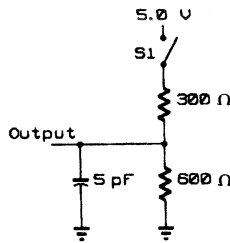
- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.  
 2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.

\*Subgroups 7 and 8 apply to functional tests.

**SWITCHING TEST CIRCUITS**



TC003442



TC003452

**A. Output Load for all A - C tests except TGVQZ**

**B. Output Load for TGVQZ**

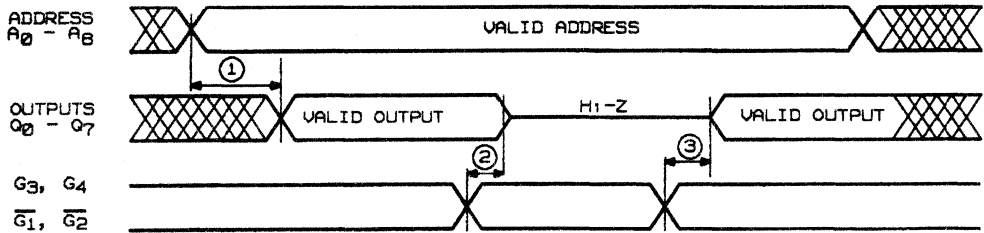
- Notes: 1. All device test loads should be located within 2" of device output pin.  
 2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests.  
 S<sub>1</sub> is closed for all other AC tests.  
 3. Load capacitance includes all stray and fixture capacitance.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF021260

# Am27S33/27S33A

4,096-Bit (1024x4) Bipolar PROM

## DISTINCTIVE CHARACTERISTICS

- High speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

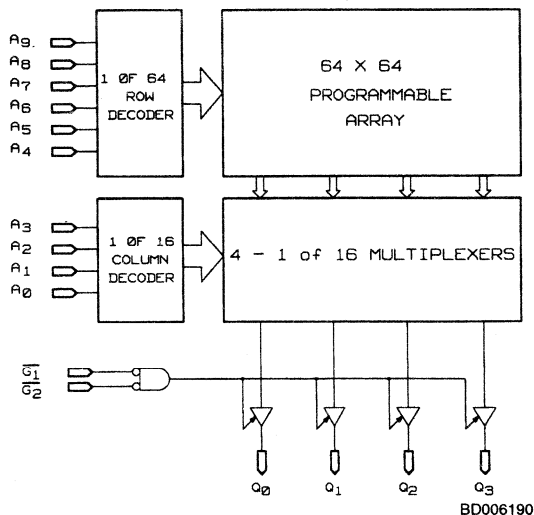
## GENERAL DESCRIPTION

The Am27S33 (1024 words by 4 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in three-state (Am27S33) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the require-

ments of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by active LOW ( $\overline{G}_1$  &  $\overline{G}_2$ ) output enables.

## BLOCK DIAGRAM

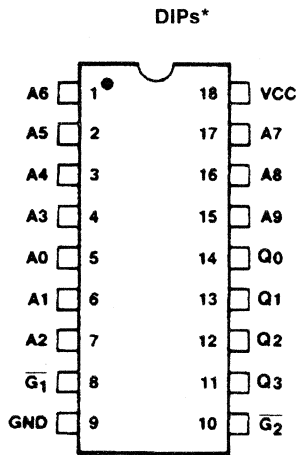


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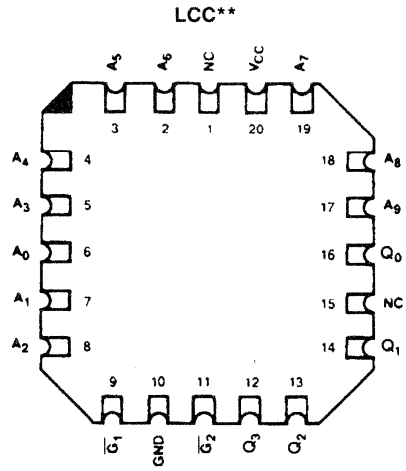
## PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S33A		Am27S33	
	35 ns	45 ns	55 ns	70 ns
Operating Range	C	M	C	M

**CONNECTION DIAGRAMS**  
Top View



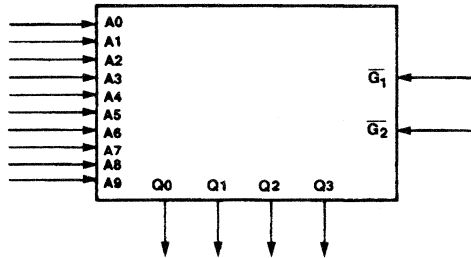
CD000721



CD000731

\*Also available in 18-pin Flatpack. Pinout identical to DIPs.  
 \*\*Also available in a 20-pin square PLCC. Pinout identical to LCC.  
 Note: Pin 1 is marked for orientation.

**LOGIC SYMBOL**



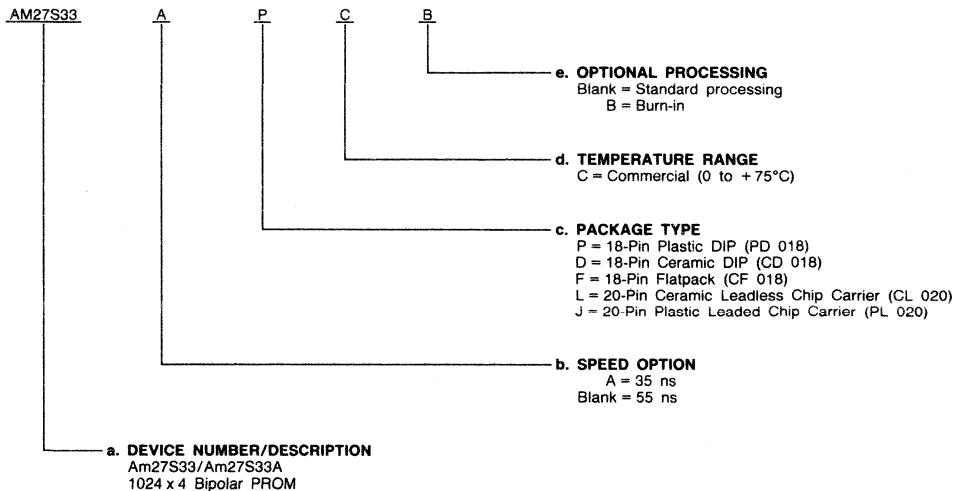
LS002500

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM27S33	PC, PCB, DC, DCB,
AM27S33A	FC, FCB, LC, LCB, JC, JCB

#### Valid Combinations

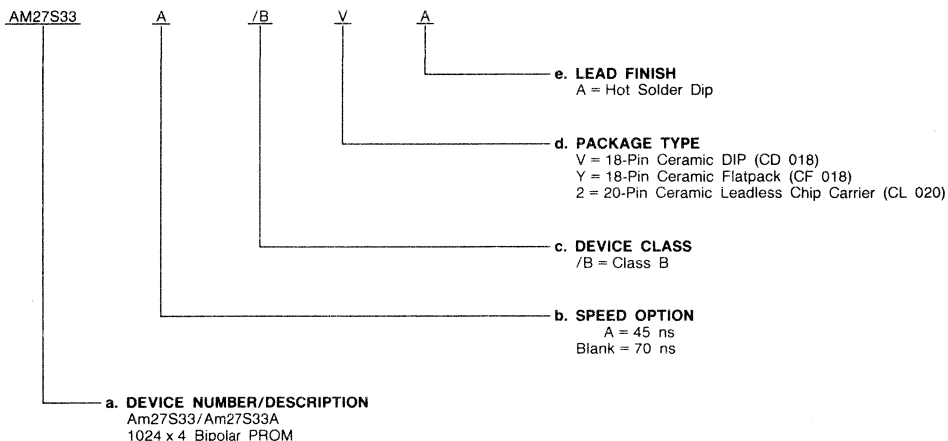
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S33	/BVA, /BYA,
AM27S33A	/B2A

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

## MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>9</sub> Address Inputs

The 10-bit field presented at the address inputs selects one of 1024 memory locations to be read from.

### Q<sub>0</sub> - Q<sub>3</sub> Data Output Port

The outputs whose state represents the data read from the selected memory locations.

### $\overline{G_1}, \overline{G_2}$ Output Enable

Provides direct control of the Q-output buffers. Outputs disabled forces all open-collector outputs to an OFF state

and all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G_1} \cdot \overline{G_2}$$

$$\text{Disable} = \overline{G_1} \cdot \overline{G_2} \\ = G_1 + G_2$$

### VCC Device Power Supply Pin

The most positive of the logic power supply pins.

### GND Device Power Supply Pin

The most negative of the logic power supply pins.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+475 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military Product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.45	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7 V			25	μA
I <sub>SC</sub> (Note 1)	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 2)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND, V <sub>CC</sub> = Max.			140	mA
					145	
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>G1</sub> = 2.4 V			40	μA
		(Note 1)			40	
					-40	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 3) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		5		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 3) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		8		

- Notes: 1. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.  
 3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

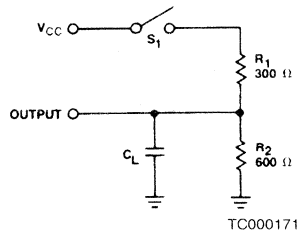
No.	Parameter Symbol	Parameter Description	Am27S33A				Am27S33				Unit
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		35		45		55		70	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		25		30	ns

See also Switching Test Circuit.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.

\*Subgroups 7 and 8 apply to functional tests.

## SWITCHING TEST CIRCUIT



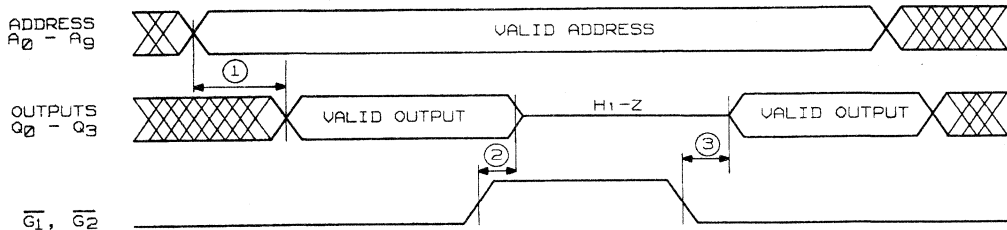
- Notes: 1. TAVQV is tested with switch  $S_1$  closed and  $C_L = 50$  pF.  
 2. For three-state outputs, TGVQV is tested with  $C_L = 50$  pF to the 1.5 V level;  $S_1$  is open for high impedance to HIGH tests and closed for high impedance to LOW tests. TGVQZ is tested with  $C_L = 5$  pF. HIGH to high-impedance tests are made with  $S_1$  open to an output voltage of steady state HIGH  $-0.5$  V; LOW to high-impedance tests are made with  $S_1$  closed to the steady state LOW  $+0.5$  V level.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010





# Am27S35/S35A/Am27S37/S37A

8,192-Bit (1024x8) Bipolar Registered PROM  
with Programmable INITIALIZE Input



## DISTINCTIVE CHARACTERISTICS

- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Versatile programmable asynchronous or synchronous enable for simplified word expansion
- Buffered common INITIALIZE input either asynchronous (Am27S35) or synchronous (Am27S37)
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%)

## GENERAL DESCRIPTION

The Am27S35 and the Am27S37 (1024 words by 8 bits) are fully decoded, Schottky array, TTL Programmable Read-Only Memories (PROMs), incorporating D-type master-slave data registers on chip. These devices have three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

These devices contain an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control

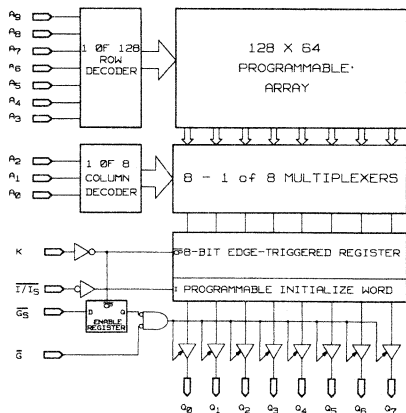
stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, these devices contain both asynchronous ( $\bar{G}$ ) and synchronous ( $\bar{G}_S$ ) output enables.

These devices contain a single pin initialize function capable of loading any arbitrary microinstruction for system interrupt or initialization. On the Am27S35 this function operates asynchronously, independent of clock. The Am27S37 provides synchronous operation of this function.

Upon power-up the outputs ( $Q_0 - Q_7$ ) will be in a floating or high-impedance state.

## BLOCK DIAGRAM



BD006352

5

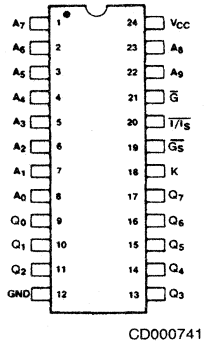
## PRODUCT SELECTOR GUIDE

Part Number Asynchronous Initialize	Am27S35A		Am27S35	
Part Number Synchronous Initialize	Am27S37A		Am27S37	
Address Setup Time	35 ns	40 ns	40 ns	45 ns
Clock-to-Output Delay	20 ns	25 ns	25 ns	30 ns
Operating Range	C	M	C	M

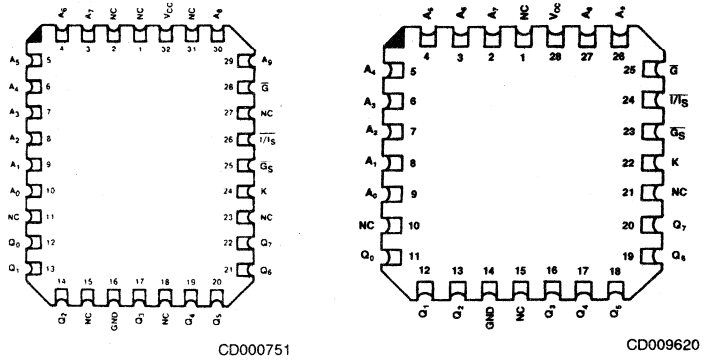
Publication # 03187 Rev. D Amendment /0  
Issue Date: January 1989

## CONNECTION DIAGRAMS Top View

**DIPs\*\***



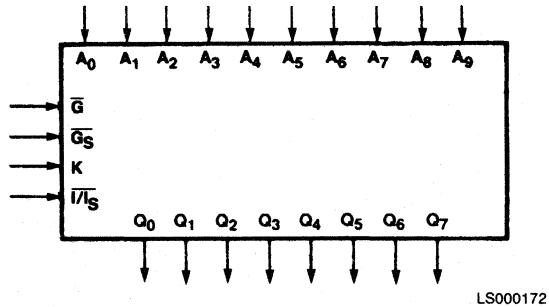
**LCCs\*\***



\*Also available in a 24-pin Flatpack. Pinout identical to DIPs.  
 \*\*Also available in a 28-pin Square PLCC. Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL

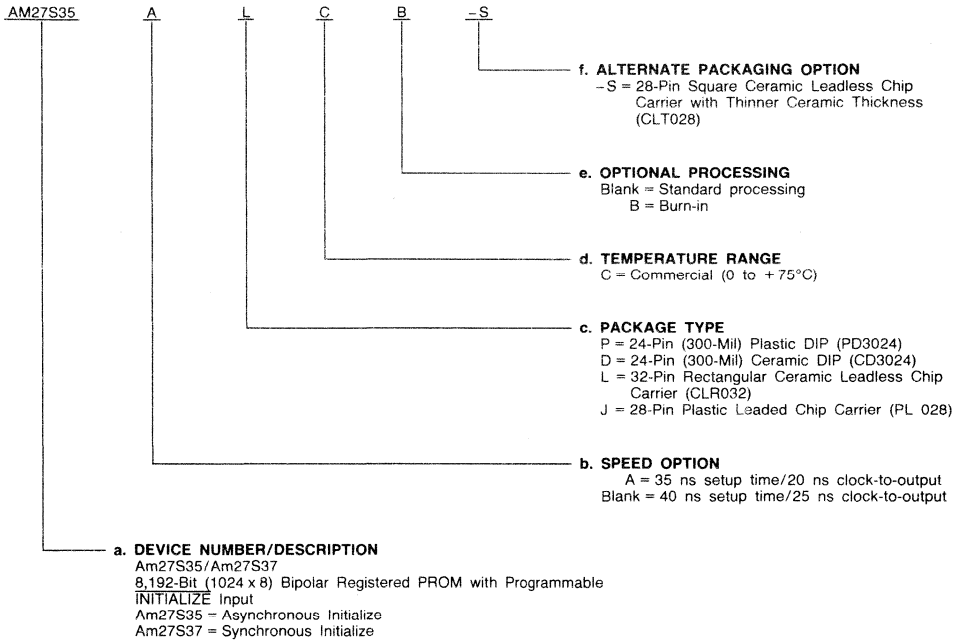


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**
- f. **Alternate Packaging Option**



Valid Combinations	
AM27S35	
AM27S35A	DC, DCB, PC, PCB,
AM27S37	LC, LCB, LC-S, LCB-S,
AM27S37A	JC, JCB

#### Valid Combinations

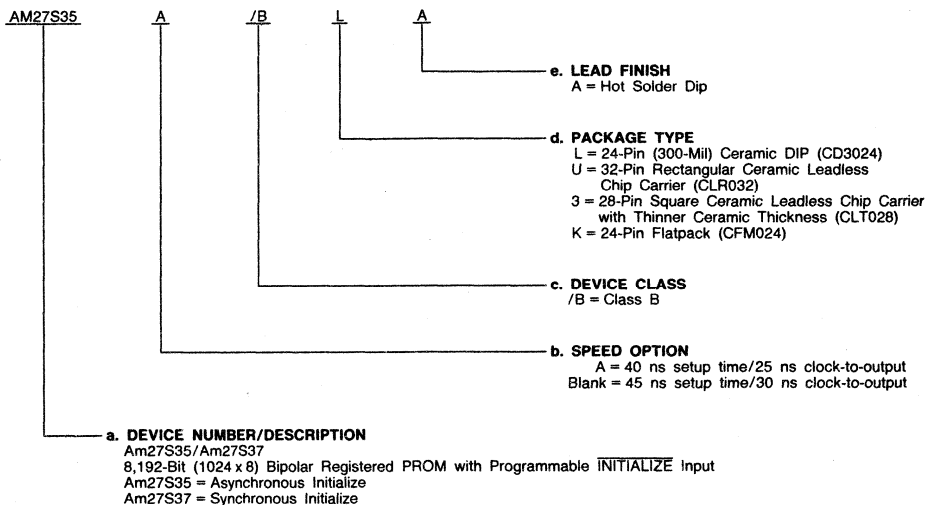
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S35	
AM27S35A	/BLA, /BKA
AM27S37	/BUA, /B3A
AM27S37A	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups  
 1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## PIN DESCRIPTION

### **A<sub>0</sub>–A<sub>9</sub> Address Inputs**

The 10-bit field presented at the address inputs selects one of 1024 memory locations to be read from.

### **K Clock**

The clock is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

### **Q<sub>0</sub>–Q<sub>7</sub> Data Output Port**

Parallel data output from the pipeline register. The disabled state of these outputs is floating or high impedance.

### **$\bar{G}$ Asynchronous Output Enable**

Provides direct control of the Q-output, three-state drivers independent of K.

### **$\bar{G}_S$ Synchronous Output Enable**

Controls the state of the Q-output, three-state drivers in conjunction with K. This is useful where more than one registered PROM is bussed together for word-depth

expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

### **$\bar{I}$ Asynchronous Initialize (Am27S35)**

Control pin used to initialize the output data registers from a programmable word independent of K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

### **$\bar{I}_S$ Synchronous Initialize (Am27S37)**

Control pin used to initialize the output data registers from a programmable word in conjunction with K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

### **V<sub>CC</sub> Device Power Supply Pin**

The most positive of the logic power supply pins.

### **GND Device Power Supply Pin**

The most negative of the logic power supply pins.

## FUNCTIONAL DESCRIPTION

The Am27S35A/35 and Am27S37A/37 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 1024-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S35A/35 and Am27S37A/37 also offer maximum flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V<sub>CC</sub> power is first applied, the synchronous enable ( $\bar{G}_S$ ) flip-flop will be in the set condition causing the outputs (Q<sub>0</sub>–Q<sub>7</sub>) to be in the OFF or high-impedance state. This occurs regardless of the state of the asynchronous enable input. A LOW-to-HIGH transition of the clock input (K) while  $\bar{G}_S$  input is low is required after power-up in order to enable the outputs to an active state. Reading data is accomplished by first applying the binary word address to the address inputs (A<sub>0</sub>–A<sub>9</sub>) and a logic LOW to the synchronous enable ( $\bar{G}_S$ ). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (K), data is transferred to the slave flip-flops which drive the output buffers. Provided that the asynchronous enable ( $\bar{G}$ ) is also LOW, stored data will appear on the outputs (Q<sub>0</sub>–Q<sub>7</sub>). If ( $\bar{G}_S$ ) is HIGH when the positive clock edge occurs, outputs go to the OFF or high-impedance state regardless of the value of ( $\bar{G}$ ). The outputs may be disabled at any time by switching ( $\bar{G}$ ) to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge

occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

These devices also contain a built-in initialize function. When activated, the initialize control input ( $\bar{I}$ ) causes the contents of an additional (1025th) 8-bit word to be loaded into the on-chip register. This extra word is user programmable. Since each bit is individually programmable, the initialize function can be used to load any desired combination of HIGHs and LOWs into the register. In the unprogrammed state, activating  $\bar{I}$  will perform a register CLEAR (all outputs LOW). If all bits of the initialize word are programmed, activating  $\bar{I}$  performs a register PRESET (all outputs HIGH).

This ability to tailor the initialize outputs to the system requirements simplifies system design and enhances performance. The initialize function is useful during power-up and timeout sequences. This flexible feature can also facilitate implementation of other sophisticated functions such as a built-in "jump-start" address.

The Am27S35A/35 has an asynchronous initialize input ( $\bar{I}$ ). Applying a LOW to the  $\bar{I}$  input causes an immediate load of the programmed initialize word into the slave flip-flops of the register independent of all other inputs (including K). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ( $\bar{G}$ ) LOW.

The Am27S37A/37 has a synchronous  $\bar{I}_S$  input. Applying a LOW to the  $\bar{I}_S$  input causes an immediate load of the programmed initialize word into the master flip-flops of the register only independent of all other inputs (including K). To bring this data to the device outputs, the synchronous enable ( $\bar{G}_S$ ) should be held LOW until the next LOW-to-HIGH transition of the clock (K). Following this, the data will appear on the outputs after the asynchronous enable ( $\bar{G}$ ) is brought LOW.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>			40	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 2)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND, V <sub>CC</sub> = Max.			185	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>S</sub> = 2.4 V			40	μA
		V <sub>O</sub> = V <sub>CC</sub> V <sub>O</sub> = 0.4 V			-40	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 3) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		5		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 3) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		12		

- Notes: 1. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 2. Only one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.  
 3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (For APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*) (Note 1)

No.	Parameter Symbol	Parameter Description	Am27S35A/ Am27S37A		Am27S35/ Am27S37		Unit
			Min.	Max.	Min.	Max.	
1	TAVKH	Address to K HIGH Setup Time	COM'L	35		40	ns
			MIL	40		45	
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0	ns
			MIL	0		0	
3	TKHQV <sub>1</sub>	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW)	COM'L		20	25	ns
			MIL		25	30	
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	20		20	ns
			MIL	20		20	
5	TGLOV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (See Note 3)	COM'L		25	30	ns
			MIL		30	35	
6	TGHQZ	Asynchronous Output Enable HIGH to Output Hi-Z (See Notes 2 & 3)	COM'L		25	30	ns
			MIL		30	35	
7	TGSVKH	$\overline{G}_S$ to K HIGH Setup Time (See Note 4)	COM'L	15		15	ns
			MIL	15		15	
8	TKHGSX	$\overline{G}_S$ to K HIGH Hold Time (See Note 4)	COM'L	5		5	ns
			MIL	5		5	
9	TKHQV <sub>2</sub>	Delay from K HIGH to Output Valid, for initially Hi-Z outputs (See Note 4)	COM'L		25	30	ns
			MIL		30	35	
10	TKHQZ	Delay from K HIGH to Output Hi-Z (See Notes 2 & 4)	COM'L		25	30	ns
			MIL		30	35	
11	TILQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (See Note 5)	COM'L		30	35	ns
			MIL		35	40	
12	TIHKH	Asynchronous $\overline{I}$ Recovery Time (See Note 5)	COM'L	20		20	ns
			MIL	20		25	
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (See Note 5)	COM'L	25		25	ns
			MIL	30		30	
14	TISVKH	$\overline{I}_S$ to K HIGH Setup Time (See Note 6)	COM'L	25		30	ns
			MIL	30		35	
15	TKHISX	$\overline{I}_S$ to K HIGH Hold Time (See Note 6)	COM'L	0		0	ns
			MIL	0		0	

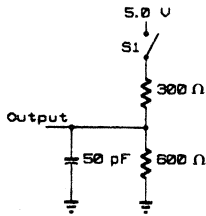
See also Switching Test Circuits.

- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.  
 2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.  
 3. Applies only when Asynchronous Enable ( $\overline{G}$ ) function is used.  
 4. Applies only when Synchronous Enable ( $\overline{G}_S$ ) function is used.  
 5. Applies only to the Am27S35 (Asynchronous Initialize ( $\overline{I}$ )) version.  
 6. Applies only to the Am27S37 (Synchronous Initialize ( $\overline{I}_S$ )) version.

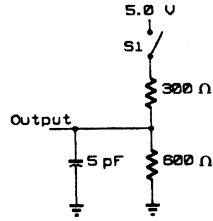
\*Subgroups 7 and 8 apply to functional tests.



## SWITCHING TEST CIRCUITS



TC003442



TC003452

### A. Output Load for All AC Tests Except TGHQZ and TKHQZ

### B. Output Load for TGHQZ and TKHQZ

- Notes:
1. All device test loads should be located within 2" of device output pin.
  2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S<sub>1</sub> is closed for all other AC tests.
  3. Load capacitance includes all stray and fixture capacitance.

## SWITCHING WAVEFORMS

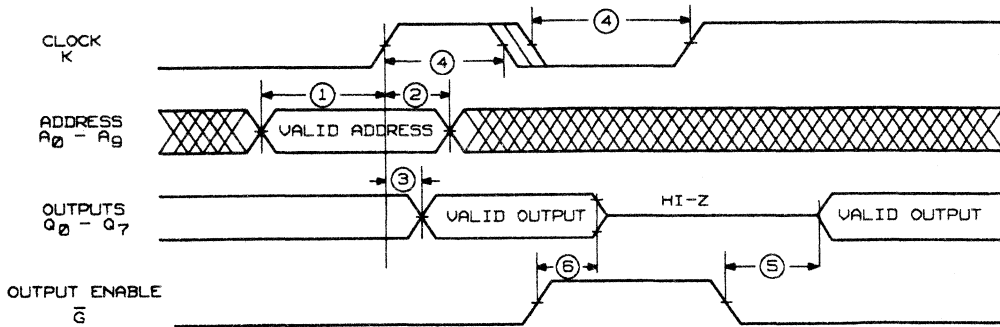
### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE. ANY CHANGE PERMITTED	CHANGING. STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

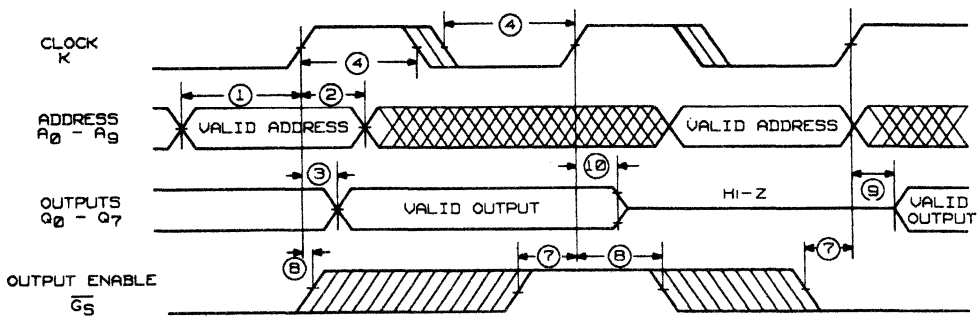


SWITCHING WAVEFORMS (Cont'd.)



WF021580

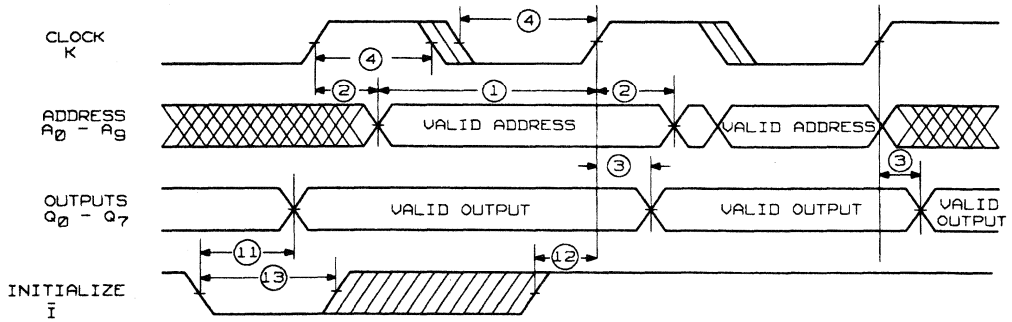
Timing Set 1. Using Asynchronous Enable



WF021611

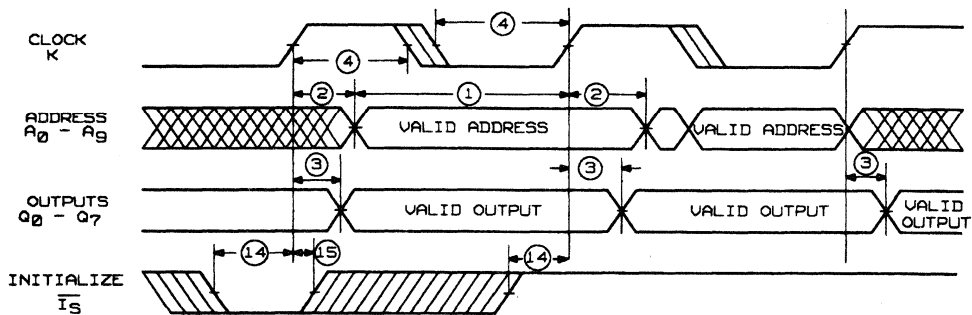
Timing Set 2. Using Synchronous Enable

SWITCHING WAVEFORMS (Cont'd.)



WF021590

Timing Set 3. Using Asynchronous Initialize  
Am27S35 Only



WF021601

Timing Set 4. Using Synchronous Initialize  
Am27S37 Only



# Am27S41/27S41A/27PS41

16,384-Bit (4,096x4) Bipolar PROM

## DISTINCTIVE CHARACTERISTICS

- Ultra-fast access time "A" version (35 ns Max.)
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

## GENERAL DESCRIPTION

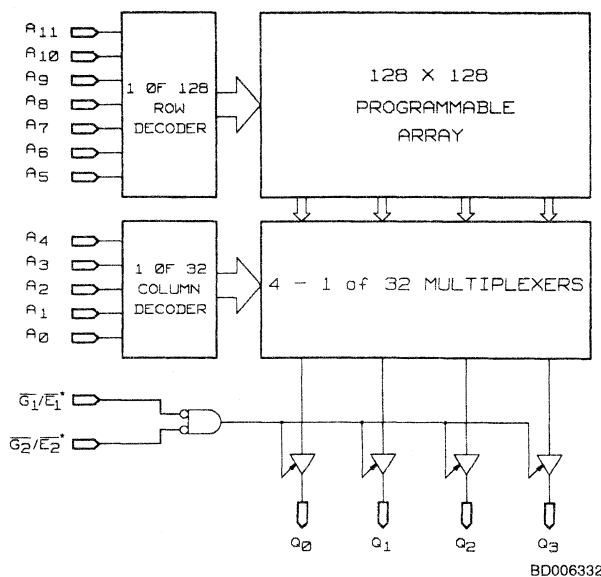
The Am27S41 (4,096 words by 4 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls,

mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by active LOW ( $\overline{G}_1$  &  $\overline{G}_2$ ) output enables.

As an APL product, this device is also offered in a power-switched version, the Am27PS41.

## BLOCK DIAGRAM

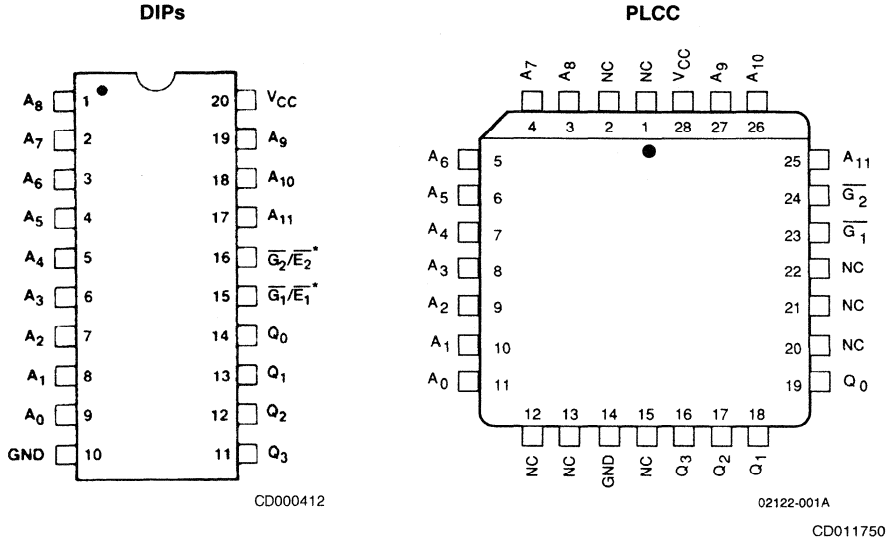


\*E nomenclature applies only to Am27PS power-switched version.

## PRODUCT SELECTOR GUIDE

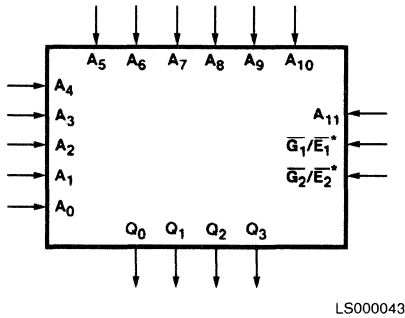
Part Number	Am27S41A		Am27S41		Am27PS41
Address Access Time	35 ns	50 ns	50 ns	65 ns	65 ns
Operating Range	C	M	C	M	M

**CONNECTION DIAGRAMS**  
**Top View**



Note: Pin 1 is marked for orientation.

**LOGIC SYMBOL**



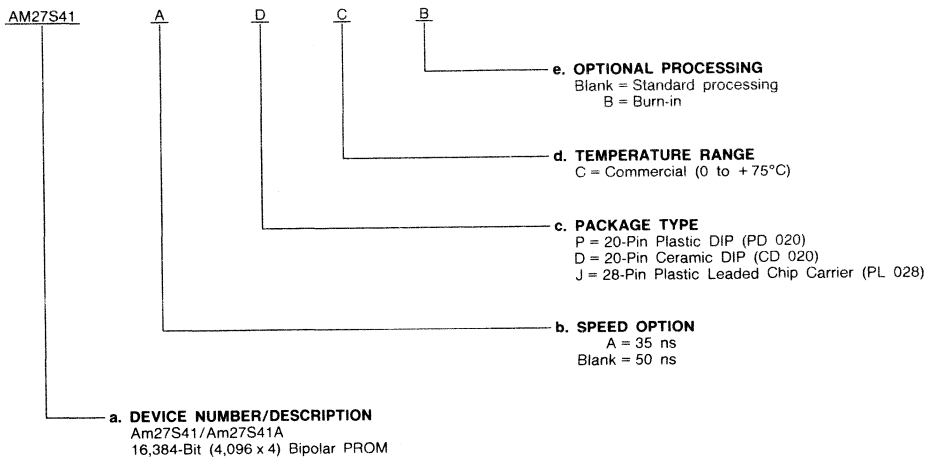
\*E nomenclature applies only to Am27PS power-switched version.

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM27S41	PC, PCB, DC, DCB,
AM27S41A	JC, JCB

### Valid Combinations

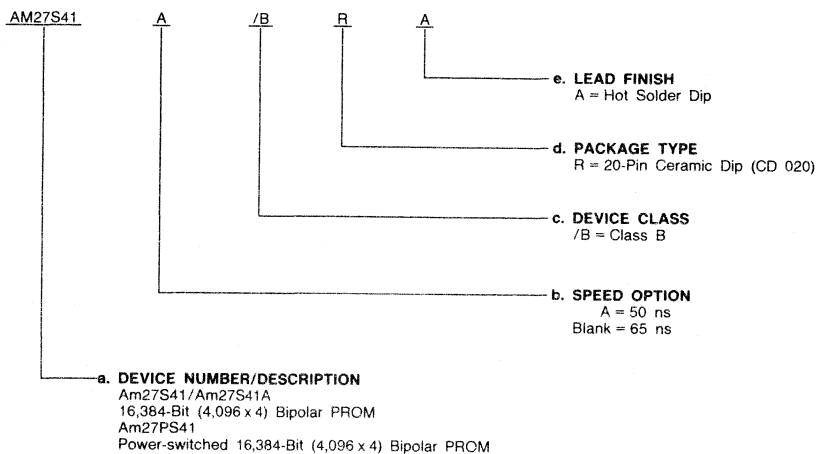
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S41	/BRA
AM27S41A	
AM27PS41	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
 1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

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## PIN DESCRIPTION

### **A<sub>0</sub> – A<sub>11</sub> Address Inputs**

The 12-bit field presented at the address inputs selects one of 4,096 memory locations to be read from.

### **Q<sub>0</sub> – Q<sub>3</sub> Data Output Port**

The outputs whose state represents the data read from the selected memory locations.

### **$\overline{G}_1, \overline{G}_2$ Output Enable**

Provides direct control of the Q-output, three-state buffers. Outputs disabled forces all outputs to a floating or high-

impedance state. On power-switched version, the disabled state reduces the I<sub>CC</sub> to I<sub>CCD</sub>.

$$\text{Enable} = \overline{G}_1 \cdot \overline{G}_2$$

$$\begin{aligned} \text{Disable} &= \overline{G}_1 \cdot \overline{G}_2 \\ &= G_1 \cdot G_2 \end{aligned}$$

### **V<sub>CC</sub> Device Power Supply Pin**

The most positive of the logic power supply pins.

### **GND Device Power Supply Pin**

The most negative of the logic power supply pins.

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## FUNCTIONAL DESCRIPTION

### Power Switching

The Am27PS41 is a power-switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I<sub>CC</sub> is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS41 is selected by a low level on  $\overline{E}_1$ , a current surge is placed on the V<sub>CC</sub> supply due to the power-up feature in order to minimize the effects of this current transient, it is recommended that a 0.1 μf ceramic capacitor be connected from pin 20 to pin 10 at each device. (See Figure 1.)
2. Address access time (TAVQ1) can be optimized if a chip enable set-up time (TEVAV) of greater than 25 ns is observed. Negative set-up times on chip enable (TEVAV < 0) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to + 5.5 V
DC Input Current .....	-30 mA to +5 mA

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military Products 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	COM'L		0.45	V
			MIL		0.50	
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>			40	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 1)	COM'L	-20	-90	mA
			MIL	-15	-90	
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = Max. All inputs = 0.0 V	COM'L		165	mA
			MIL		170	
I <sub>CCD</sub> *	Am27PS Version Power Down Supply Current	V <sub>CC</sub> = Max V <sub>E1</sub> = 2.4 V, All other inputs = 0.0 V			85	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>GT</sub> = 2.4 V	V <sub>O</sub> = V <sub>CC</sub>		40	μA
			V <sub>O</sub> = 0.4 V		-40	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 2) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		5.0		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 2) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		8.0		

- Notes: 1. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.  
 2. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.  
 3. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 \* For Am27PS41, APL only.

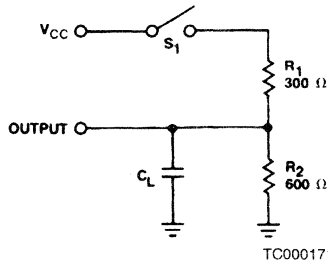
**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

No.	Parameter Symbol	Parameter Description	Version	27S Version		27PS Version		Unit
				COM'L		MIL		
				Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time	A	35	50			ns
			STD	50	65	65		
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	A	25	30			ns
			STD	25	30	30		
3	TGVQV	Delay from Output Enable Valid to Output Valid	A	25	30			ns
			STD	25	30	85		
4	TAVQV1	Power Switched Address Valid to Output Valid Access Time (Am27PS Versions only)	A					ns
			STD				85	

- See also Switching Test Circuit.  
 Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.  
 \*Subgroups 7 and 8 apply to functional tests.



## SWITCHING TEST CIRCUIT



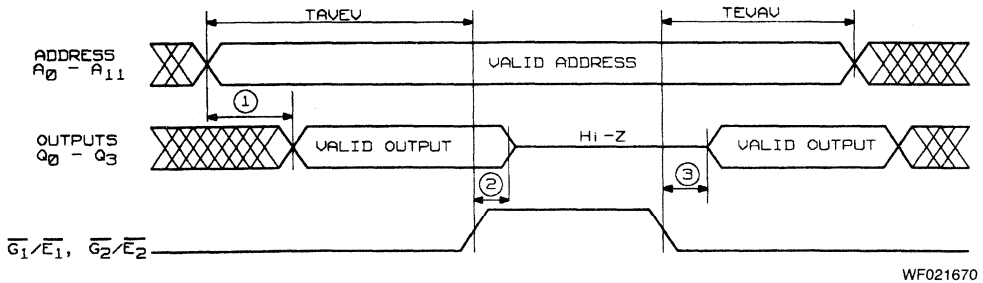
- Notes: 1. TAVQV is tested with switch  $S_1$  closed and  $C_L = 50$  pF. TEVAV is defined as chip enable setup time.  
 2. For the three-state output, TGVQV is tested with  $C_L = 50$  pF to the 1.5 V level;  $S_1$  is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGVQZ is tested with  $C_L = 5$  pF. HIGH to high-impedance tests are made with  $S_1$  open to an output voltage of steady state HIGH - 0.5 V; LOW to high-impedance tests are made with  $S_1$  closed to the steady state LOW + 0.5 V level.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010





# Am27S43/27S43A

32,768-Bit (4096x8) Bipolar PROM

## DISTINCTIVE CHARACTERISTICS

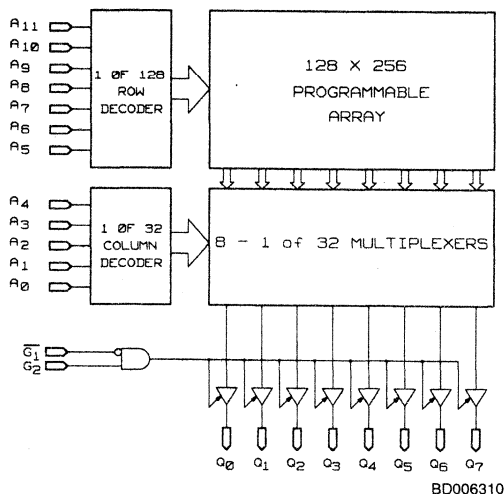
- Ultra-fast access time
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)

## GENERAL DESCRIPTION

The Am27S43 (4096 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls.

## BLOCK DIAGRAM



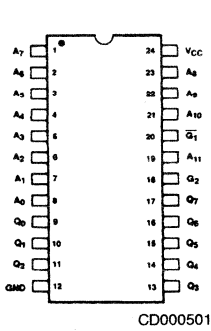
## PRODUCT SELECTOR GUIDE

Part Number	Am27S43A		Am27S43	
	Address Access Time	40 ns	55 ns	55 ns
Operating Range	C	M	C	M

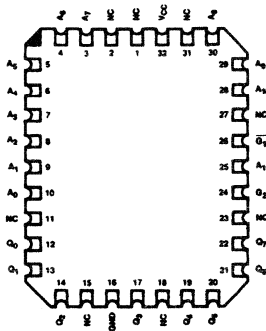
## CONNECTION DIAGRAMS Top View

DIPs\*

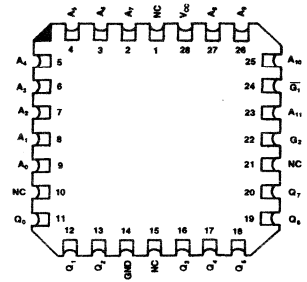
LCCs



CD000501



CD000511

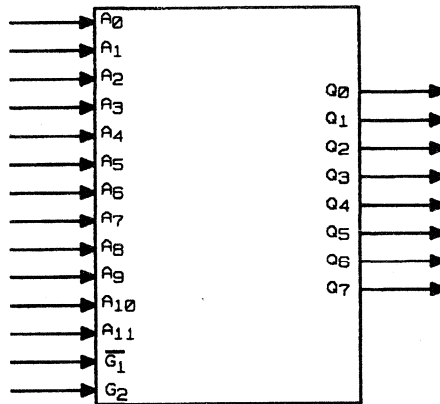


CD009490

\*Also available in 24-Pin Flatpack. Pinout identical to DIPs.

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



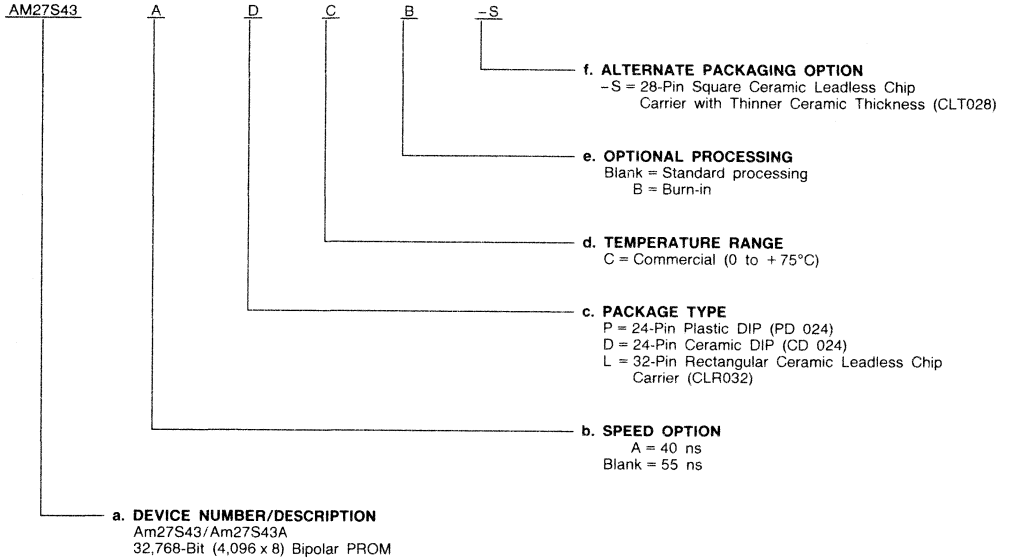
LS002401

# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**
- f. **Alternate Packaging Option**



Valid Combinations	
AM27S43	DC, DCB, PC, PCB, LC, LCB
AM27S43A	LC-S, LCB-S

### Valid Combinations

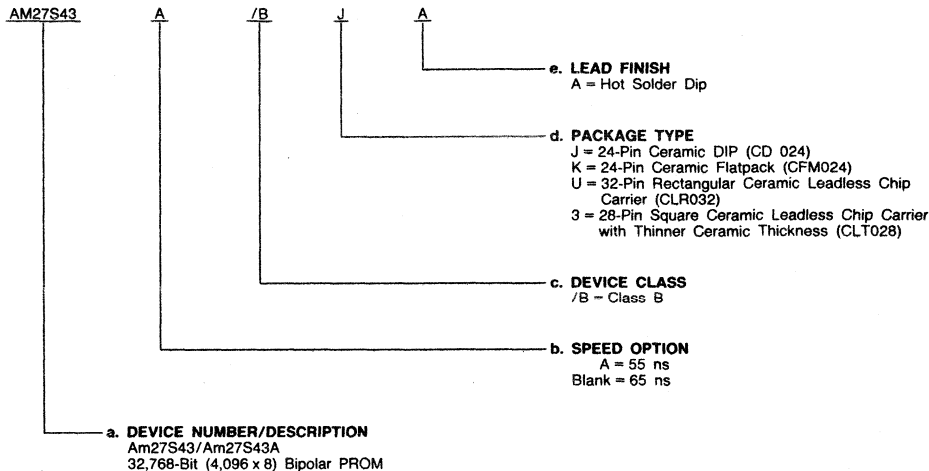
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM27S43	/BJA, /BKA,
AM27S43A	/BUA, /B3A

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>11</sub> Address (Inputs)

The 12-bit field presented at the address inputs selects one of 4,096 memory locations to be read from.

### Q<sub>0</sub> - Q<sub>7</sub> Data Output Port

The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which when disabled are in a floating or high-impedance state.

### $\overline{G}_1, \overline{G}_2$ Output Enable (Input)

Provides direct control of the Q-output, three-state buffers. Outputs disabled forces all outputs to to a floating or high-impedance state.

$$\text{Enable} = \overline{G}_1 \cdot G_2$$

$$\text{Disable} = \overline{G}_1 \cdot \overline{G}_2 \\ = G_1 \cdot G_2$$

### V<sub>CC</sub> Device Power Supply Pin

The most positive of the logic power supply pins.

### GND Device Power Supply Pin

The most negative of the logic power supply pins.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military Product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>			40	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 2)	-15		-100	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND, V <sub>CC</sub> = Max.			185	mA
		COM'L			185	
		MIL			185	
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max., V <sub>G1</sub> = 2.4 V			40	μA
		V <sub>O</sub> = V <sub>CC</sub>			-40	
		V <sub>O</sub> = 0.4 V			-40	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 3) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		5.0		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 3) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		8.0		

- Notes: 1. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.  
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

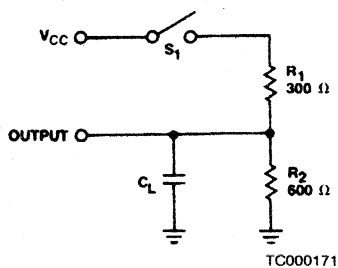
**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

No.	Parameter Symbol	Parameter Description	Am27S43A				Am27S43				Unit
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		40		55		55		65	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		30		35		35		40	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		30		35		35		40	ns

- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.  
2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels.

\*Subgroups 7 and 8 apply to functional tests.

## SWITCHING TEST CIRCUIT



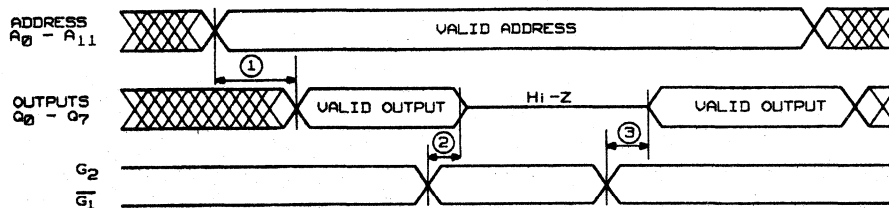
- Notes: 1. TAVQV is tested with Switch  $S_1$  closed and  $C_L = 30$  pF.  
 2. For three-state outputs, TGQVQ is tested with  $C_L = 30$  pF to the 1.5 V level;  $S_1$  is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGQVZ is tested with  $C_L = 5$  pF. HIGH to high-impedance tests are made with  $S_1$  open to an output voltage of  $V_{OH} - 0.5$  V; LOW to high-impedance tests are made with  $S_1$  closed to the  $V_{OL} + 0.5$  V level.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



# Am27S45/27S45A/27S45SA

# Am27S47/27S47A/27S47SA

16,384-Bit (2048x8) Bipolar Registered PROM  
with Programmable INITIALIZE Input



## DISTINCTIVE CHARACTERISTICS

- "SA" version offers superior performance with 25 ns setup time and 10 ns clock-to-output delay
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Versatile programmable asynchronous or synchronous enable for simplified word expansion
- Buffered common INITIALIZE input either asynchronous (Am27S45) or synchronous (Am27S47)
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%)

## GENERAL DESCRIPTION

The Am27S45 and the Am27S47 (2048-words by 8-bits) are fully decoded, Schottky array, TTL Programmable Read-Only Memories (PROMs), incorporating D-type master-slave data registers on chip. These devices have three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

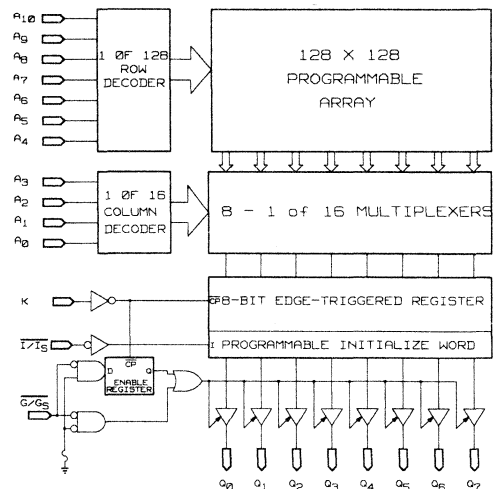
These devices contain an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To Offer the system designer maximum flexibility, these devices contain a user programmable asynchronous or synchronous output enable. The unprogrammed state of the enable pin operates as an Asynchronous Enable ( $\overline{G}$ ) input. An architecture word permits the programming of the functionality of this pin to Synchronous Enable ( $\overline{G_S}$ ).

These devices contain a single pin initialize function capable of loading any arbitrary microinstruction for system interrupt or initialization. On the Am27S45 this function operates asynchronously, independent of clock. The Am27S47 provides synchronous operation of this function.

If the architecture has been programmed to synchronous enable, upon power-up the outputs ( $Q_0 - Q_7$ ) will be in a floating or high-impedance state.

## BLOCK DIAGRAM



BD006381

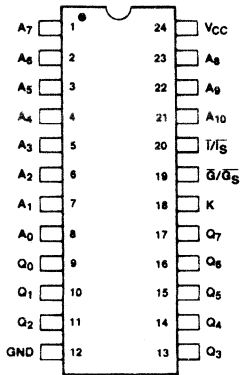


## PRODUCT SELECTOR GUIDE

Part Number Asynchronous Initialize	27S45SA	27S45A	27S45			
Part Number Synchronous Initialize	27S47SA	27S47A	27S47			
Address Setup Time (ns)	25	28	40	45	45	50
Clock-to-Output Delay (ns)	10	12	20	25	25	30
Operating Range	C	M	C	M	C	M

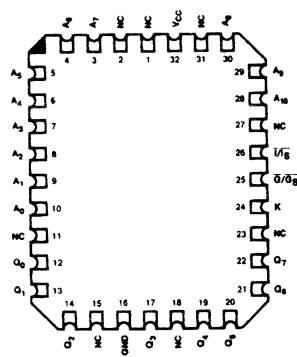
## CONNECTION DIAGRAMS Top View

**DIPs\***

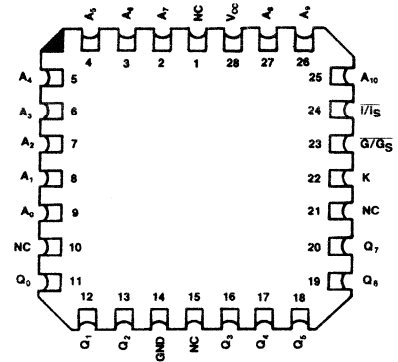


CD000461

**LCCs\*\***



CD000471



CD009630

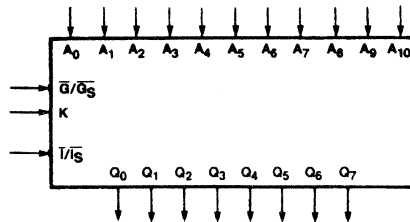
Note: Pin 1 is marked for orientation.

\*Also available in a 24-pin Flatpack. Pinout identical to DIPs.

\*\*Also available in a 28-pin Square Plastic Leaded Chip Carrier. Pinout identical to LCC.



## LOGIC SYMBOL



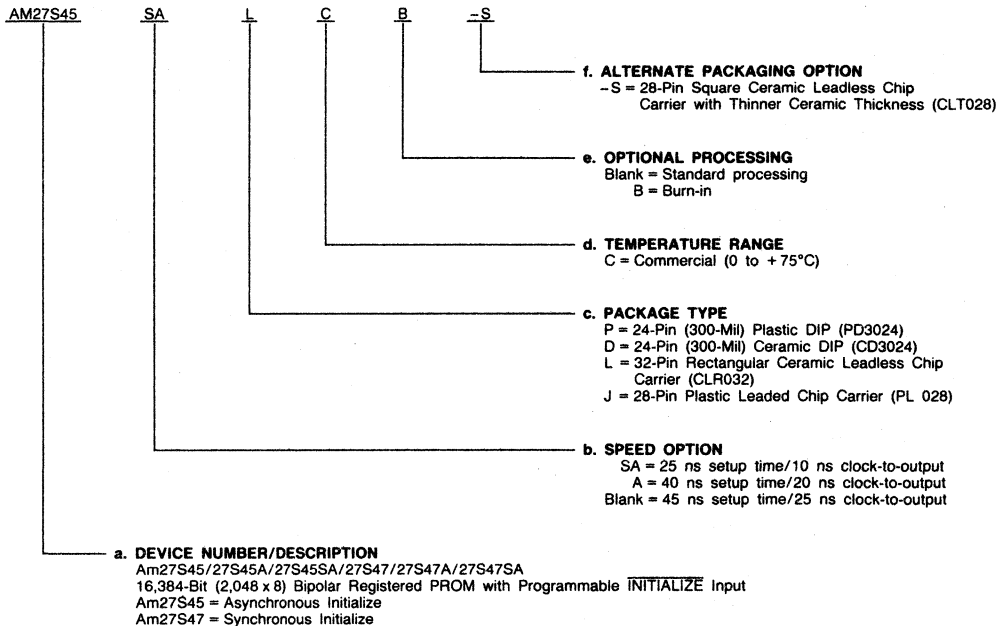
LS000051

# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**
- f. **Alternate Packaging Option**



Valid Combinations	
AM27S45SA	DC, DCB, PC, PCB, LC, LCB, LC-S, LCB-S, JC, JCB
AM27S45A	
AM27S45	
AM27S47SA	
AM27S47A	
AM27S47	

### Valid Combinations

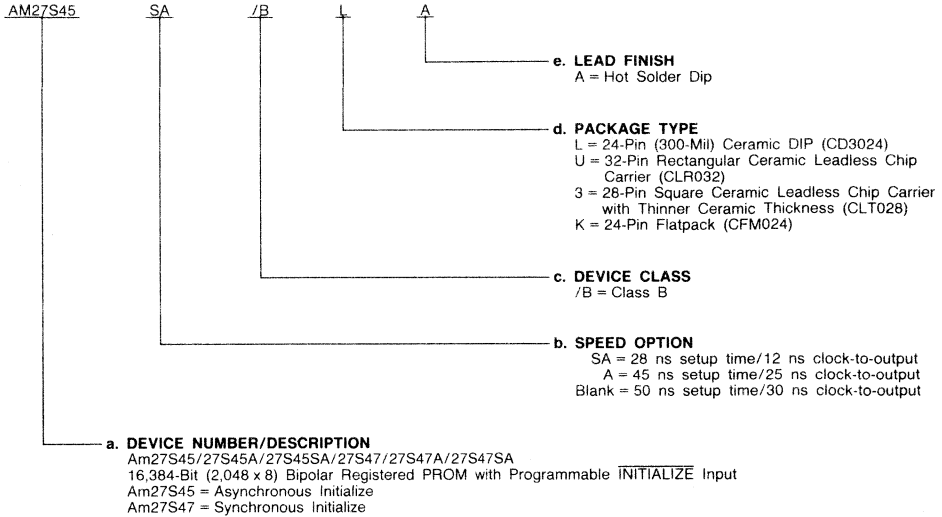
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S45SA	/BLA, /BKA, /BUA, /B3A
AM27S45A	
AM27S45	
AM27S47SA	
AM27S47A	
AM27S47	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.



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## PIN DESCRIPTION

### **A<sub>0</sub> - A<sub>10</sub> Address (Input)**

The 11-bit field presented at the address inputs selects one of 2048 memory locations to be read from.

### **K Clock (Input)**

The clock is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

### **Q<sub>0</sub> - Q<sub>7</sub> Data Output Port**

Parallel data output from the pipeline register. The disabled state of these outputs is floating or high impedance.

### **$\bar{I}$ Asynchronous Initialize (Input) (Am27S45)**

Control pin used to initialize the output data registers from a programmable word independent of K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

### **$\bar{I}_S$ Synchronous Initialize (Input) (Am27S47)**

Control pin used to initialize the output data registers from a programmable word in conjunction with K. This can be used

to generate any arbitrary microinstruction for system interrupt or initialization.

### **V<sub>CC</sub> Device Power Supply Pin**

The most positive of the logic power supply pins.

### **GND Device Power Supply Pin**

The most negative of the logic power supply pins.

This device contains a single-bit architecture word which, according to programming, will provide one of the following functions.

### **$\bar{Q}$ Asynchronous Output Enable (Input)**

Provides direct control of the Q-output, three-state drivers independent of K.

### **$\bar{Q}_S$ Synchronous Output Enable (Input)**

Controls the state of the Q-output, three-state drivers in conjunction with K. This is useful where more than one registered PROM is bussed together for word-depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

## FUNCTIONAL DESCRIPTION

The Am27S45A/45 and Am27S47A/47 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 2048-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S45A/45 and Am27S47A/47 also offer maximum flexibility for system design by providing either synchronous or asynchronous initialize, and synchronous or asynchronous output enable.

When  $V_{CC}$  power is first applied, the state of the outputs will depend on whether the enable has been programmed to be a synchronous or asynchronous enable. If the synchronous enable ( $\overline{G_S}$ ) is being used, the register will be in the set condition causing the outputs ( $Q_0$  to  $Q_7$ ) to be in the OFF or high-impedance state. If the asynchronous enable ( $\overline{G}$ ) is being used, the outputs will come up in the OFF or high-impedance state only if the enable ( $\overline{G}$ ) input is at a logic HIGH level. Reading data is accomplished by first applying the binary word address to the address inputs ( $A_0$  through  $A_{10}$ ) and a logic LOW to the enable input. During the address setup time, the stored data is accessed and loaded into the master flip-flops of the data register. Upon the next LOW-to-HIGH transition of the clock input (K), data is transferred to the slave flip-flops which drive the output buffers, and the accessed data will appear at the outputs ( $Q_0$  through  $Q_7$ ). If the asynchronous enable ( $\overline{G}$ ) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable back to the logic LOW state. For devices using the synchronous enable ( $\overline{G_S}$ ), the outputs will go into the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the next positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change, since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the PROM decoders and

sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from the system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

These devices also contain a built-in initialize function. When activated, the initialize control input ( $\overline{I}$ ) causes the contents of an additional (2049th) 8-bit word to be loaded into the on-chip register. This extra word is user programmable. Since each bit is individually programmable, the initialize function can be used to load any desired combination of HIGHs and LOWs into the register. In the unprogrammed state, activating  $\overline{I}$  will perform a register CLEAR (all outputs LOW). If all bits of the initialize word are programmed, activating  $\overline{I}$  performs a register PRESET (all outputs HIGH).

This ability to tailor the initialize outputs to the system requirements simplifies system design and enhances performance. The initialize function is useful during power up and timeout sequences. This flexible feature can also facilitate implementation of other sophisticated functions such as a built-in "jump-start" address.

The Am27S45A/45 has an asynchronous initialize input ( $\overline{I}$ ). Applying a LOW to the  $\overline{I}$  input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register independent of all other inputs (including K). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ( $\overline{G}$ ) LOW.

The Am27S47A/47 has a synchronous  $\overline{I_S}$  input. Applying a LOW to the  $\overline{I_S}$  input causes an immediate load of the programmed initialize word into the master flip-flops of the register only independent of all other inputs (including K). To bring this data to the outputs of a device with a synchronous enable, the synchronous enable ( $\overline{G_S}$ ) should be held LOW until the next LOW-to-HIGH transition of the clock (K). For a device with an asynchronous enable, the data will appear at the device outputs after the next LOW-to-HIGH clock transition if the enable ( $\overline{G}$ ) is held LOW.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec.) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>			40	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 2)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	Am27S45/Am27S47 Standard & "A" versions V <sub>CC</sub> = Max., All inputs = 0.0 V			185	mA
		Am27S45/Am27S47 "SA" version only	COM'L	T <sub>A</sub> = 0°C	195	
				T <sub>A</sub> = 25°C	190	
				T <sub>A</sub> = 75°C	175	
		MIL	T <sub>C</sub> = -55°C	210		
			T <sub>C</sub> = 25°C	190		
T <sub>C</sub> = 125°C	160					
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>G</sub> = 2.4 V	(Note 3)		40 -40	μA
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5.00 V; T <sub>A</sub> = 25°C		5		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5.00 V; T <sub>A</sub> = 25°C		12		

- Notes: 1. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 2. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.  
 3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.  
 4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.  
 5. I<sub>CC</sub> limits at temperature extremes are guaranteed by correlation to +25°C test limits.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*) (Note 1)

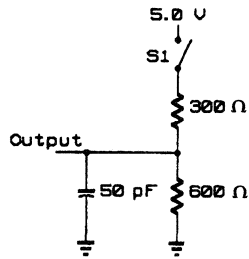
No.	Parameter Symbol	Parameter Description	Am27S45SA/ Am27S47SA		Am27S45A/ Am27S47A		Am27S45/ Am27S47		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVKH	Address to K HIGH Setup Time	COM'L	25		40		45	ns
			MIL	28				50	
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		0	ns
			MIL	0		0		0	
3	TKHQV <sub>1</sub>	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW) (Note 7)	COM'L	4	10		20		ns
			MIL	4	12		25	30	
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	15		20		20	ns
			MIL	20		20		20	
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (Note 3)	COM'L		17		25		ns
			MIL		20		30	35	
6	TGHQZ	Asynchronous Output Enable HIGH to Output Hi-Z (Notes 2 & 3)	COM'L		17		25		ns
			MIL		20		30	35	
7	TGSVKH	$\overline{G}_S$ to K HIGH Setup Time (Note 4)	COM'L	10		15		15	ns
			MIL	15		15		15	
8	TKHGSX	$\overline{G}_S$ to K HIGH Hold Time (Note 4)	COM'L	5		5		5	ns
			MIL	5		5		5	
9	TKHQV <sub>2</sub>	Delay from K HIGH to Output Valid, for initially Hi-Z outputs (Note 4)	COM'L		17		25		ns
			MIL		20		30	35	
10	TKHQZ	Delay from K HIGH to Output Hi-Z (Notes 2 & 4)	COM'L		17		25		ns
			MIL		20		30	35	
11	TILQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (Note 5)	COM'L		17		30		ns
			MIL		20		35	40	
12	TIHKH	Asynchronous $\overline{I}$ Recovery Time (Note 5)	COM'L	17		20		20	ns
			MIL	20		20		20	
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (Note 5)	COM'L	15		25		25	ns
			MIL	20		30		30	
14	TISVKH	$\overline{I}_S$ to K HIGH Setup Time (Note 6)	COM'L	15		25		30	ns
			MIL	20		30		35	
15	TKHISX	$\overline{I}_S$ to K HIGH Hold Time (Note 6)	COM'L	0		0		0	ns
			MIL	0		0		0	

See also Switching Test Circuits.

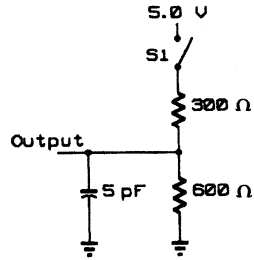
- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A, under Switching Test Circuits.  
 2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B, under Switching Test Circuits.  
 3. Applies only when Asynchronous Enable ( $\overline{G}$ ) function is used.  
 4. Applies only when Synchronous Enable ( $\overline{G}_S$ ) function has been programmed.  
 5. Applies only to the Am27S45 (Asynchronous Initialize ( $\overline{I}$ )) version.  
 6. Applies only to the Am27S47 (Synchronous Initialize ( $\overline{I}_S$ )) version.  
 7. Minimum delay time is guaranteed by design and supported by characterization data.

\*Subgroups 7 and 8 apply to functional tests.

## SWITCHING TEST CIRCUITS



TC003442



TC003452

### A. Output Load for all AC tests except TGHQZ and TKHQZ

### B. Output Load for TGHQZ and TKHQZ

- Notes:
1. All device test loads should be located within 2" of device output pin.
  2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S<sub>1</sub> is closed for all other AC tests.
  3. Load capacitance includes all stray and fixture capacitance.

## SWITCHING WAVEFORMS

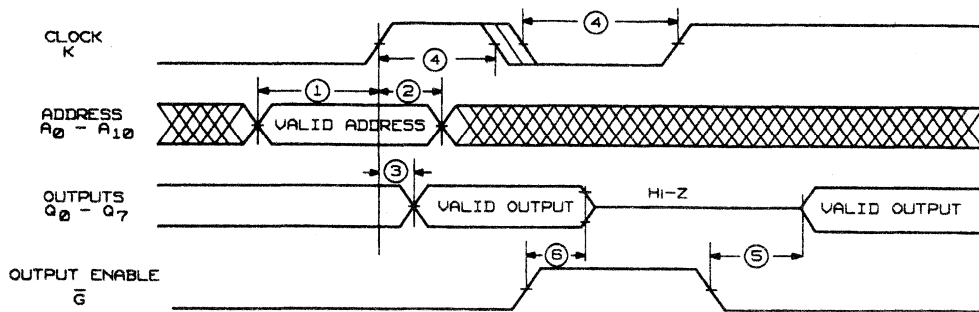
### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

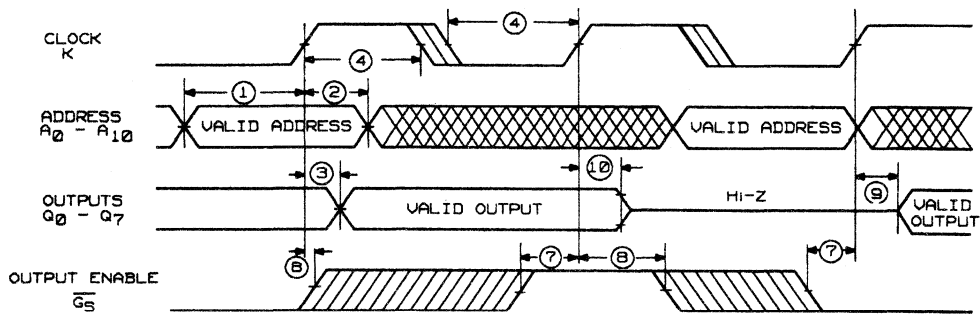


SWITCHING WAVEFORMS (Cont'd.)



WF021691

Timing Set 1. Using Asynchronous Enable

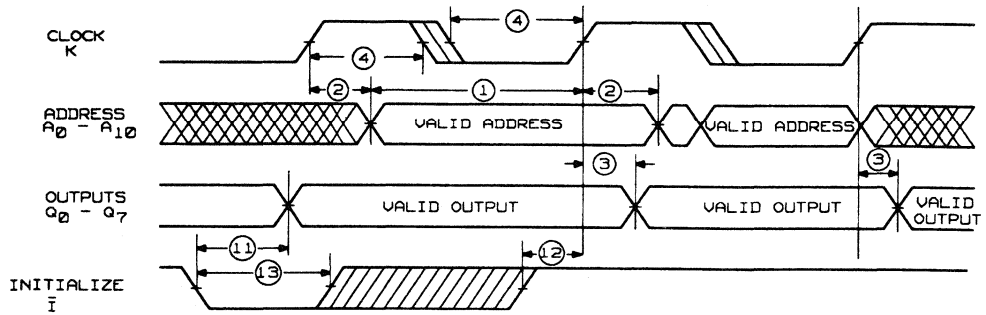


WF021711

Timing Set 2. Using Synchronous Enable

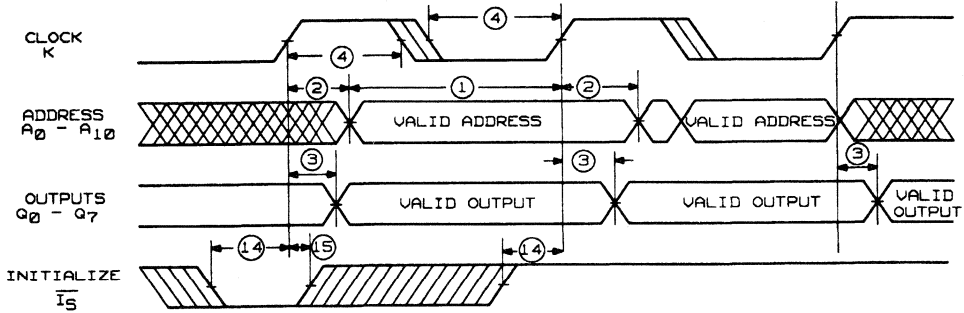
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**SWITCHING WAVEFORMS (Cont'd.)**



WF021720

**Timing Set 3. Using Asynchronous Initialize  
Am27S45 Only**



WF021701

**Timing Set 4. Using Synchronous Initialize  
Am27S47 Only**



# Am27S49/27S49A/29S49SA

8192x8 Generic Series IMOX™ Bipolar PROM

## DISTINCTIVE CHARACTERISTICS

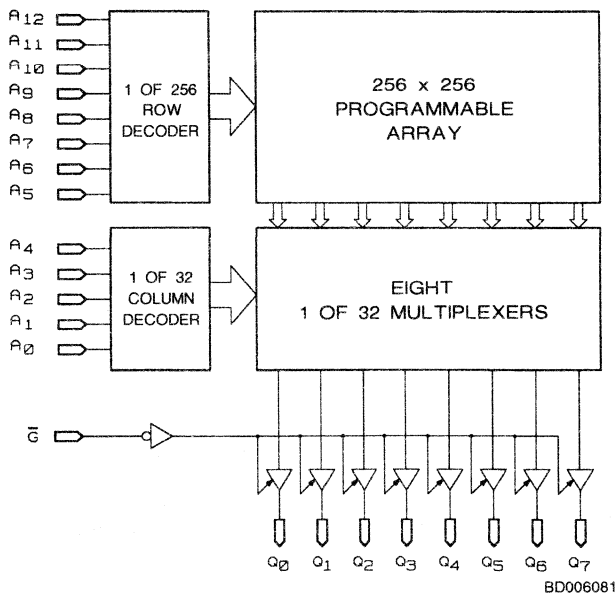
- Fast access time
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensation provides extremely flat AC performance over military range

## GENERAL DESCRIPTION

The Am27S49 Series are high-speed, electrically programmable Schottky read-only memories, organized in 8192 x 8 configuration. After programming, stored information is read on outputs Q<sub>0</sub> - Q<sub>7</sub> by applying unique binary ad-

resses to A<sub>0</sub> - A<sub>12</sub> and holding the Output Enable ( $\bar{G}$ ) input LOW. When  $\bar{G}$  is HIGH, Q<sub>0</sub> - Q<sub>7</sub> are in the OFF, or high-impedance state.

## BLOCK DIAGRAM

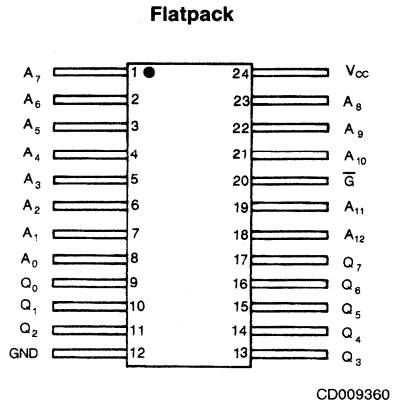
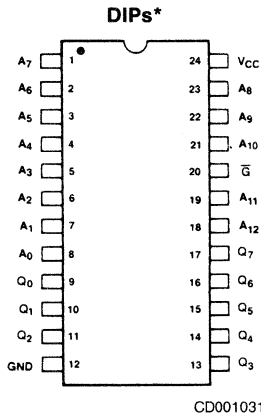


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## PRODUCT SELECTOR GUIDE

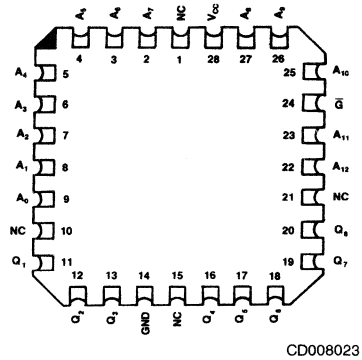
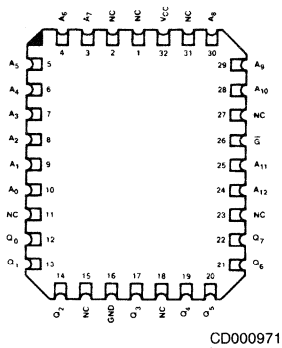
Part Number	Am27S49SA		Am27S49A			Am27S49	
Address Access Time (ns)	25	30	40	45	55	55	65
Operating Range	COM'L	MIL	COM'L	COM'L	MIL	COM'L	MIL

## CONNECTION DIAGRAMS Top View



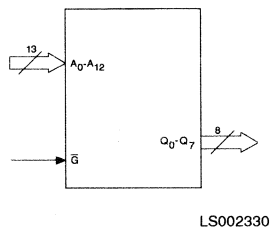
\*Also available in 24-pin Slim DIPs (Alternate Packaging Option Only); pinout is identical to standard DIPs.

### LCCs



Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL

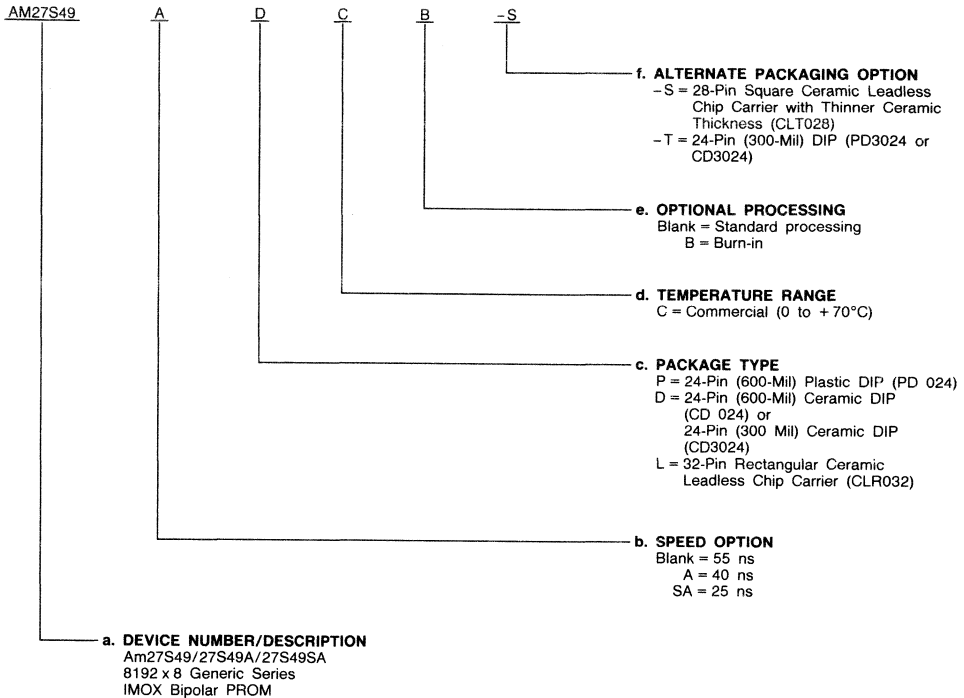


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**
- f. **Alternate Packaging Option**



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#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

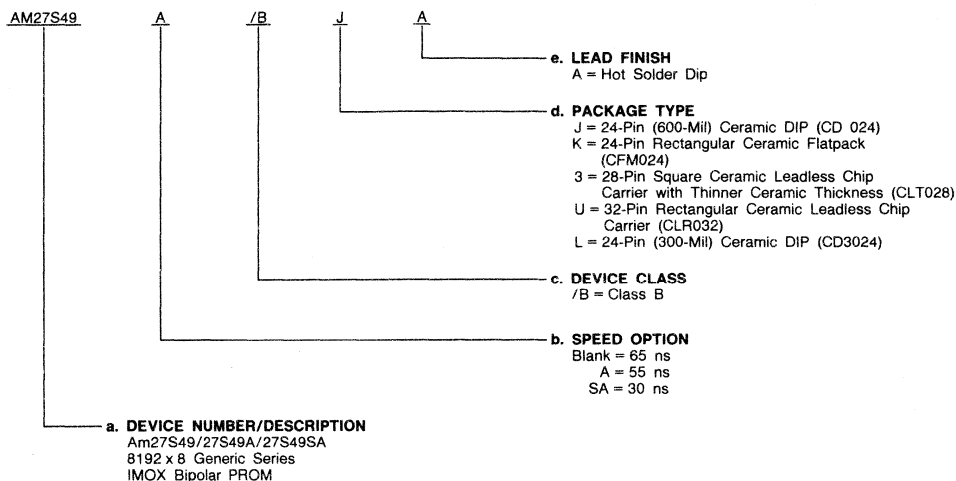
Valid Combinations	
AM27S49	DC, DCB, PC, PCB,
AM27S49A	LC, LCB, LC-S, LCB-S,
AM27S49SA	DC-T, DCB-T, PC-T, PCB-T

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



### Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM27S49	
AM27S49A	/BJA, /BKA, /B3A, /BUA, /BLA
AM27S49SA	

### Group A Tests

Group A tests include Subgroups 1, 2, 3, 7, 8, 9, 10, and 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

### PIN DESCRIPTION

#### A<sub>0</sub> - A<sub>12</sub> Address (Inputs)

The 13-bit field presented at the address inputs selects one of 8192 memory locations to be read from.

#### $\bar{G}$ Output Enable (Input, Active LOW)

Provides direct control of the Q-output three-state buffers.

#### Q<sub>0</sub> - Q<sub>7</sub> Data Output Port (Outputs, Three-State)

The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which when disabled, are in a floating or high-impedance state.

### GENERIC PROGRAMMING INFORMATION

Advanced Micro Devices' Bipolar PROMs are members of a generic series incorporating common programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be

selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

See the AMD Bipolar/MOS Memories Data Book for detailed programming information.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military Product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>					0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)			2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)					0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V					-250	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max.	COM'L MIL	V <sub>IN</sub> = 5.0 V V <sub>IN</sub> = V <sub>CC</sub>			40	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 2)	-20	-90	mA			
I <sub>CC</sub>	Power Supply Current	All Inputs = GND, V <sub>CC</sub> = Max.		COM'L MIL			190 190	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA					-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. G = 2.4 V	COM'L MIL	V <sub>O</sub> = 5.0 V V <sub>O</sub> = V <sub>CC</sub> V <sub>O</sub> = 0.4 V			40 -40	μA
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C				5		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> /V <sub>OUT</sub> = 2.0 V at f = 1 MHz (Note 3)				8		

- Notes: 1. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.  
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

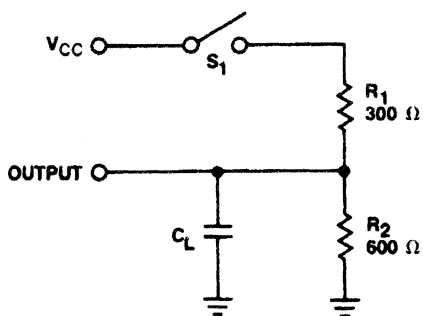
**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

No.	Parameter Symbol	Parameter Description	Am27S49SA		Am27S49A		Am27S49		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time	COM'L	25	40	55	ns		
			MIL	30	55	65			
2	TGHQZ	Delay from Output Enable Valid to Output High Z	COM'L	15	30	35	ns		
			MIL	20	35	40			
3	TGLQV	Delay from Output Enable Valid to Output Valid	COM'L	15	30	35	ns		
			MIL	20	35	40			

- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V — See Switching Test Circuit diagram.  
\*Subgroups 7 and 8 apply to functional tests.



## SWITCHING TEST CIRCUIT



TC000171

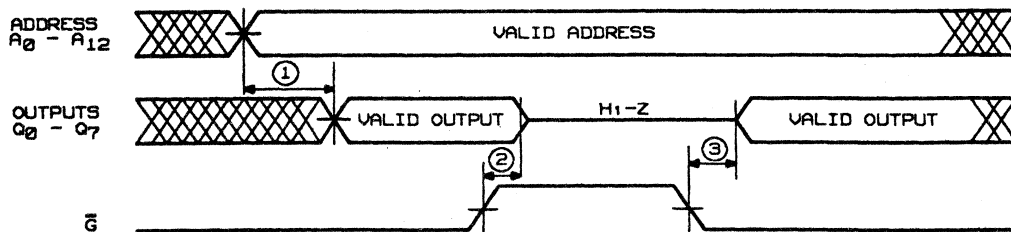
- Notes: 1. TAVQV is tested with switch  $S_1$  closed and  $C_L = 50$  pF.  
 2. For three-state outputs, TGLQV is tested with  $C_L = 50$  pF to the 1.5 V level;  $S_1$  is open for high impedance to HIGH tests and closed for high impedance to LOW tests. TGHQZ is tested with  $C_L = 5$  pF. HIGH to high impedance tests are made with  $S_1$  open to an output voltage of Steady State HIGH  $-0.5$  V; LOW to high-impedance tests are made with  $S_1$  closed to the Steady State LOW  $+0.5$  V level.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000011



WF021480



# Am27S85/27S85A

16,384-Bit (4096x4) Registered PROM  
with SSR™ Diagnostics Capability



## DISTINCTIVE CHARACTERISTICS

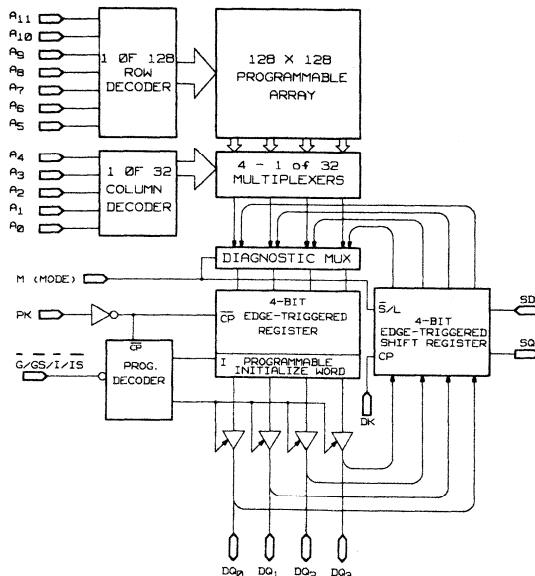
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable for Asynchronous Enable, Synchronous Enable, Asynchronous Initialize, or Synchronous Initialize
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and registers.
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability.
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%).
- Increased drive capability, 24 mA  $I_{OL}$

## GENERAL DESCRIPTION

This device contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies, the shadow register is intended to operate in the background of the normal output data register. This shadow register can be used in a systematic way to control and observe the output data register to exercise desired system functions during a diagnostic test mode.

To offer the system designer maximum flexibility, this device contains a single programmable multi-functional input ( $\bar{G}/GS/I/IS$ ). The unprogrammed state of this pin operates an Asynchronous Enable ( $\bar{G}$ ) input. An architecture word permits the programming of the functionality of this pin to Synchronous Enable ( $GS$ ), Asynchronous Initialize ( $I$ ), or Synchronous Initialize ( $IS$ ).

## BLOCK DIAGRAM



BD005850

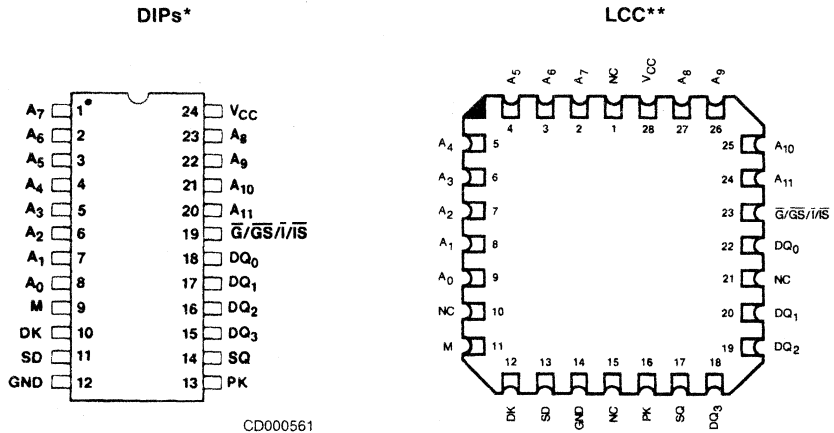
5

## PRODUCT SELECTOR GUIDE

Part Number	Am27S85A		Am27S85	
Address Setup Time	27 ns	30 ns	35 ns	40 ns
Clock-to-Output Delay	12 ns	17 ns	15 ns	20 ns
Operating Range	C	M	C	M

## CONNECTION DIAGRAMS

### Top View

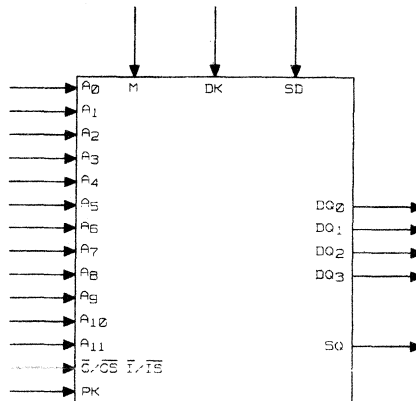


\*Also available in a 24-pin Flatpack. Pinout identical to DIPs.

\*\*Also available in a 28-pin Square PLCC. Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



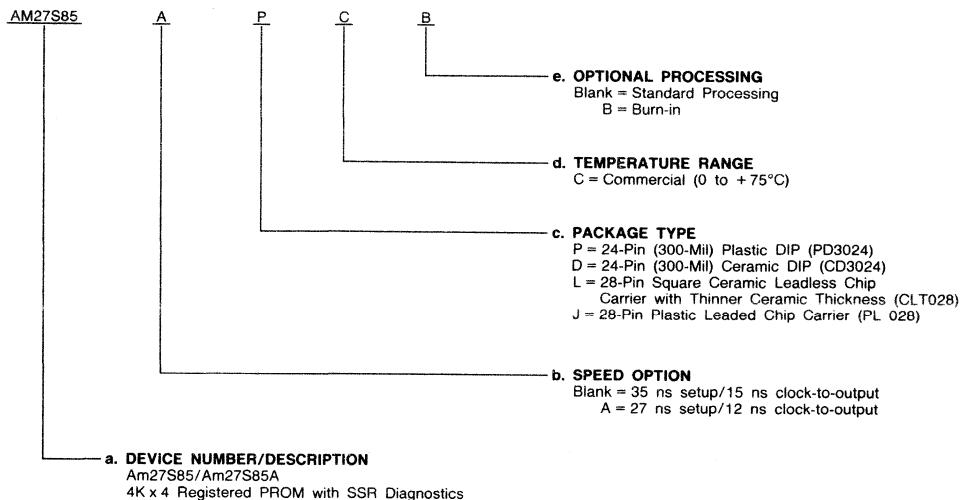
LS002111

## ORDERING INFORMATION

### Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM27S85	PC, PCB, DC, DCB,
AM27S85A	LC, LCB, JC, JCB

#### Valid Combinations

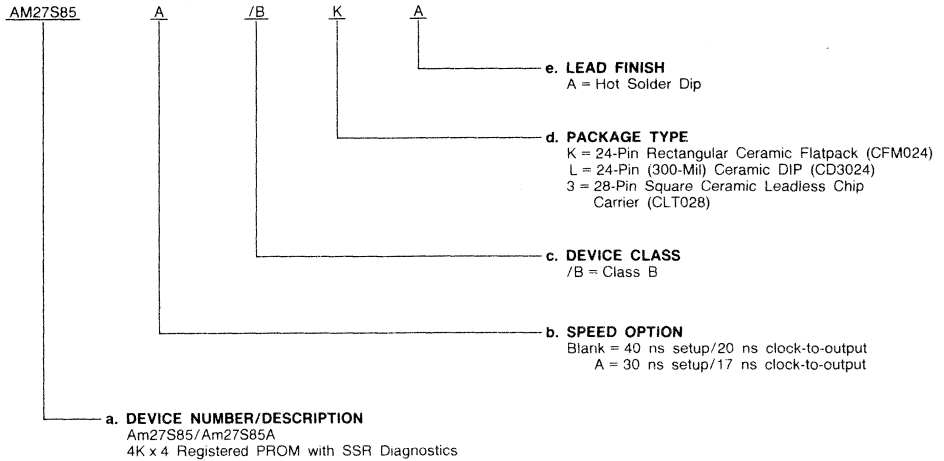
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S85	/BKA, /BLA, /B3A
AM27S85A	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>11</sub> Address Inputs

The 12-bit field presented at the address inputs selects one of 4096 memory locations to be read from.

### PK Pipeline Clock (Input)

The pipeline clock is used to load data into the parallel registers. The data source may be the memory array, the shadow register, or the initialize word if programmed for synchronous initialize architecture. Transfer occurs on the LOW-to-HIGH transition of PK.

### DQ<sub>0</sub> - DQ<sub>3</sub> Data I/O Port

Parallel data output from the pipeline register or parallel data input to the shadow register.

### M Mode (Input)

Control input which controls the source data for both sets of registers. MODE inputs is LOW in the normal mode of operation. The PROM array is the input source for the output data registers. The shadow register is in the shift mode (SD→S<sub>0</sub>→S<sub>1</sub>→S<sub>2</sub>→S<sub>3</sub>/SQ). MODE input HIGH allows transfer of data for diagnostic testing. Shadow register data may be loaded into the output register or output data bus information may be loaded into the shadow register.

### DK Diagnostic Clock (Input)

The diagnostic clock is used to load or shift the data into the shadow register. Transfer occurs on the LOW-to-HIGH transition of DK.

### SD Serial Data Input

This pin performs two functions depending on the state of the MODE input. If M is LOW, the SD pin is the data transfer pin for serial data (SD→S<sub>0</sub>). If the M input is HIGH, the SD pin operates as a control pin where SD asserted LOW permits output data to be loaded into the shadow register on the next LOW-to-HIGH transition of DK. SD asserted HIGH represents a NO-OP function on this device.

### SQ Serial Data Output

This pin operates as a transfer pin for serial data. When M input is LOW, SQ = S<sub>3</sub>. When M is HIGH and SD operates as a control pin, the SQ pin operates as a pass through of SD control. SQ is an active totem-pole output.

### VCC Device Power Supply Pin

The most positive of the logic power supply pins.

### GND Device Power Supply Pin

The most negative of the logic power supply pins.

This device contains a two bit architecture word which, according to programming, will provide the following functions:

### G/GS/I/I Asynchronous/Synchronous Output Enable/Asynchronous/Synchronous Initialize

With the architecture word unprogrammed this pin operates as an Asynchronous Output Enable (G) and provides direct control of the DQ output three-state drivers independent of PK. With proper programming of the architecture word this pin will function as a Synchronous Output Enable (GS) which will control the state of the DQ output three-state drivers in conjunction with PK. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

The architecture word may also be programmed so that this pin will function as an Asynchronous Initialize (I) which is a control pin used to initialize the output data registers from a programmable word independent of PK. This can be used to generate any arbitrary microinstruction for system interrupt or reset. When the architecture word is properly programmed this pin will function as a Synchronous Initialize (IS) which will initialize the output data registers from a programmable word in conjunction with PK. This can be used for a system interrupt or reset which must be synchronized with PK.

## MODE SELECT TABLE

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DK. M (MODE) and SD determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PK. M (MODE) selects whether the data source is the PROM Array or the shadow register output.

Because of the independence of the clock inputs, data can be shifted in the shadow register via DK and loaded into the pipeline register from the data input via PK as long as no set up or hold times are violated.

Inputs					Outputs			Operation
SD	M	DK	PK	$\overline{IS}^*$	SQ	Shadow Register	Pipeline Register	
X	L	↑	–	X	S <sub>3</sub>	S <sub>n</sub> –S <sub>n-1</sub> S <sub>0</sub> –SD	NA	Serial Shift; SD→S <sub>0</sub> →S <sub>1</sub> →S <sub>2</sub> →S <sub>3</sub> /SQ
X	L	–	↑	H	S <sub>3</sub>	NA	Q <sub>n</sub> – ARRAY DATA	Normal Load Pipeline Register from PROM
X	L	–	↑	L	S <sub>3</sub>	NA	Q <sub>n</sub> – INIT DATA	Synchronous Initialize Pipeline Register*
L	H	↑	–	X	SD	S <sub>n</sub> –Q <sub>n</sub>	NA	Load Shadow Register from Outputs (DQ <sub>0</sub> –DQ <sub>3</sub> )
X	H	–	↑	X	SD	NA	Q <sub>n</sub> –S <sub>n</sub>	Load Pipeline Register from Shadow Register
H	H	↑	–	X	SD	Hold	NA	No-Op; Hold Shadow Register

### MODE SELECT TABLE DEFINITIONS

#### INPUTS

H = HIGH  
 L = LOW  
 X = Don't Care  
 – = Steady State LOW or HIGH or HIGH-to-LOW transition  
 ↑ = LOW-to-HIGH transition

#### OUTPUTS

SQ = Serial Data Output  
 S<sub>3</sub>–S<sub>0</sub> = Shadow Register Outputs (internal to devices)  
 Q<sub>3</sub>–Q<sub>0</sub> = Pipeline Register Outputs  
 NA = NOT applicable; Output is not a function of the specified input combinations

\*Applies only if the architecture word has been programmed for Synchronous Initialize operation.

## APPLICATIONS

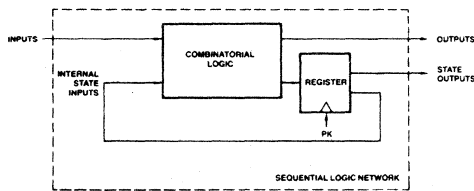
### Applying Serial Shadow Register (SSR) Diagnostics in Bipolar Microcomputers

#### Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals – address, data, control, and status – to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs and determine whether the system is functioning correctly.

#### Testing Combinational and Sequential Networks

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.



AF000181

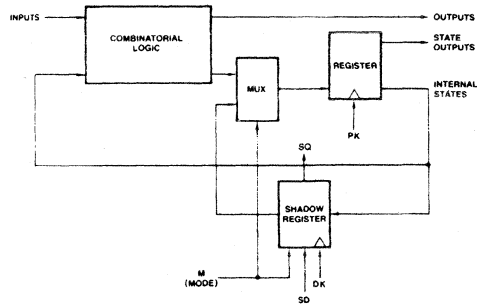
Figure 1.

A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available.

The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

#### Serial Shadow Register Diagnostics

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.



AF000191

Figure 2.

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 to $V_{CC}$ Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec.) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature ( $T_A$ ) .....	0 to +75°C
Supply Voltage ( $V_{CC}$ ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature ( $T_C$ ) .....	-55 to +125°C
Supply Voltage ( $V_{CC}$ ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

\*Military product 100% tested at  $T_C = +25^\circ\text{C}$ ,  $+125^\circ\text{C}$ , and  $-55^\circ\text{C}$ .

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
$V_{IH}$	Input Voltage HIGH	Guarantee Input HIGH Voltage (Note 1)	2.0			V
$V_{IL}$	Input Voltage LOW	Guarantee Input LOW Voltage (Note 1)			0.8	V
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min.}$ , $I_{IN} = -18 \text{ mA}$			-1.2	V
$V_{OH}$	Output Voltage (HIGH)	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	2.4			V
		$I_{OH} (DQ_0 - DQ_3) = -2 \text{ mA}$ $I_{OH} (SQ) = -0.5 \text{ mA}$				
$V_{OL}$	Output Voltage (LOW)	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$			0.5	V
$I_{IH}$	Input Current (HIGH)	$V_{CC} = \text{Max.}$			25	$\mu\text{A}$
					40	
$I_{IL}$	Input Current (LOW)	$V_{CC} = \text{Max.}$ , $V_{IN} = 0.40 \text{ V}$			-250	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{CC} = \text{Max.}$ $V_{OUT} = 0 \text{ V}$ (Note 2)			-90	mA
					-85	
$I_{CEX}$	Output Leakage Current	$V_{CC} = \text{Max.}$ $V_{G}/\overline{GS} = 2.4 \text{ V}$ (Note 3)			50	$\mu\text{A}$
					-150	
$I_{CC}$	Power Supply Current	$V_{CC} = \text{Max.}$ , All inputs = 0.0 V (Note 4)	COM'L	$T_A = 0^\circ\text{C}$	185	mA
				$T_A = 25^\circ\text{C}$	175	
				$T_A = 75^\circ\text{C}$	165	
			MIL	$T_C = -55^\circ\text{C}$	195	
				$T_C = 25^\circ\text{C}$	180	
				$T_C = 125^\circ\text{C}$	155	
$C_{IN}$	Input Capacitance	$V_{CC} = 5.0 \text{ V}$ , $T_A = 25^\circ\text{C}$		5	pF	
$C_{OUT}$	Output Capacitance	$V_{IN}/V_{OUT} = 2.0 \text{ V}$ @ $f = 1 \text{ MHz}$ (Note 5)		12		

- Notes: 1.  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4.  $I_{CC}$  limits at temperature extremes are guaranteed by correlation to 25°C test limits.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.



**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*) (Note 1)

No.	Parameter Symbol	Parameter Description	Am27S85A				Am27S85				Unit
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVPKH	Address to PK HIGH Setup Time	27		30		35		40		ns
2	TPKHAX	Address to PK HIGH Hold Time	0		0		0		0		ns
3	TPKHDQV1	Delay from PK HIGH to Output Valid, for initially active outputs (HIGH) or LOW (Note 7)	4	12	4	17	4	15	4	20	ns
4	TPKHPKL TPKLPKH	PK Pulse Width (HIGH or LOW)	15		20		20		20		ns
5	TGLDQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (Note 3)		22		25		25		30	ns
6	TGHDQZ	Asynchronous Output Enable HIGH to Output High Z (Note 3)		17		22		20		25	ns
7	TGSVPKH	$\overline{GS}$ to PK HIGH Setup Time (Note 4)	12		12		15		15		ns
8	TPKHGSX	$\overline{GS}$ to PK HIGH Hold Time (Note 4)	0		0		0		0		ns
9	TPKHDQV2	Delay from PK HIGH to Output Valid, for initially High Z outputs (Note 4)		17		22		20		25	ns
10	TPKHDQZ	Delay from PK HIGH to Output High Z (Notes 2 & 4)		17		22		20		25	ns
11	TILDQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (Note 5)		25		30		30		35	ns
12	TIHPKH	Asynchronous $\overline{I}$ Recovery to PK (HIGH) (Note 5)	20		25		25		30		ns
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (LOW) (Note 5)	20		20		25		25		ns
14	TISVPKH	$\overline{IS}$ to PK HIGH Setup Time (Note 6)	20		25		20		25		ns
15	TPKHISX	$\overline{IS}$ to PK HIGH Setup Time (Note 6)	5		5		5		5		ns

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V, using test loads in A & B.

2. TGHDQZ and TPKHDQZ are measured to Steady State HIGH -0.5 V and Steady State LOW +0.5 V output levels, using the test load in C.

3. Applies only if the architecture is configured for Asynchronous Enable.

4. Applies only if the architecture word has been programmed for a Synchronous Enable input.

5. Applies only if the architecture word has been programmed for a Synchronous Initialize input.

6. Applies only if the architecture word has been programmed for a Synchronous Initialize input.

7. Minimum Delay times are guaranteed by design and supported by characterization data.

\*Subgroups 7 and 8 apply to functional tests.

**5**

**DIAGNOSTIC MODE SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

No.	Parameter Symbol	Parameter Description	Am27S85/27S85A				Unit
			COM'L		MIL		
			Min.	Max.	Min.	Max.	
16	TSDVDKH	Serial Data In to DK HIGH Setup Time	25		30		ns
17	TDKHS DX	Serial Data In to DK HIGH Hold Time	0		0		ns
18	TMV PKH	Mode to PK HIGH Setup Time	35		40		ns
19	TPK HMX	Mode to PK HIGH Hold Time	0		0		ns
20	TMVDKH	Mode to DK HIGH Setup Time	35		40		ns
21	TDK HMX	Mode to DK HIGH Hold Time	0		0		ns
22	TDQVDKH	Output Data In to DK HIGH Setup Time	25		30		ns
23	TDK HDQX	Output Data In to DK HIGH Hold Time	0		0		ns
24	TDKHSQV	Delay from DK HIGH to Serial Data Output (Shifting)		30		35	ns
25	TSDVSQV	Delay from SD Valid to SQ Valid (Mode Input HIGH)		25		30	ns
26	TDKHDKL TDKLDKH	DK Pulse Width (HIGH or LOW)		25		25	ns
27	TMHSQV TMLSQV	Delay from Mode (HIGH or LOW) to SQ Valid		25		30	ns

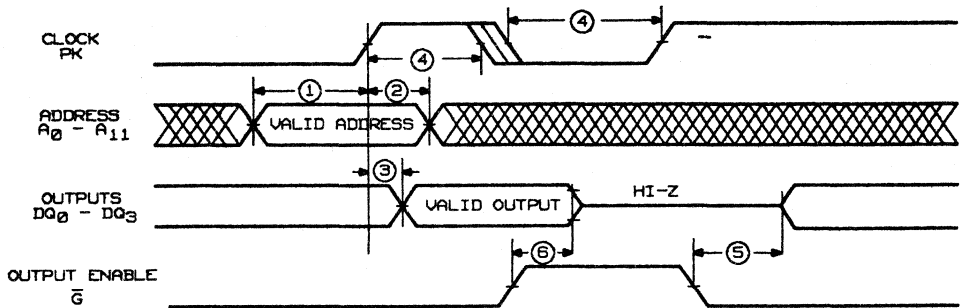
See also Switching Test Circuits.

# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

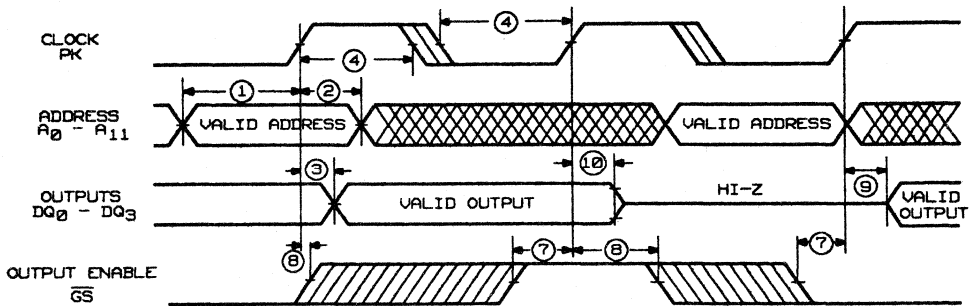
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF020770

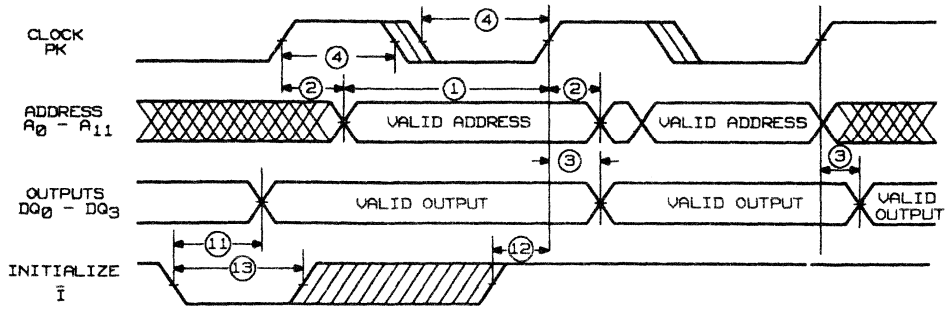
Timing Set 1. Using Asynchronous Enable



WF020780

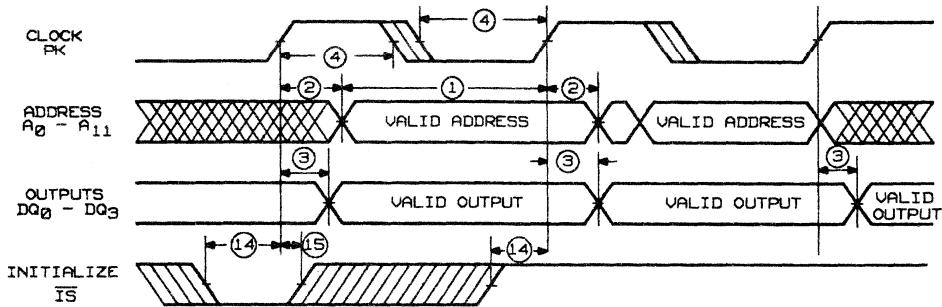
Timing Set 2. Using Synchronous Enable

SWITCHING WAVEFORMS (Cont'd.)



WF020790

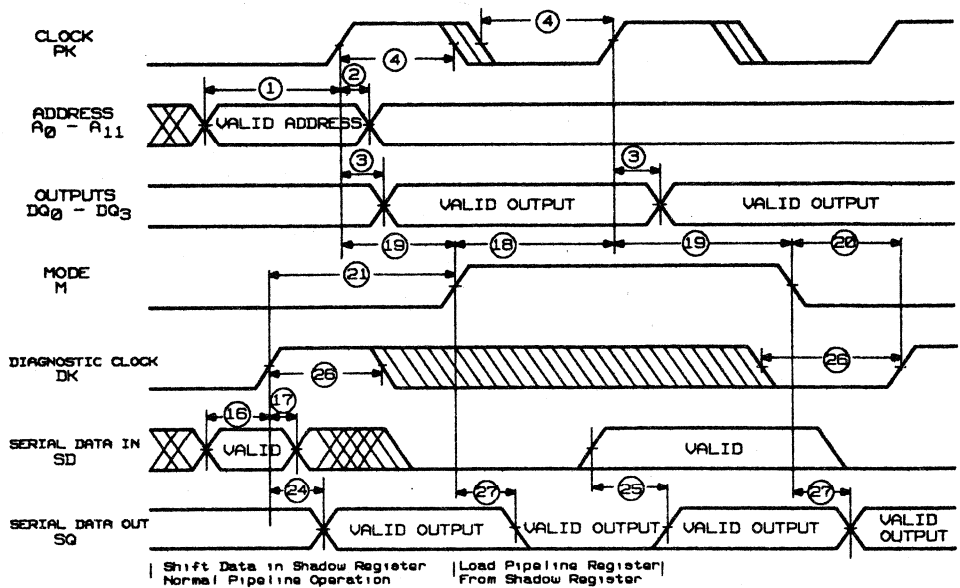
Timing Set 3. Using Asynchronous Initialize



WF020800

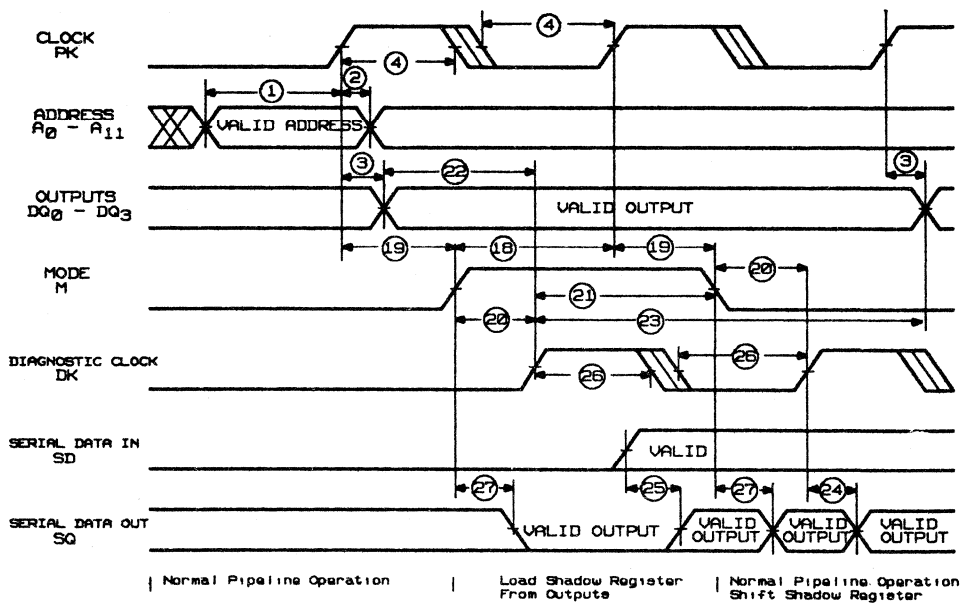
Timing Set 4. Using Synchronous Initialize

SWITCHING WAVEFORMS (Cont'd.)



WF020810

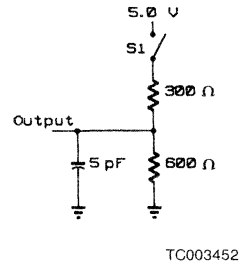
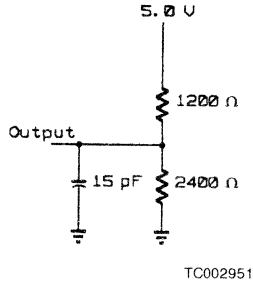
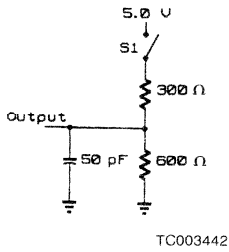
Timing Set 5. Diagnostic Test Mode (System Control)



WF020820

Timing Set 6. Diagnostic Test Mode (System Observation)

## SWITCHING TEST CIRCUITS



### A. Output Load for DQ<sub>0</sub> – DQ<sub>3</sub>

### B. Output Load for SQ

### C. Output Load for TGHDQZ and TPKHDQZ on Outputs DQ<sub>0</sub> – DQ<sub>3</sub>

- Notes:
1. All devices test loads should be located within 2" of device output pin.
  2. S<sub>1</sub> is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S<sub>1</sub> is closed for all other AC tests.
  3. Load capacitance includes all stray and fixture capacitance.

## NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V<sub>CC</sub> and ground terminals. Multiple capacitors are recommended, including a 0.1 μFarad or larger capacitor and a 0.01 μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of

power supply voltage, creating erroneous function or transient performance failures.

2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

# Am27S181/27S181A

# Am27S281/27S281A

## 8,192-Bit (1024x8) Bipolar PROM



### DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts — enhances reliability through total system heat reduction
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Rapid recovery from power-down state provides minimum delay

### GENERAL DESCRIPTION

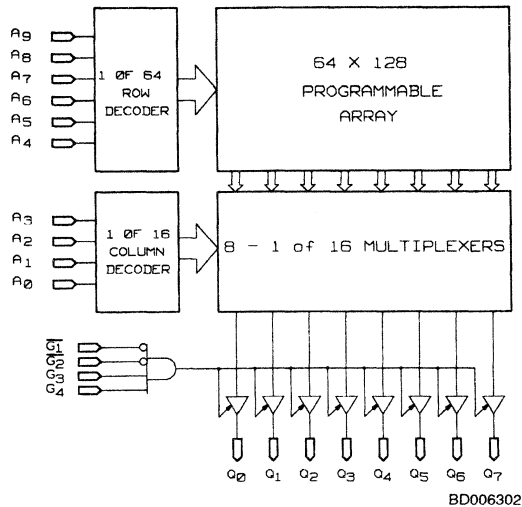
The Am27S181 (1024 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs which are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic

replacement. Easy word-depth expansion is facilitated by both active LOW ( $\overline{G}_1$  and  $\overline{G}_2$ ) and active HIGH ( $G_3$  and  $G_4$ ) output enables.

This device is also available in a 300-mil. lateral-center DIP (Am27S281).

### BLOCK DIAGRAM



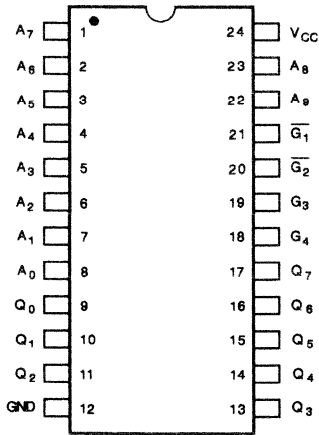
### PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S181A, Am27S281A		Am27S181, Am27S281	
Address Access Time	35 ns	50 ns	60 ns	80 ns
Operating Range	C	M	C	M

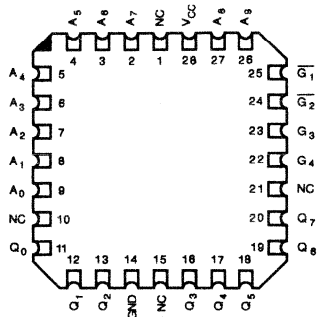
## CONNECTION DIAGRAMS Top View

DIP

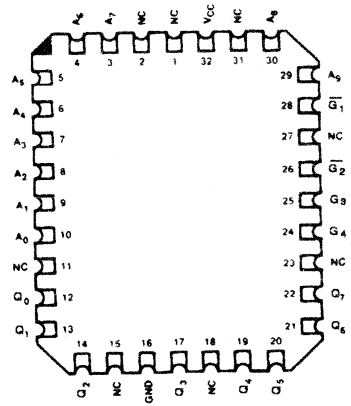
LCCs\*\*



CD000791



CD009561



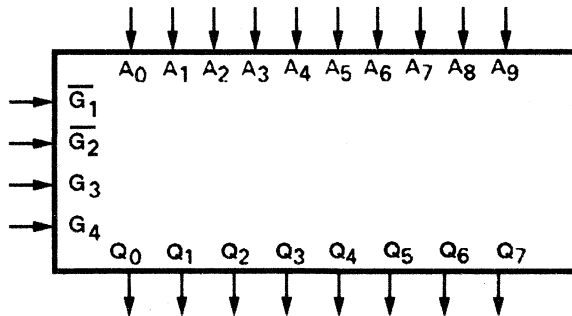
CD000821

\*Also available in a 300-mil DIP and a 24-pin Flatpack. Pinout identical to those listed here for the 600-mil DIP.

\*\*Also available in a 28-Pin Square PLCC. Pinout identical to the 28-Pin LCC.

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



LS000193

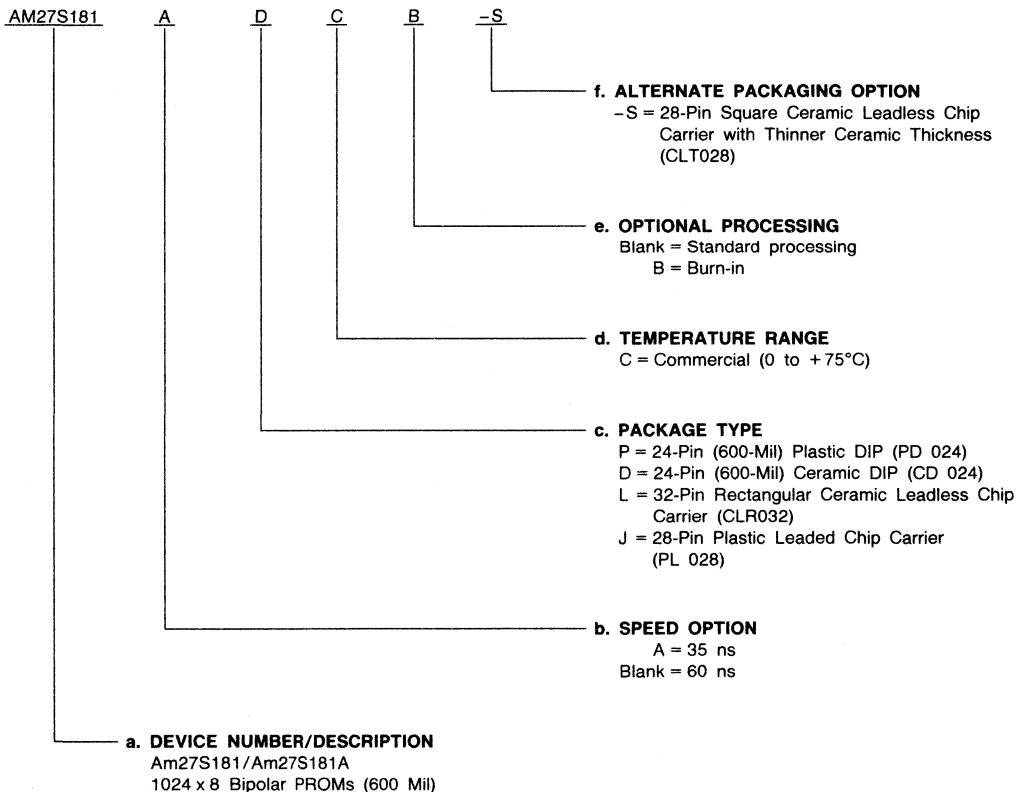
## ORDERING INFORMATION

(Am27S181/181A)

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing
- f. Alternate Packaging Option



Valid Combinations	
AM27S181	PC, PDB, DC, DCB, LC, LCB, LC-S, LCB-S,
AM27S181A	JC, JCB

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.



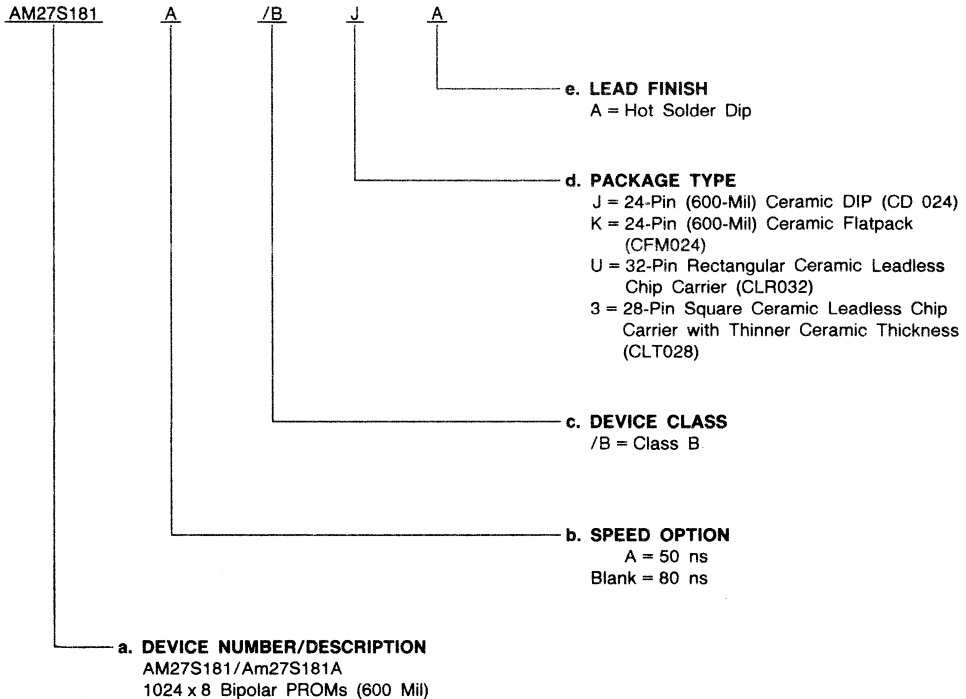
## MILITARY ORDERING INFORMATION

(Am27S181/181A)

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S181	/BJA, /BKA, /BUA,
AM27S181A	/B3A

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

5

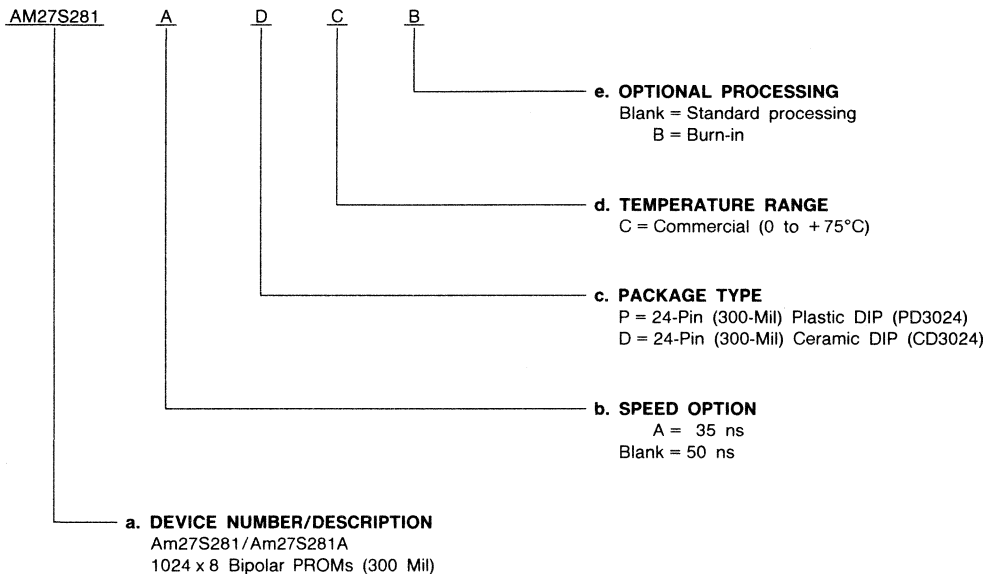
## ORDERING INFORMATION

(Am27S281/281A)

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM27S281	PC, PCB, DC, DCB
AM27S281A	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

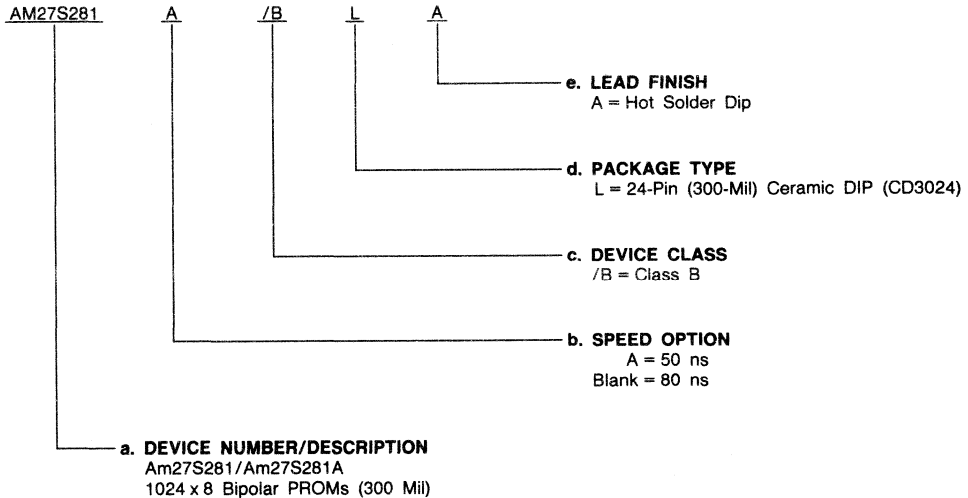
## MILITARY ORDERING INFORMATION

(Am27S281/281A)

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S281	/BLA
AM27S281A	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

### PIN DESCRIPTION

#### A<sub>0</sub> – A<sub>9</sub> Address Inputs

The 10-bit field presented at the address inputs selects one of 1,048 memory locations to be read from.

#### Q<sub>0</sub> – Q<sub>7</sub> Data Output Port

The outputs whose state represents the data read from the selected memory locations.

#### $\bar{G}_1, \bar{G}_2, G_3, G_4$ Output Enable

Provides direct control of the Q output buffers. Outputs disabled force all outputs to a floating or high-impedance

state.

$$\text{Enable} = \bar{G}_1 \cdot \bar{G}_2 \cdot G_3 \cdot G_4$$

$$\begin{aligned} \text{Disable} &= \bar{G}_1 \cdot \bar{G}_2 \cdot G_3 \cdot G_4 \\ &= G_1 + G_2 + \bar{G}_3 + \bar{G}_4 \end{aligned}$$

#### V<sub>CC</sub> Device Power Supply Pin

The most positive of the logic power supply pins

#### GND Device Power Supply Pin

The most negative of the logic power supply pins.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>			40	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 1)	COM'L -20 MIL -15		-90 -90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND			185	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEx</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>G1</sub> = 2.4 V			40 -40	μA
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 2) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		4.0		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 2) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		8.0		

- Notes: 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.  
 2. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.  
 3. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

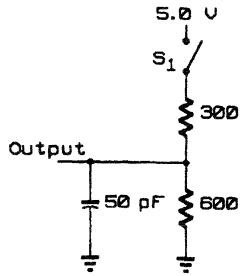
**SWITCHING CHARACTERISTICS** (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

No.	Parameter Symbol	Parameter Description	Version	COM'L	MIL	Unit
				Max.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time	A	35	50	ns
			STD	60	80	
2	TGVQZ TEVQZ	Delay from Output Enable Valid to Output Hi-Z	A	25	30	ns
			STD	40	50	
3	TGVQV TEVQV	Delay from Output Enable Valid to Output Valid	A	25	30	ns
			STD	40	50	

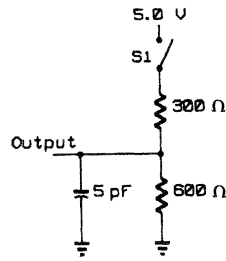
See also Switching Test Circuits.

- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in Figure A.  
 2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in Figure B.

## SWITCHING TEST CIRCUITS



TC003441



TC003452

### A. Output Load for all Switching tests except TGVQZ

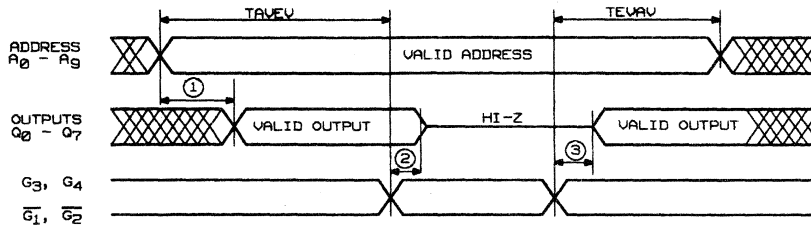
### B. Output Load for TGVQZ

- Notes: 1. All device test loads should be located within 2" of device output pin.  
 2.  $S_1$  is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests.  
 $S_1$  is closed for all other Switching tests.  
 3. Load capacitance includes all stray and fixture capacitance.

## SWITCHING WAVEFORM KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF021683



# Am27S185/27S185A

8,192-Bit (2048x4) Bipolar PROM

## DISTINCTIVE CHARACTERISTICS

- Ultra-fast access time "A" version (35 ns Max.) — Fast access time Standard version (50 ns Max.) — allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

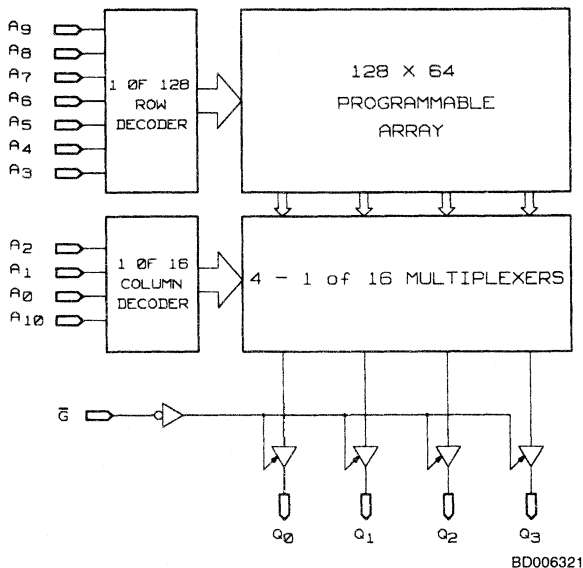
## GENERAL DESCRIPTION

The Am27S185 (2048 words by 4 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs, compatible with low-power Schottky bus standards capable of satisfying the

requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy-word depth expansion is facilitated by an active LOW ( $\bar{G}$ ) output enable.

## BLOCK DIAGRAM

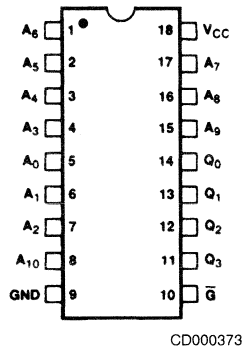


## PRODUCT SELECTOR GUIDE

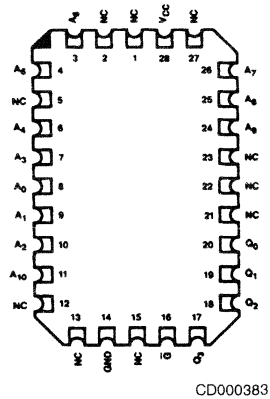
Three-State Part Number	Am27S185A		Am27S185	
	Address Access Time	35 ns	45 ns	50 ns
Operating Range	C	M	C	M

## CONNECTION DIAGRAMS Top View

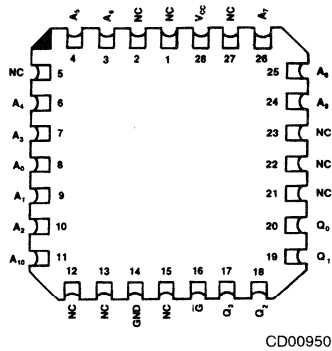
**DIPs\***



**LCC**



**LCC\*\***

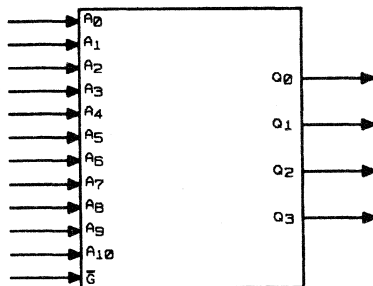


Note: Pin 1 is marked for orientation.

\*Also available in an 18-pin Flatpack. Pinout identical to DIPs.

\*\*Also available in a 28-pin square PLCC. Pinout identical to LCC.

## LOGIC SYMBOL



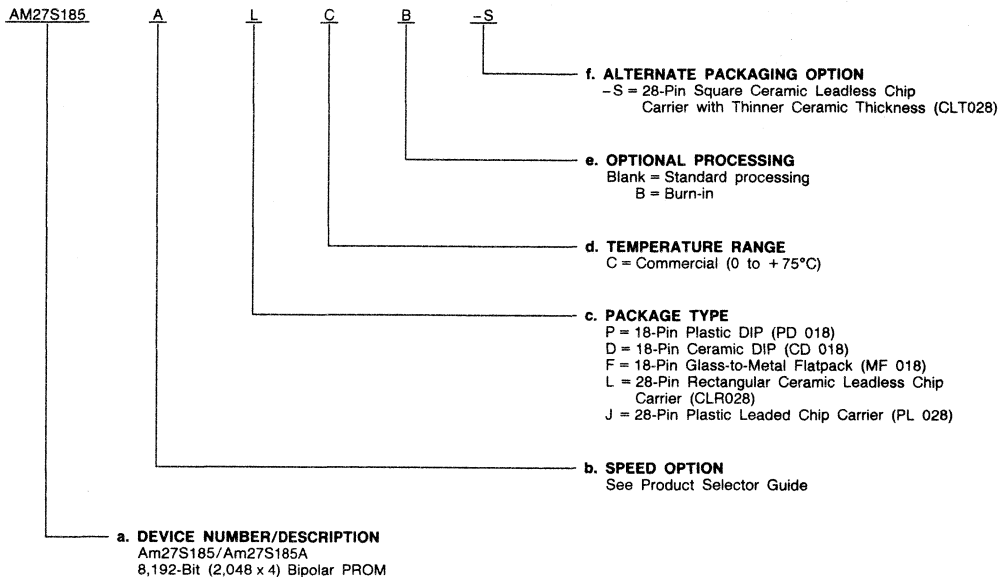
LS002411

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**
- f. **Alternate Packaging Option**



Valid Combinations	
AM27S185	PC, PCB, DC DCB, FC, FCB, LC, LCB, LC-S, LCB-S, JC, JCB
AM27S185A	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

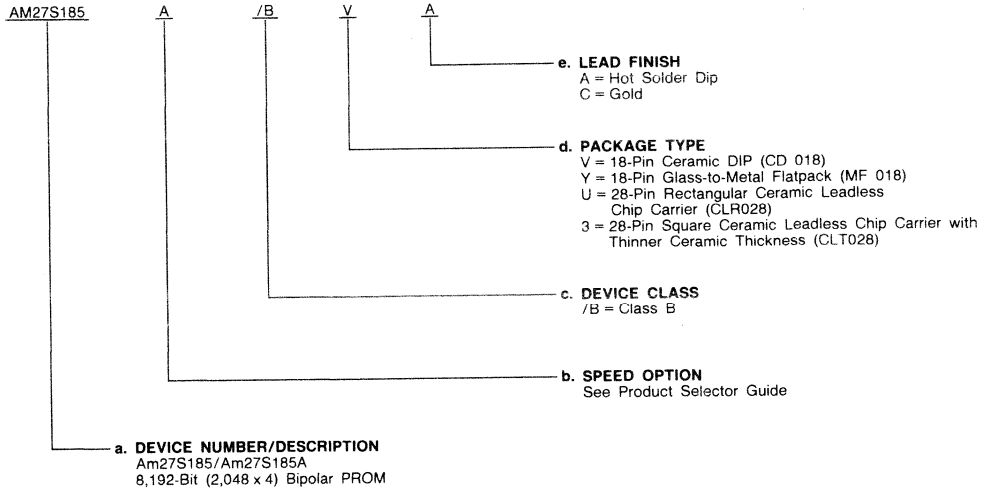


## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S185	/BVA, /BYC,
AM27S185A	/BUA, /B3A,

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
 1, 2, 3, 7, 8, 9, 10, 11.

#### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

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## PIN DESCRIPTION

### **A<sub>0</sub> - A<sub>10</sub> Address Inputs**

The 11-bit field presented at the address inputs selects one of 2,048 memory locations to be read from.

### **Q<sub>0</sub> - Q<sub>3</sub> Data Output Port**

The outputs whose state represents the data read from the selected memory locations.

### **$\bar{G}$ Output Enable**

Provides direct control of the Q-output buffers. Outputs disabled forces all three-state outputs to a floating or high-impedance state.

Enable =  $\bar{G}$

Disable = G

### **V<sub>CC</sub> Device Power Supply Pin**

The most positive of the logic power supply pins.

### **GND Device Power Supply Pin**

The most negative of the logic power supply pins.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices	Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military products 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub> (Note 1)	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>			40	μA
I <sub>SC</sub> (Note 1)	Output Short Circuit Current	V <sub>CC</sub> = Max. V <sub>OUT</sub> = 0.0 V (Note 3)	-20		-90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND V <sub>CC</sub> = Max.			150	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>G</sub> = 2.4 V			40	μA
		V <sub>O</sub> = V <sub>CC</sub> V <sub>O</sub> = 0.4 V			-40	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5 V., T <sub>A</sub> = 25°C		5.0		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5 V., T <sub>A</sub> = 25°C		8.0		

Notes: 1. This applies to three-state devices only.

2. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.

4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

5

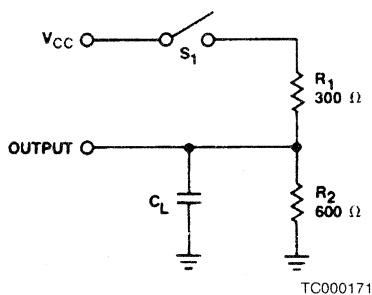
**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

No.	Parameter Symbol	Parameter Description	Version	COM'L		MIL		Unit
				Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time	A		35		45	ns
			STD		50		55	
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	A		25		30	ns
			STD		25		30	
3	TGVQV	Delay from Output Enable Valid to Output Valid	A		25		30	ns
			STD		25		30	

See also Switching Test Circuit.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.






### SWITCHING TEST CIRCUIT



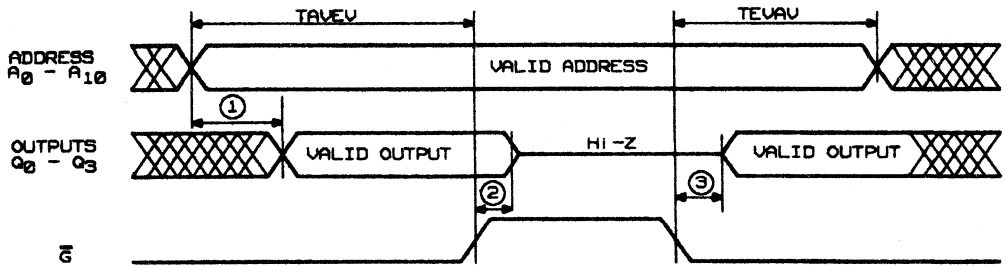
- Notes: 1. TAVQV is tested with switch  $S_1$  closed and  $C_L = 50\ \text{pF}$ .  
 2. For three-state outputs, TGVQV is tested with  $C_L = 50\ \text{pF}$  to the 1.5 V level;  $S_1$  is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGVQZ is tested with  $C_L = 5\ \text{pF}$ . HIGH to high-impedance tests are made to an output steady state HIGH voltage  $-0.5\ \text{V}$  with  $S_1$  open; LOW to high-impedance tests are made to the steady state LOW  $+0.5\ \text{V}$  level with  $S_1$  closed.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF021621

# Am27S191/S191A/S191SA/PS191/PS191A

## Am27S291/S291A/S291SA/PS291/PS291A

16,384-Bit (2048x8) Bipolar PROM



### DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts — enhances reliability through total system heat reduction (27PS devices)
- Plug in replacement for industry standard product — no board changes required
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Rapid recovery from power-down state provides minimum delay (27PS devices)

### GENERAL DESCRIPTION

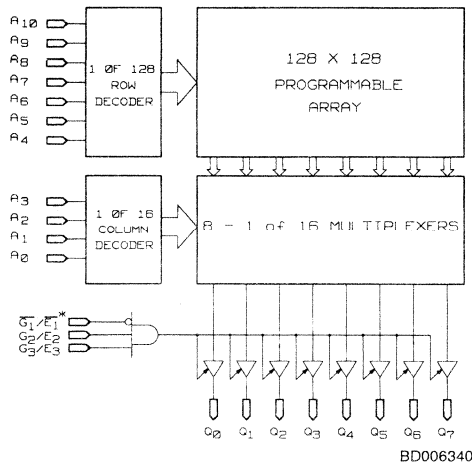
The Am27S191 (2048 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs which are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic

replacement. Easy word-depth expansion is facilitated by both active LOW ( $\bar{G}_1$ ) and active HIGH ( $G_2$  and  $G_3$ ) output enables.

This device is also available in 300-mil, lateral center DIP (Am27S291). Additionally, this device is offered in a power-switched, three-state version (Am27PS191/Am27PS291).

### BLOCK DIAGRAM

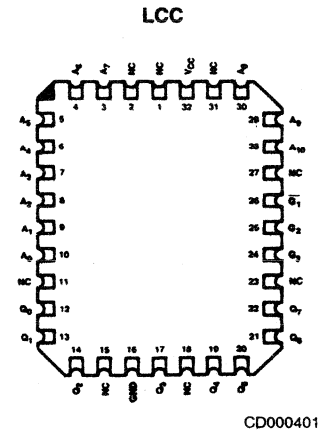
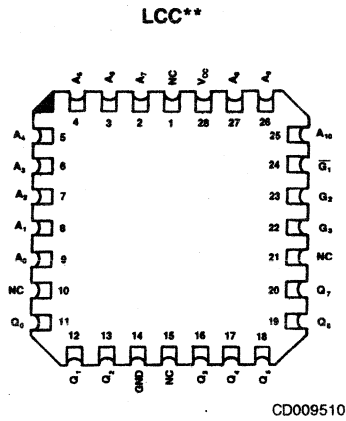
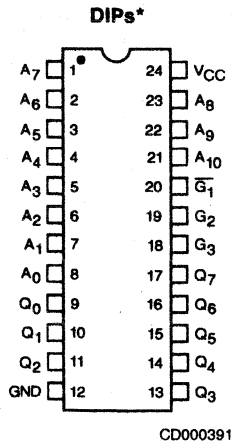


\*E nomenclature applies to the power-switched versions only (Am27PSXXX).

### PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S191SA, Am27S291SA		Am27S191A, Am27S291A		Am27S191, Am27S291		Am27PS191A, Am27PS291A		Am27PS191, Am27PS291	
Address Access Time (ns)	25	30	35	50	50	65	50	65	65	75
Operating Range	C	M	C	M	C	M	C	M	C	M

## CONNECTION DIAGRAMS Top View

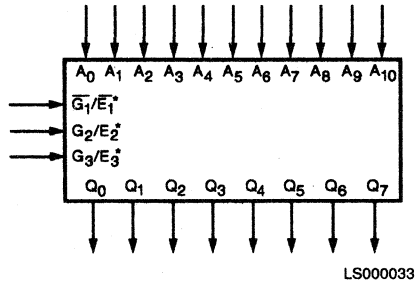


\*Also available in a 24-pin Flatpack.  
Pinout identical to DIPs.

\*\*Also available in a 28-pin Square PLCC. Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



\*E nomenclature applies to the power-switched versions only (Am27PSXXX).

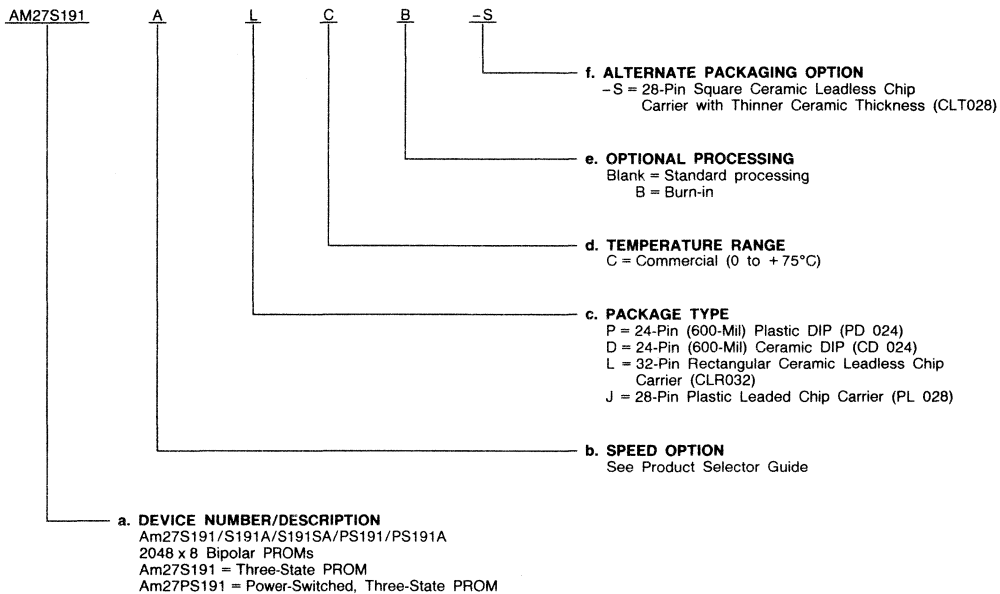
## ORDERING INFORMATION

(Am27S191/27PS191)

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**
- f. **Alternate Packaging Option**



Valid Combinations	
AM27S191	PC, PCB, DC, DCB, LC, LCB, LC-S, LCB-S, JC, JCB
AM27S191A	
AM27S191SA	
AM27PS191	
AM27PS191A	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.



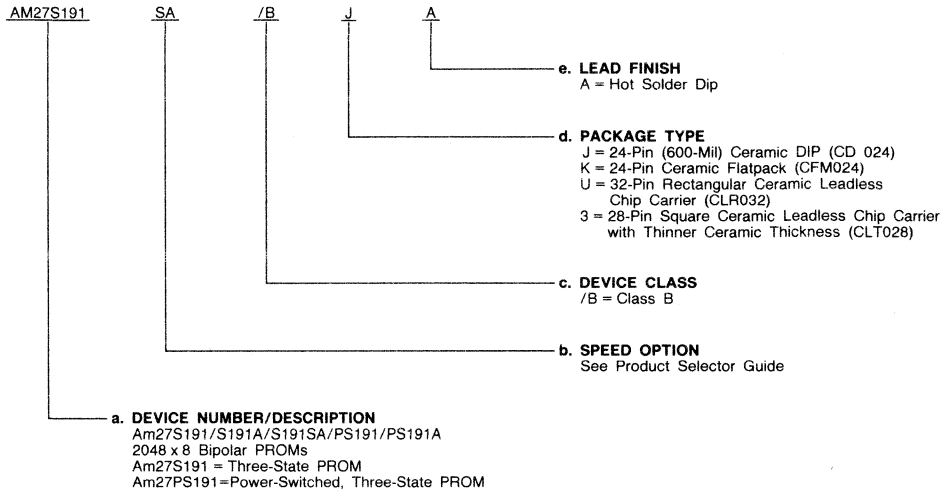
# MILITARY ORDERING INFORMATION

(Am27S191/27PS191)

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S191	/BJA, /BKA, /BUA, /B3A
AM27S191A	
AM27S191SA	
AM27PS191	
AM27PS191A	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

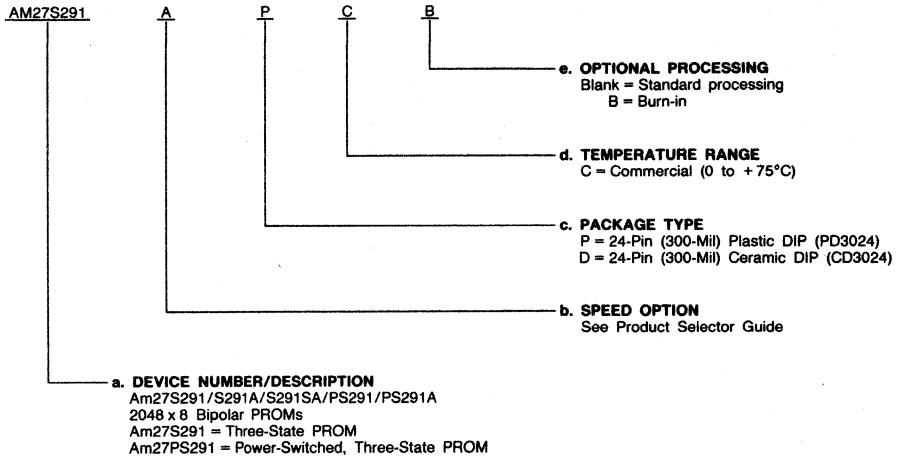
## ORDERING INFORMATION

(Am27S291/27PS291)

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM27S291	PC, PCB, DC, DCB
AM27S291A	
AM27S291SA	
AM27PS291	
AM27PS291A	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

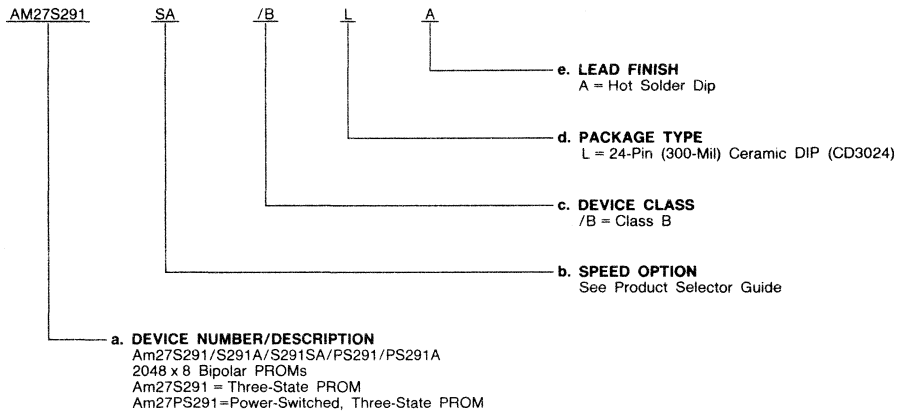
## MILITARY ORDERING INFORMATION

(Am27S291/27PS291)

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM27S291	/BLA
AM27S291A	
AM27S291SA	
AM27PS291	
AM27PS291A	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups  
 1, 2, 3, 7, 8, 9, 10, 11.

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

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## PIN DESCRIPTION

### **A<sub>0</sub> – A<sub>10</sub> Address Inputs (Input)**

The 11-bit field presented at the address inputs selects one of 2048 memory locations to be read from.

### **Q<sub>0</sub> – Q<sub>7</sub> Data Output Port (Output)**

The outputs whose state represents the data read from the selected memory locations.

### **$\overline{G}_1, G_2, G_3$ Output Enable (Input)**

Provides direct control of the Q-output buffers. Outputs disabled forces all open-collector outputs to an "OFF" state

and all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G}_1 \cdot G_2 \cdot G_3$$

$$\begin{aligned} \text{Disable} &= \overline{G}_1 \cdot G_2 \cdot G_3 \\ &= G_1 + \overline{G}_2 + \overline{G}_3 \end{aligned}$$

### **V<sub>CC</sub> Device Power Supply Pin**

The most positive of the logic power supply pins.

### **GND Device Power Supply Pin**

The most negative of the logic power supply pins.

---

## FUNCTIONAL DESCRIPTION

### Notes on Power Switching

The Am27PS191 and Am27PS291 are power-switched devices. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I<sub>CC</sub> is reduced to less than half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS191 and Am27PS291 are selected, a current surge is placed on the V<sub>CC</sub> supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 24 to pin 12 at each device. (See Figure 1.)
2. Address access time (TAVQV) can be optimized if a chip enable set-up time (TEVAV) of greater than 25ns is observed. Negative set-up times on chip enable (TEVAV < 0) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming) .....	-0.5 V to +V <sub>CC</sub> Max.
DC Voltage Applied to Outputs During Programming .....	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec) .....	250 mA
DC Input Voltage .....	-0.5 V to +5.5 V
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +75°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub> (Note 1)	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.50	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V			-0.250	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>			40	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 1)		COM'L -20 MIL -15	-90 -90	mA
I <sub>CC</sub>	Power Supply Current	All inputs = GND, V <sub>CC</sub> = Max.			185	mA
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-1.2	V
I <sub>CEX</sub>	Output Leakage Current	V <sub>CC</sub> = Max. V <sub>GT</sub> = 2.4 V		V <sub>O</sub> = V <sub>CC</sub> V <sub>O</sub> = 0.4 V	40 -40	μA
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 2) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		4.0		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 2) V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		8.0		

- Notes: 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.  
 2. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.  
 3. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

5

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

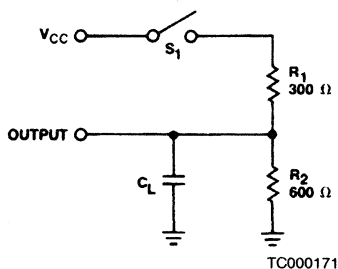
No.	Parameter Symbol	Parameter Description	Version	Am27S Version		Am27PS Version		Unit
				COM'L	MIL	COM'L	MIL	
				Max.	Max.	Max.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time	SA	25	30			ns
			A	35	50	50	65	
			STD	50	65	65	75	
2	TGVQZ TEVQZ	Delay from Output Enable Valid to Output Hi-Z	SA	18	20			ns
			A	25	30	25	30	
			STD	25	30	35	45	
3	TGVQV TEVQV	Delay from Output Enable Valid to Output Valid	SA	18	20			ns
			A	25	30	65	75	
			STD	25	30	80	90	
4	TAVQV1	Power-Switched Address Valid to Output Valid Access Time (Am27PS Versions only)	A			65	75	ns
			STD			80	90	

See also Switching Test Circuits.

- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.  
 2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels.  
 3. TAVQV is tested with switch S<sub>1</sub> closed and C<sub>L</sub> = 50 pF.  
 4. TGVQV is tested with C<sub>L</sub> = 50 pF to the 1.5 V level; S<sub>1</sub> is open for high impedance to HIGH tests and closed for high impedance to LOW tests. TGVQZ is tested with C<sub>L</sub> = 5 pF. HIGH to high impedance tests are made with S<sub>1</sub> open to an output voltage of steady state HIGH -0.5 V with S<sub>1</sub> open; LOW-to-HIGH impedance tests are made to the steady state LOW +0.5 V level with S<sub>1</sub> closed.






\*Subgroups 7 and 8 apply to functional tests.

**SWITCHING TEST CIRCUIT**

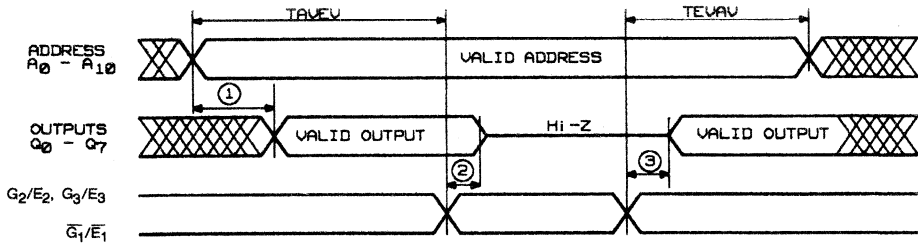


# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF021572

# 53/63RA1681/A

2048 x8 High Performance

Registered PROM with Asynchronous Enable



Advanced  
Micro  
Devices

## FEATURES/BENEFITS

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNY DIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16mA I<sub>OL</sub> output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

## APPLICATIONS

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™)  
11 Inputs, 8 Registered Outputs, 2048 product terms

## GENERAL DESCRIPTION

The 53/63RA1681 and 53/63RA1681A are 2Kx8 PROMs with on-chip "D"-type registers, output enable control through an asynchronous enable input, and flexible start-up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous enable ( $\bar{E}$ ) is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing.

Memory expansion and data control are made flexible with asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting  $\bar{E}$  to a HIGH.

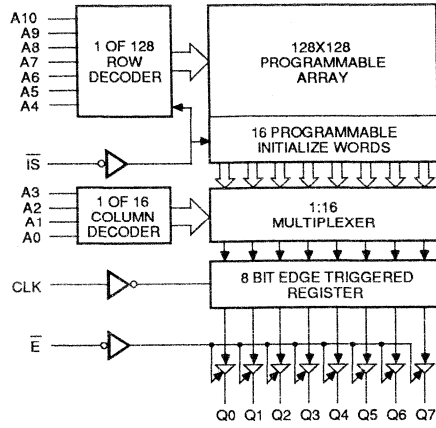
The flexible initialization feature allows start-up and time-out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ( $\bar{IS}$ ) pin LOW, one of the sixteen column words (A3–A0) will be set in the output registers independent of the row addresses (A9–A4). With all  $\bar{IS}$  column words (A3–A0) programmed to the same pattern, the  $\bar{IS}$  function will be independent of both row and column addressing and may be used as a single pin control. With all  $\bar{IS}$  words programmed HIGH, a PRE-SET function is performed. The unprogrammed state of  $\bar{IS}$  words is LOW, presenting a CLEAR with  $\bar{IS}$  pin LOW.

## SELECTION GUIDE

Memory		Package		Performance	Part Number	
Size	Organization	Pins	Type		0°C to +75°C	-55°C to +125°C
16K	2048x8	24 (28)	CD 3024 PD 3024 PL 028 CL 028 CFM 024	Enhanced	63RA1681A	53RA1681A
				Standard	63RA1681	53RA1681

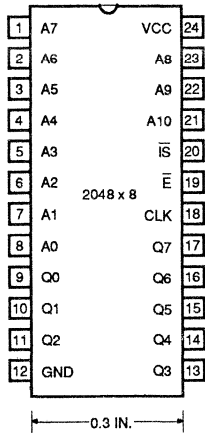


# BLOCK DIAGRAM

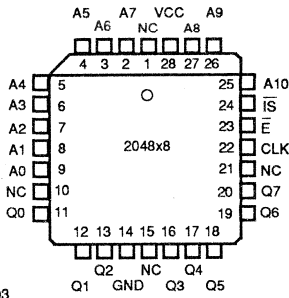


1315 01

# PIN CONFIGURATIONS

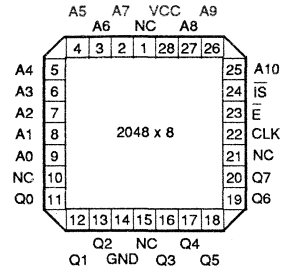


1315 02



1315 03

Plastic Chip Carrier



1315 04

Leadless Chip Carrier

## ABSOLUTE MAXIMUM RATINGS

	Operating	Programming
Supply voltage $V_{CC}$ .....	-0.5 to 7 V	12 V
Input voltage .....	-1.5 to 7 V	7 V
Input current .....	-30 mA to +5 mA	
Off-state output voltage .....	-0.5 V to 5.5 V	12 V
Storage temperature .....	-65°C to +150°C	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect reliability. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

## OPERATING CONDITIONS

Symbol	Parameter	Military†				Commercial				Unit	
		Typ.†	53RA1681A		53RA1681		63RA1681A		63RA1681		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.		Max.
$t_w$	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_s(\overline{IS})$	Setup time from $\overline{IS}$ to clock	20	30		35		25		30		ns
$t_h(A)$	Hold time address to clock	-5	0		0		0		0		ns
$t_h(\overline{IS})$	Hold time ( $\overline{IS}$ )	-5	0		0		0		0		ns
$V_{CC}$	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
$T_A$	Operating temperature*	25	-55	125	-55	125	0	75	0	75	°C

\* This is defined as the instant-on case temperature.

† Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

**Electrical Characteristics** Over Operating Conditions. For APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted.

Symbol	Parameter	Test Conditions		Min.	Typ.†	Max.	Unit	
$V_{IL}$	Low-level input voltage**					0.8	V	
$V_{IH}$	High-level input voltage**			2.0			V	
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.2	V	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	$\mu\text{A}$	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$			0.5	V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	Com	$I_{OH} = -3.2 \text{ mA}$	2.4		V	
			Mil	$I_{OH} = -2 \text{ mA}$				
$I_{OZL}$	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$				-40	$\mu\text{A}$
$I_{OZH}$			$V_O = 2.4 \text{ V}$				40	
$I_{OS}$	Output short-circuit current*	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$		-20		-90	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ . All inputs TTL. All outputs open.				140	185	mA

**Switching Characteristics** Over Operating Conditions (See standard test load). For APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted. ††

Symbol	Parameter	Typ.†	Military				Commercial				Unit
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CLK}$	Clock to output Delay	10		20		25		15		20	ns
$t_{EA}$	Enable to output access time ( $\bar{E}$ )	15		30		35		25		30	ns
$t_{ER}$	Disable to output recovery time ( $\bar{E}$ )	15		30		35		25		30	ns

\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

\*\*  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

† Typicals at 5.0 V  $V_{CC}$  and 25°C  $T_A$ .

†† Subgroups 7 and 8 apply to Functional tests.



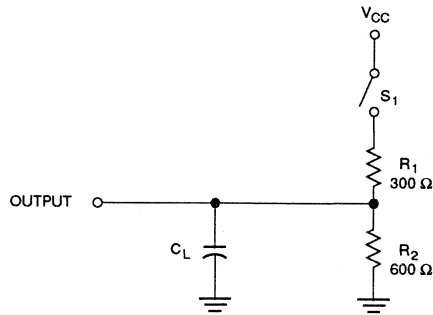


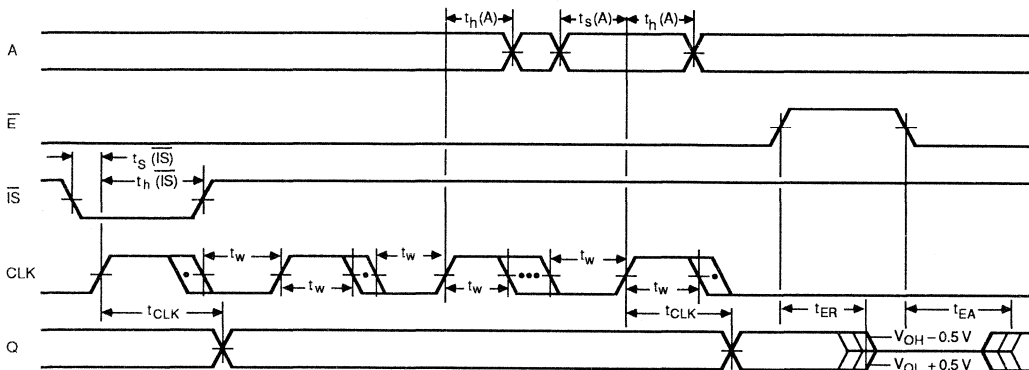
Figure 1. Switching Test Load

1315 06

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

1314 07

Figure 2. Definition of Timing Diagrams



- NOTES:
1. INPUT PULSE AMPLITUDE 0 V TO 3.0 V.
  2. INPUT RISE AND FALL TIMES 2–5 ns FROM 0.8 V TO 2.0 V.
  3. INPUT ACCESS MEASURED AT THE 1.5 V LEVEL.
  4. SWITCH  $S_1$  CLOSED,  $C_L = 30$  pF AND MEASURED AT 1.5 V OUTPUT LEVEL FOR ALL TESTS EXCEPT  $t_{EA}$  AND  $t_{ER}$ .
  5.  $t_{EA}$  IS MEASURED AT THE 1.5 V OUTPUT LEVEL WITH  $C_L = 30$  pF.  $S_1$  IS OPEN FOR HIGH IMPEDANCE TO "1" TEST, AND CLOSED FOR HIGH IMPEDANCE TO "0" TEST.  
 $t_{ER}$  IS TESTED WITH  $C_L = 5$  pF.  $S_1$  IS OPEN FOR "1" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OH} - 0.5$  V OUTPUT LEVEL,  $S_1$  IS CLOSED FOR "0" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OL} + 0.5$  V OUTPUT LEVEL.

Figure 3. Definition of Waveforms

1315 05



# 53/63RS881/A

High Performance 1024x8 Registered PROM

## FEATURES/BENEFITS

- Edge triggered "D" registers
- Synchronous and asynchronous enables
- Versatile 1:16 initialization words
- 8-Bit-wide in 24-pin SKINNYDIP® package for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA IOL output drive capability
- Reliable titanium-tungsten fuses (TIW), with programming yields typically greater than 98%

## APPLICATIONS

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™) 10 inputs, 8 Registered Outputs, 1024 product terms

## DESCRIPTION

The 53/63RS881 and 53/63RS881A are 1Kx8 PROMs with on-chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start-up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ( $\bar{E}$ ) and synchronous ( $\bar{ES}$ ) enables are LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting  $\bar{E}$  to a HIGH or if  $\bar{ES}$  is HIGH when the rising clock edge occurs. When  $V_{CC}$  power is first ap-

plied, the synchronous enable flip-flop will be in the set condition, causing the outputs to be in the high-impedance state.

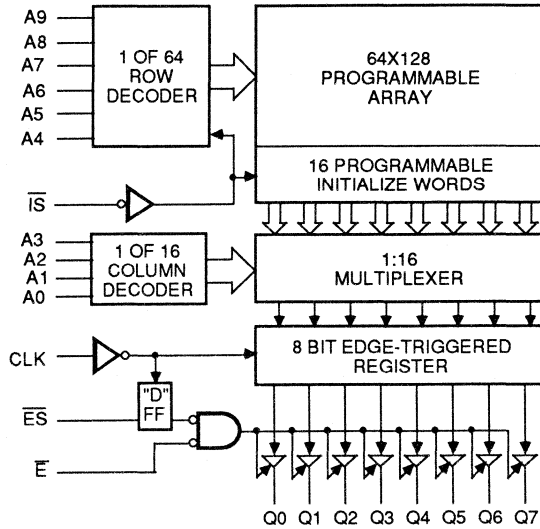
The flexible initialization feature allows start-up and time-out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ( $\bar{IS}$ ) pin LOW, one of the sixteen column words ( $A_3$ – $A_0$ ) will be set in the output registers independent of the row addresses ( $A_9$ – $A_4$ ). The unprogrammed state of  $\bar{IS}$  words are LOW, presenting a CLEAR with  $\bar{IS}$  pin LOW. With all  $\bar{IS}$  column words ( $A_3$ – $A_0$ ) programmed to the same pattern, the  $\bar{IS}$  function will be independent of both row and column addressing and may be used as a single pin control. With all  $\bar{IS}$  words programmed HIGH, a PRESET function is performed.

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## SELECTION GUIDE

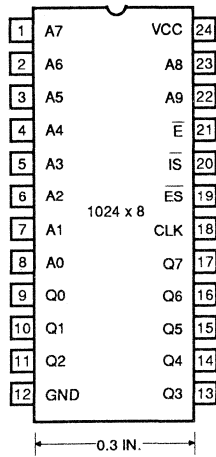
Memory		Package		Performance	Part Number	
Size	Organization	Pins	Type		0°C to +75°C	–55°C to +125°C
8K	1024x8	24 (28)	CD 3024 PD 3024 PL 028 CL 024 CFM 024	Enhanced	63RS881A	53RS881A
				Standard	63RS881	53RS881

## BLOCK DIAGRAM

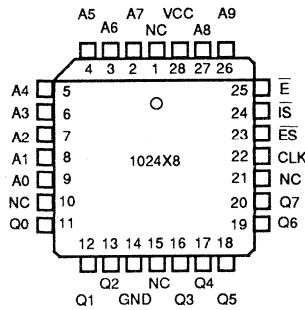


1316 01

## PIN CONFIGURATIONS

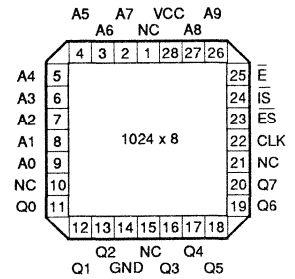


1316 02



Plastic Chip Carrier

1316 03



Leadless Chip Carrier

1316 04

## ABSOLUTE MAXIMUM RATINGS

### Operating Programming

Supply voltage $V_{CC}$ .....	-0.5 V to 7 V .....	12 V
Input voltage .....	-1.5 V to 7 V .....	7 V
Input current .....	-30 mA to +5 mA	
Off-state output voltage .....	-0.5 V to 5.5 V .....	12 V
Storage temperature .....	-65°C to +150°C	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect reliability. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

## Operating Conditions

Symbol	Parameter	Typ†	Military††				Commercial				Unit
			53RS881A		53RS881		63RS881A		63RS881		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_w$	Width of clock (High or Low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	25	40		45		30		35		ns
$t_{s(\overline{ES})}$	Setup time from $\overline{ES}$ to clock	8	15		15		15		15		ns
$t_{s(\overline{IS})}$	Setup time from $\overline{IS}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	-5	0		0		0		0		ns
$t_{h(\overline{ES})}$	Hold time ( $\overline{ES}$ )	-3	5		5		5		5		ns
$t_{h(\overline{IS})}$	Hold time ( $\overline{IS}$ )	-5	0		0		0		0		ns
$V_{CC}$	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
$T_A$	Operating temperature*	25	-55	125	-55	125	0	75	0	75	°C

\* This is defined as the instant-on case temperature.\*

† Typicals at 5.0 V  $V_{CC}$  and 25°C  $T_A$ .

†† Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

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**Electrical Characteristics** Over Operating Conditions. For APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted.

Symbol	Parameter	Test Conditions		Min	Typ†	Max	Unit	
$V_{IL}$	Low-level input voltage**					0.8	V	
$V_{IH}$	High-level input voltage**			2.0			V	
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.2	V	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	$\mu\text{A}$	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$			0.5	V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	Com	$I_{OH} = -3.2 \text{ mA}$	2.4		V	
			Mil	$I_{OH} = -2 \text{ mA}$				
$I_{OZL}$	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$				-40	$\mu\text{A}$
			$V_O = 2.4 \text{ V}$				40	
$I_{OS}$	Output short-circuit current*	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$			-20		mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ . All inputs TTL. All outputs open.				130	180	mA

\* Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

\*\*  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

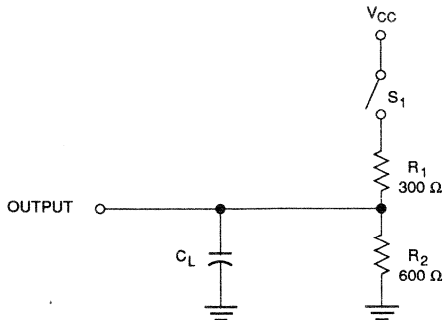
† Typicals at 5.0 V  $V_{CC}$  and 25°C  $T_A$ .

**Switching Characteristics** Over Operating Conditions and using Standard Test Load. For APL Products, Group A, subgroups 9, 10, 11 are tested unless otherwise noted.††

Symbol	Parameter	Typ†	Military				Commercial				Unit
			53RS881A		53RS881		63RS881A		63RS881		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CLK}$	Clock to output Delay	10		20		25		15		20	ns
$t_{ESA}$	Clock to output access time ( $\overline{ES}$ )	18		30		35		25		30	ns
$t_{ESR}$	Clock to output recovery time ( $\overline{ES}$ )	17		30		35		25		30	ns
$t_{EA}$	Enable to output access time ( $\overline{E}$ )	18		30		35		25		30	ns
$t_{ER}$	Disable to output recovery time ( $\overline{E}$ )	17		30		35		25		30	ns

†† Subgroups 7 and 8 apply to Functional tests.





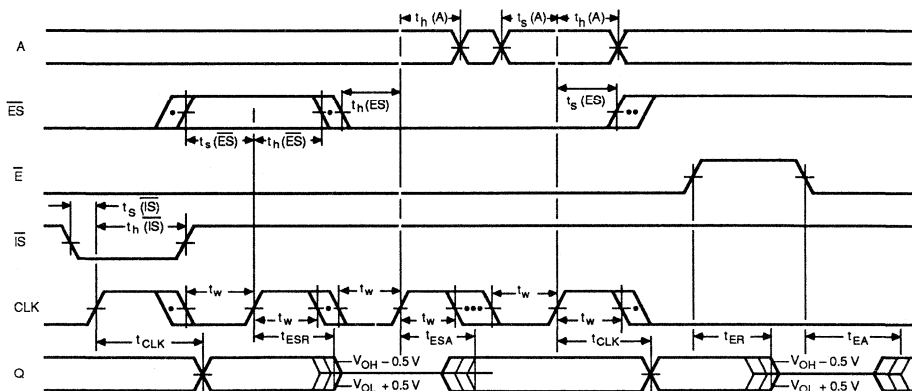
1316 05

Figure 1. Switching Test Load

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

1316 06

Figure 2. Definition of Timing Diagrams



- NOTES:
1. INPUT PULSE AMPLITUDE 0 V TO 3.0 V.
  2. INPUT RISE AND FALL TIMES 2-5 ns FROM 0.8 V TO 2.0 V.
  3. INPUT ACCESS MEASURED AT THE 1.5 V LEVEL.
  4.  $t_{AA}$  IS TESTED WITH SWITCH  $S_1$  CLOSED,  $C_L = 30$  pF AND MEASURED AT 1.5 V OUTPUT LEVEL.
  5.  $t_{EA}$  AND  $t_{ESA}$  ARE MEASURED AT THE 1.5 V OUTPUT LEVEL WITH  $C_L = 30$  pF.  $S_1$  IS OPEN FOR HIGH IMPEDANCE TO "1" TEST, AND CLOSED FOR HIGH IMPEDANCE TO "0" TEST.

$t_{ER}$  AND  $t_{ESR}$  ARE TESTED WITH  $C_L = 5$  pF.  $S_1$  IS OPEN FOR "1" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OH} - 0.5$  V OUTPUT LEVEL;  $S_1$  IS CLOSED FOR "0" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OL} + 0.5$  V OUTPUT LEVEL.

1316 07

Figure 3. Definition of Waveforms

# 53/63RS1681/A

2048x8 High Performance  
Registered PROM with Synchronous Enable



## FEATURES/BENEFITS

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA  $I_{OL}$  output drive capability
- Reliable titanium-tungsten fuses (TIW), with programming yields typically greater than 98%

## APPLICATIONS

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™) 11 inputs, 8 Registered Outputs, 2048 product terms

## GENERAL DESCRIPTION

The 53/63RS1681 and 53/63RS1681A are 2Kx8 PROMS with on-chip "D" type registers, versatile output enable control through synchronous enable inputs and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the synchronous ( $\overline{ES}$ ) enable is low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous enable inputs. Outputs may be set to the high impedance state by setting  $\overline{ES}$  HIGH before the rising clock edge occurs. When  $V_{CC}$  power is first

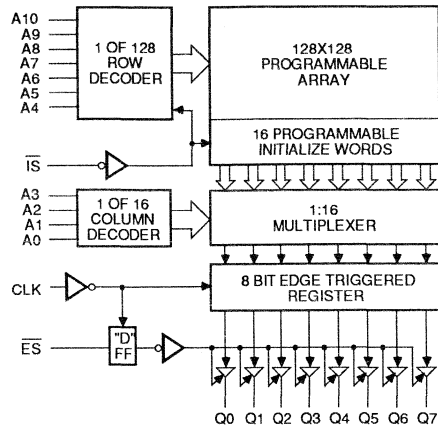
applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ( $\overline{IS}$ ) pin LOW, one of the 16 column words (A3–A0) will be set in the output registers independent of the row addresses (A10–A4). With all  $\overline{IS}$  column words (A3–A0) programmed to the same pattern, the  $\overline{IS}$  function will be independent of both row and column addressing and may be used as a single pin control. With all  $\overline{IS}$  words programmed HIGH a PRESET function is performed. The unprogrammed state of  $\overline{IS}$  words are LOW, presenting a CLEAR with  $\overline{IS}$  pin LOW.

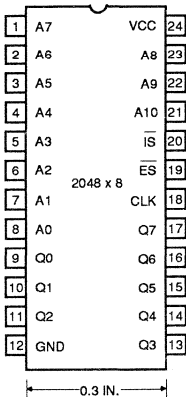
## SELECTION GUIDE

Memory		Package		Performance	Part Number	
Size	Organization	Pins	Type		0°C to +75°C	–55°C to +125°C
16K	2048x8	24 (28)	CD 3024 PD 3024 PL 028 CL 028 CFM 024	Enhanced	63RS1681A	53RS1681A
				Standard	63RS1681	53RS1681

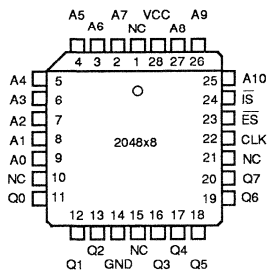
## BLOCK DIAGRAM



## PIN CONFIGURATIONS

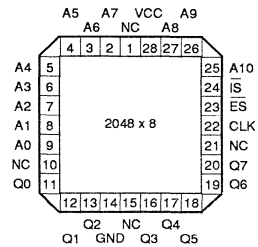


1317 01



Plastic Chip Carrier

1317 03



Leadless Chip Carrier

1317 02

## ABSOLUTE MAXIMUM RATINGS

	Operating	Programing
Supply voltage $V_{CC}$ .....	-0.5 V to 7 V	12 V
Input voltage .....	-1.5 V to 7 V	7 V
Input current .....	-30 mA to +5 mA	
Off-state output voltage .....	-0.5 V to 5.5 V	12 V
Storage temperature.....	-65°C to +150°C	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect reliability. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

## Operating Conditions

Symbol	Parameter	Typ†	Military †				Commercial				Unit
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_w$	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{ES})}$	Setup time from $\overline{ES}$ to clock	7	15		15		15		15		ns
$t_{s(\overline{IS})}$	Setup time from $\overline{IS}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	-5	0		0		0		0		ns
$t_{h(\overline{ES})}$	Hold time ( $\overline{ES}$ )	-3	5		5		5		5		ns
$t_{h(\overline{IS})}$	Hold time ( $\overline{IS}$ )	-5	0		0		0		0		ns
$V_{CC}$	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
$T_A$	Operating temperature*	25	-55	125	-55	125	0	75	0	75	°C

\* This is defined as the instant-on case temperature

† Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

**Electrical Characteristics** Over Operating Conditions. For APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted.

Symbol	Parameter	Test Conditions		Min	Typ†	Max	Unit	
$V_{IL}$	Low-level input voltage**					0.8	V	
$V_{IH}$	High-level input voltage**			2.0			V	
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.2	V	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA	
$I_{IH}$	High level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	$\mu\text{A}$	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$			0.5	V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	Com	$I_{OH} = -3.2 \text{ mA}$	2.4		V	
			Mil	$I_{OH} = -2 \text{ mA}$				
$I_{OZL}$	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$			-40	$\mu\text{A}$	
$I_{OZH}$			$V_O = 2.4 \text{ V}$			40		
$I_{OS}$	Output short-circuit current*	$V_{CC} = 5\text{V}$	$V_O = 0 \text{ V}$		-20	-90	mA	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ . All inputs TTL. All outputs open.				140	185	mA

**Switching Characteristics** Over Operating Conditions and Using Standard Test Load. For APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted.††

Symbol	Parameter	Typ†	Military				Commercial				Unit
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CLK}$	Clock to output delay	10		20		25		15		20	ns
$t_{ESA}$	Clock to output access time (ES)	15		30		35		25		30	ns
$t_{ESR}$	Clock to output recovery time (ES)	15		30		35		25		30	ns

\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

\*\*  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

† Typicals at 5.0 V  $V_{CC}$  and 25°C  $T_A$ .

†† Subgroups 7 and 8 apply to Functional tests.

**5**

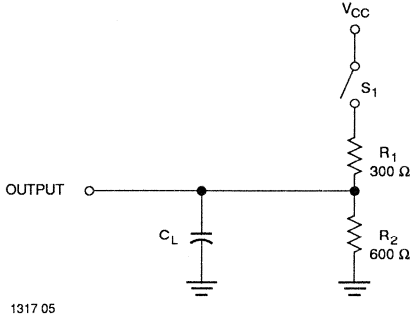
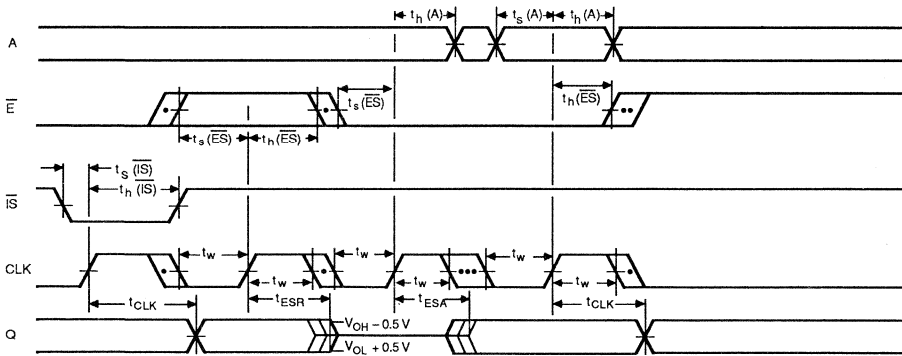


Figure 1. Switching Test Load

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

1317 07

Figure 2. Definition of Timing Diagrams



- NOTES:
1. INPUT PULSE AMPLITUDE 0 V TO 3.0 V.
  2. INPUT RISE AND FALL TIMES 2–5 ns FROM 0.8 V TO 2.0 V.
  3. INPUT ACCESS MEASURED AT THE 1.5 V LEVEL.
  4. SWITCH  $S_1$  CLOSED,  $C_L = 30$  pF AND MEASURED AT 1.5 V OUTPUT LEVEL FOR ALL TESTS EXCEPT  $t_{ESA}$  AND  $t_{ESR}$ .
  5.  $t_{ESA}$  IS MEASURED AT THE 1.5 V OUTPUT LEVEL WITH  $C_L = 30$  pF.  $S_1$  IS OPEN FOR HIGH IMPEDANCE TO "1" TEST, AND CLOSED FOR HIGH IMPEDANCE TO "0" TEST.  
 $t_{ESR}$  IS TESTED WITH  $C_L = 5$  pF.  $S_1$  IS OPEN FOR "1" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OH} - 0.5$  V OUTPUT LEVEL;  $S_1$  IS CLOSED FOR "0" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OL} + 0.5$  V OUTPUT LEVEL.

Figure 3. Definition of Waveforms



# 53/63S281/A

High Performance 256x8 PROM TiW PROM Family

## FEATURES/BENEFITS

- 28-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Three-state outputs

## APPLICATIONS

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 8 Inputs, 8 Outputs, and 256 product terms

## GENERAL DESCRIPTION

The 53/63S281/A are 256x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## PROGRAMMING

The 53/63S281/A PROMs are programmed with the same programming algorithm as all other Advanced

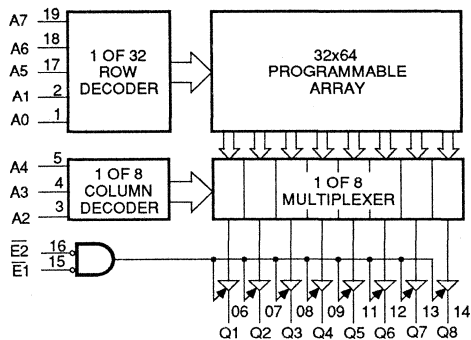
Micro Devices generic TiW PROMs. For details contact the factory.

## SELECTION GUIDE

Memory			Package		Performance	Part Number	
Size	Organization	Output	Pins	Type		0°C to +75°C	-55°C to +125°C
32K	4096x8	TS	24 (28)	CD 024	Standard	63S3281	53S3281
				PD 024			
				CFM 024			
				PL 028	Enhanced	63S3281A	53S3281A
				CL 028			
					Super Speed	—	53S3281B

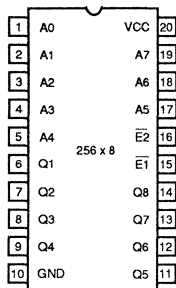
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## BLOCK DIAGRAM DIP Pinout

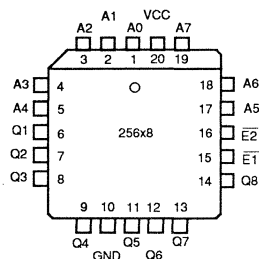


1313 03

## PIN CONFIGURATIONS



1313 01



Plastic Chip Carrier

1313 02

Note: LCC pinout identical to PLCC.



## ABSOLUTE MAXIMUM RATINGS

	Operating	Programming
Supply voltage $V_{CC}$ .....	-0.5 V to 7 V	12 V
Input voltage .....	-1.5 V to 7 V	7 V
Input current .....	-30 mA to +5 mA	
Off-state output voltage .....	-0.5 V to 5.5 V	12 V
Storage temperature .....	-65°C to +150°C	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect reliability. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

## Operating Conditions

Symbol	Parameter	Military†			Commercial			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$T_A$	Operating temperature*	-55		125	0		75	°C

\* This is defined as the instant-on case temperature.

† Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

**DC Electrical Characteristics** Over Operating Conditions. For APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted.

Symbol	Parameter	Test Conditions		Min.	Typ.†	Max	Unit	
$V_{IL}$	Low-level input voltage**					0.8	V	
$V_{IH}$	High-level input voltage**			2			V	
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.5	V	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	μA	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$	Com		0.45	V	
				Mil		0.5		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	Com	$I_{OH} = -3.2 \text{ mA}$	2.4		V	
			Mil	$I_{OH} = -2 \text{ mA}$				
$I_{OZL}$	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$			-40	μA	
$I_{OZH}$			$V_O = 2.4 \text{ V}$			40		
$I_{OS}$	Output short-circuit current*	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$		-20	-90	mA	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ . All inputs grounded. All outputs open.				90	140	mA

\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

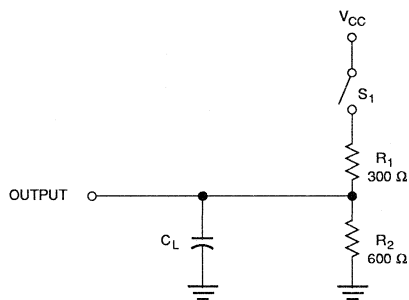
\*\*  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

**Switching Characteristics** Over Operating Conditions (See standard test load). For APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted.††

Operating Conditions	Device Type	$t_{AA}$ (ns) Address Access Time		$t_{EA}$ AND $t_{ER}$ (ns) Enable Access Time Recovery Time		Unit
		Typ.†	Max.	Typ.†	Max.	
Commercial	63S281A	21	28	18	25	ns
	63S281	21	45	18	25	
Military	53S281A	21	40	18	30	
	53S281	21	50	18	30	

† Typicals at 5.0 V  $V_{CC}$  and 25°C  $T_A$ .

†† Subgroups 7 and 8 apply to Functional tests.



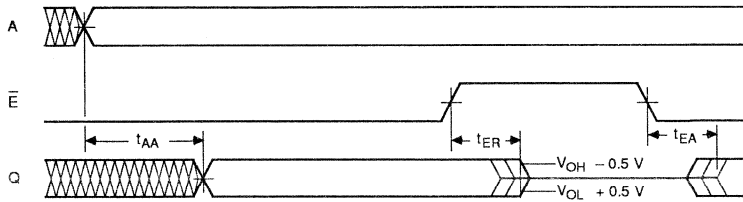
1313 06

Figure 3. Switching Test Load

WAVEFORM	INPUTS	OUTPUTS
	DONT CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

1313 07

Figure 4. Definition of Timing Diagram



- NOTES:
1. INPUT PULSE AMPLITUDE 0 V TO 3.0 V.
  2. INPUT RISE AND FALL TIMES 2-5 ns FROM 0.8 V TO 2.0 V.
  3. INPUT ACCESS MEASURED AT THE 1.5 V LEVEL.
  4.  $t_{AA}$  IS TESTED WITH SWITCH  $S_1$  CLOSED.  $C_L = 30$  pF AND MEASURED AT 1.5 V OUTPUT LEVEL.
  5.  $t_{EA}$  IS MEASURED AT THE 1.5 V OUTPUT LEVEL WITH  $C_L = 30$  pF.  $S_1$  IS OPEN FOR HIGH IMPEDANCE TO "1" TEST, AND CLOSED FOR HIGH IMPEDANCE TO "0" TEST.  
 $t_{ER}$  IS TESTED WITH  $C_L = 5$  pF.  $S_1$  IS OPEN FOR "1" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OH} - 0.5$  V OUTPUT LEVEL;  
 $S_1$  IS CLOSED FOR "0" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OL} + 0.5$  V OUTPUT LEVEL.

1313 08

Figure 5. Definition of Waveforms



# 53/63S881/A

High Performance 1024x8 PROM TiW PROM Family

## FEATURES/BENEFITS

- 30-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low voltage generic programming
- PNP inputs for low input current
- Three state outputs
- 24-pin SKINNYDIP® or 600-mil DIP package

## APPLICATIONS

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 10 Inputs, 8 Outputs and 1024 product terms

## GENERAL DESCRIPTION

The 53/63S881 and 53/63S881A are 1024x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and three state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## PROGRAMMING

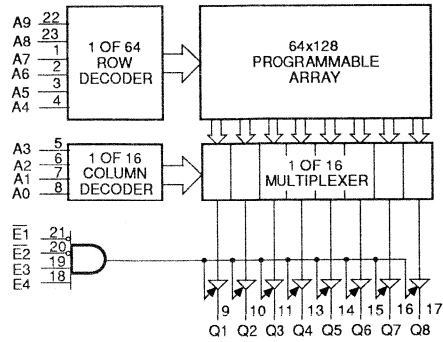
The 53/63S881 and 53/63S881A PROMs are programmed with the same programming algorithm as all

other Advanced Micro Devices generic TiW PROMs. For details contact the factory.

## SELECTION GUIDE

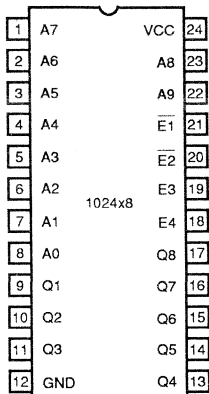
Memory			Package		Performance	Part Number	
Size	Organization	Output	Pins	Type		0°C to +75°C	-55°C to +125°C
8K	1024x8	TS	24 (28)	CD 3024	Enhanced	63S881A	53S881A
				PD 3024			
8K	1024x8	TS	24 (28)	CD 024	Standard	63S881	53S881
				PD 024			
				CFM 024			
				CL 028			
				PL 028			

## BLOCK DIAGRAM DIP Pinout



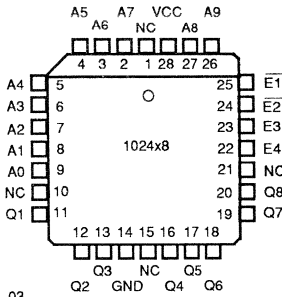
1314 01

## PIN CONFIGURATIONS



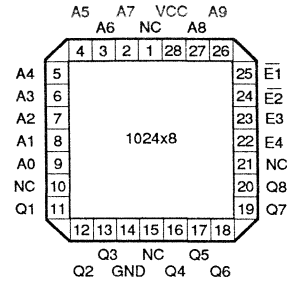
0.3 IN.  
OR  
0.6 IN.

1314 02



1314 03

Plastic Chip Carrier



1314 04

Leadless Chip Carrier

## ABSOLUTE MAXIMUM RATINGS

	Operating	Programming
Supply voltage $V_{CC}$ .....	-0.5 V to 7 V	12 V
Input voltage .....	-1.5 V to 7 V	7 V
Input current .....	-30 mA to +5 mA	
Off-state output voltage .....	-0.5 V to 5.5 V	12 V
Storage temperature .....	-65°C to +150°C	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect reliability. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

## OPERATING CONDITIONS

Symbol	Parameter	Military†			Commercial			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$T_A$	Operating temperature*	-55		125	0		75	°C

\* This is defined as the instant-on case temperature.

† Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

**DC Electrical Characteristics** Over Operating Conditions. For APL Products, Subgroups 1, 2, 3 are tested unless otherwise noted.

Symbol	Parameter	Test Condition		Min.	Typ.†	Max.	Unit	
$V_{IL}$	Low-level input voltage**					0.8	V	
$V_{IH}$	High-level input voltage**			2			V	
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.5	V	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	μA	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$	Com		0.45	V	
				Mil		0.5		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	Com	$I_{OH} = -3.2 \text{ mA}$	2.4		V	
			Mil	$I_{OH} = -2 \text{ mA}$				
$I_{OZL}$	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$			-40	μA	
$I_{OZH}$			$V_O = 2.4 \text{ V}$			40		
$I_{OS}$	Output short-circuit current*	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$		-20	-90	mA	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ . All inputs grounded. All outputs open.				92	160	mA

\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

\*\*  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

**Switching Characteristics** Over Operating Conditions (See standard test load). For APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted.\*\*

Operating Conditions	Device Type	$t_{AA}$ (ns) Address Access Time		$t_{EA}$ and $t_{ER}$ (ns) Enable Access Time Recovery Time		Unit
		Typ†	Max	Typ†	Max	
Commercial	63S881A	26	30	18	25	ns
	63S881	26	45	18	30	
Military	53S881A	26	45	18	30	
	53S881	26	55	18	35	

† Typical at 5.0 V  $V_{CC}$  and 25°C  $T_A$ .

†† Subgroups 7 and 8 apply to functional tests.

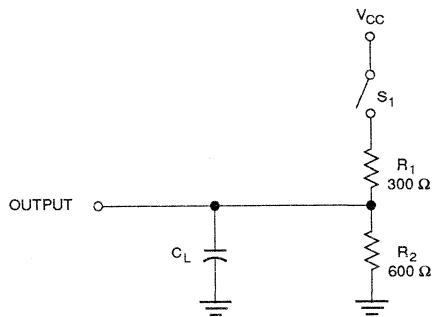


Figure 1 Switching Test Load

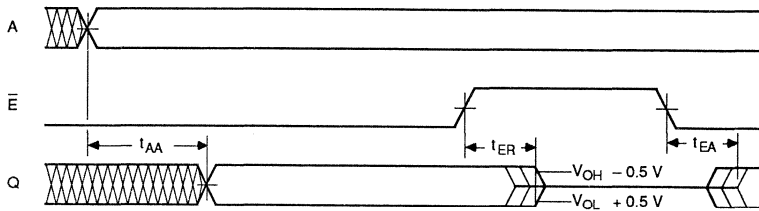
1314 07

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WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

1314 08

Figure 2 Definition of Timing Diagram



- NOTES:
1. INPUT PULSE AMPLITUDE 0 V TO 3.0 V.
  2. INPUT RISE AND FALL TIMES 2-5 ns FROM 0.8 V TO 2.0 V.
  3. INPUT ACCESS MEASURED AT THE 1.5 V LEVEL.
  4.  $t_{AA}$  IS TESTED WITH SWITCH  $S_1$  CLOSED,  $C_L = 30$  pF AND MEASURED AT 1.5 V OUTPUT LEVEL.
  5.  $t_{EA}$  IS MEASURED AT THE 1.5 V OUTPUT LEVEL WITH  $C_L = 30$  pF.  $S_1$  IS OPEN FOR HIGH IMPEDANCE TO "1" TEST, AND CLOSED FOR HIGH IMPEDANCE TO "0" TEST.
- $t_{ER}$  IS TESTED WITH  $C_L = 5$  pF.  $S_1$  IS OPEN FOR "1" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OH} - 0.5 V$  OUTPUT LEVEL;  $S_1$  IS CLOSED FOR "0" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OL} + 0.5 V$  OUTPUT LEVEL.

1314 09

Figure 3 Definition of Waveforms





# 53/63S3281/A 53S3281B

High Performance 4096 x 8 PROM TiW PROM Family

## FEATURES/BENEFITS

- 35-ns maximum access time
- 32768-bit memory
- Reliable titanium-tungsten fuses (TiW) with programming yields typically greater than 98%
- PNP inputs for low input current

## APPLICATIONS

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 12 Inputs, 8 Outputs and 4096 product terms

## GENERAL DESCRIPTION

The 53/63S3281 is a high-speed 4Kx8 PROM which uses industry standard package and pin out.

The family features low-input current PNP inputs, full Schottky clamping, and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry

and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## PROGRAMMING

The 53/63S3281 PROM is programmed with the same programming algorithm as all other Advanced Micro

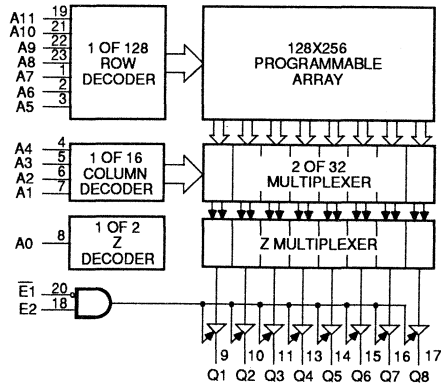
Devices generic TiW PROMs. For details contact the factory.

## SELECTION GUIDE

Memory			Package		Performance	Part Number	
Size	Organization	Output	Pins	Type		0°C to +75°C	-55°C to +125°C
2K	256x8	TS	20	CD 020	Enhanced	63S281A	53S281A
				PD 020			
				CF 020	Standard	63S281	53S281
				CL 020			
				PL 020			

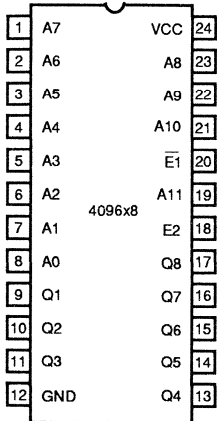
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# BLOCK DIAGRAM Dip Pinout

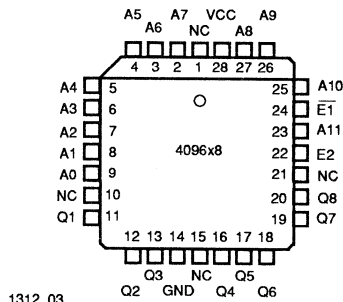


1312 01

## PIN CONFIGURATIONS

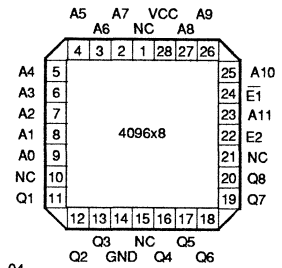


1312 02



1312 03

Plastic Chip Carrier



1312 04

Leadless Chip Carrier

## ABSOLUTE MAXIMUM RATINGS

	Operating	Programming
Supply voltage $V_{CC}$ .....	-0.5 V to 7 V	12 V
Input voltage .....	-1.5 V to 7 V	7 V
Input current .....	-30 mA to +5 mA	
Off-state output voltage .....	-0.5 V to 5.5 V	12 V
Storage temperature .....	-65°C to +150°C	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect reliability. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

## OPERATING CONDITIONS

Symbol	Parameter	Military†			Commercial			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$T_A$	Operating temperature*	-55		125	0		75	°C

\* This is defined as the instant-on case temperature.\*

† Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

**Electrical Characteristics** Over Operating Conditions. For APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted.

Symbol	Parameter	Test Condition		Min	Typ†	Max	Unit
$V_{IL}$	Low-level input voltage**					0.8	V
$V_{IH}$	High-level input voltage**			2			V
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.5	V
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	μA
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$	Com		0.45	V
				Mil		0.5	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	Com	$I_{OH} = -3.2 \text{ mA}$	2.4		V
			Mil	$I_{OH} = -2 \text{ mA}$			
$I_{OZL}$	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$				μA
$I_{OZH}$			$V_O = 2.4 \text{ V}$				
$I_{OS}$	Output short-circuit current*	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$		-20	-90	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ . All inputs grounded. All outputs open.			150	190	mA

\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

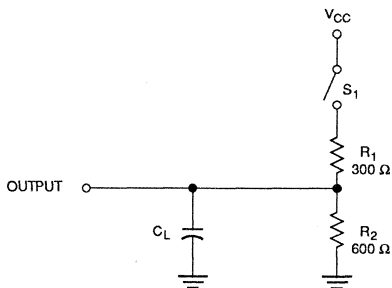
\*\*  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

**Switching Characteristics** Over Operating Conditions (See standard test load). For APL products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted.††

Operating Conditions	Device Type	$t_{AA}$ (ns) Address Access Time		$t_{EA}$ and $t_{ER}$ (ns) Enable Access time Recovery time		Unit
		Typ†	Max	Typ†	Max	
Commercial	63S3281A	26	35	18	30	ns
	63S3281	26	45	18	30	
Military	53S3281B	26	40	18	35	
	53S3281A	26	50	18	35	
	53S3281	26	60	18	35	

† Typicals at 5.0 V  $V_{CC}$  and 25°C  $T_A$ .

†† Subgroups 7 and 8 apply to functional tests.



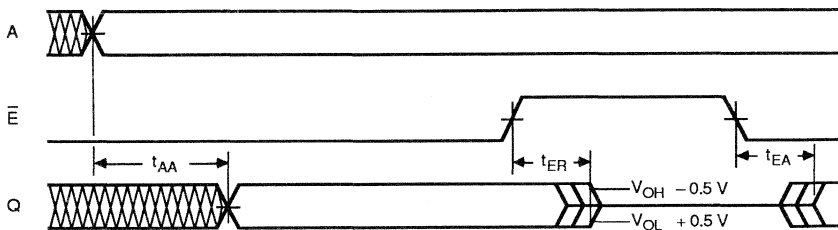
1312 07

Figure 1. Switching Test Load

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

1312 08

Figure 2. Definition of Timing Diagram



- NOTES:
1. INPUT PULSE AMPLITUDE 0 V TO 3.0 V.
  2. INPUT RISE AND FALL TIMES 2-5 ns FROM 0.8 V TO 2.0 V.
  3. INPUT ACCESS MEASURED AT THE 1.5 V LEVEL.
  4.  $t_{AA}$  IS TESTED WITH SWITCH  $S_1$  CLOSED.  $C_L = 30$  pF AND MEASURED AT 1.5 V OUTPUT LEVEL.
  5.  $t_{EA}$  IS MEASURED AT THE 1.5 V OUTPUT LEVEL WITH  $C_L = 30$  pF.  $S_1$  IS OPEN FOR HIGH IMPEDANCE TO "1" TEST, AND CLOSED FOR HIGH IMPEDANCE "0" TEST.
- $t_{ER}$  IS TESTED WITH  $C_L = 5$  pF.  $S_1$  IS OPEN FOR "1" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OH} - 0.5 V$  OUTPUT LEVEL;  $S_1$  IS CLOSED FOR "0" TO HIGH IMPEDANCE TEST, MEASURED AT  $V_{OL} + 0.5 V$  OUTPUT LEVEL.

1312 09

Figure 3. Definition of Waveforms

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# Testing High-Performance Bipolar Memory

## INTRODUCTION

During the last several years, the state-of-the art of TTL compatible bipolar memory integrated circuits has advanced very rapidly. Device complexity has increased dramatically not only in terms of the memory storage capacity but also by the addition of new on-chip functions such as the inclusion of output data registers. Simultaneously, advances in bipolar LSI design and manufacturing technology have generated significant improvements in the performance levels of bipolar memory. Similarly, the complexity and performance levels of systems which employ these devices have grown. The concomitant growth of system complexity has placed additional demands on both the device manufacturer and the user's incoming inspection area to assure the performance capabilities of each component before it is assembled into the system.

Several test equipment manufacturers now supply sophisticated, computer controlled testers for these inspection tasks. Most of this equipment is inherently capable of the millivolt and nanosecond accuracies which are required; most memory testers can generate the complex waveforms and test patterns needed. However, the details of applying this equipment to a specific test problem, including the problem of interfacing the tester to the device-under-test, are usually left to the user. The purpose of this application note is to discuss several problems which are frequently encountered when testing high performance bipolar memory devices, and to acquaint the user with how such problems may be identified, measured and corrected.

## WHAT MAKES A MEMORY GOOD?

Before discussing the specifics of bipolar memory testing problems, it is important to understand the basic characteristics which these devices should exhibit. Clearly each device must meet all product specification parameters but, first and foremost, a bipolar memory should be fast! Address access time (delay from address input to data output), enable access time and enable recovery time should be as small as possible. High performance is often the primary reason for using bipolar memory. Similarly, the performance of the ideal bipolar memory should remain relatively constant with changes in supply voltage, ambient temperature and output load capacitance. Fast devices, offering stable performance over a broad range of conditions, permit the user to qualify a smaller number of part types; one fast device can accommodate many standard as well as high performance applications. Such devices provide added safety margin for the system design, permit simplification of system test and debug and assure trouble-free system performance in the field. Hence the "best" memory is a fast, stable device which not only meets a given user specification, but also offers the extra performance needed for a broad range of applications.

Advanced Micro Devices offers a family of bipolar Random Access Memories (RAMs) and Programmable Read Only Memories (PROMs) which are designed to meet this idealized definition as closely as possible. First, each AMD device is designed to meet a "military design goal." This means AMD bipolar memories are designed to provide the extra margins and higher output drive capabilities needed to assure proper performance over the extended military supply voltage and

operating temperature ranges. This often necessitates the use of more advanced design techniques such as on-chip regulators, temperature and voltages compensation networks and feedback circuits. Second, AMD has conceived and developed an advanced, oxide separated, ion implanted manufacturing process called IMOX™. Developed specifically for the production of high density bipolar memories, this technology provides both high density and excellent performance in a truly reliable and manufacturable process. This combination of advanced design and fabrication technologies assures the military user of receiving components which are intended for his application while providing the commercial user with the extra margins, performance advantages and procurement benefits mentioned above.

## THE SYSTEM ENVIRONMENT

To understand the problems of high-performance memory testing, it is helpful to understand the electrical environment in which the memory devices will actually operate, i.e., the typical system environment. The system designer must address and resolve several critically important questions if the system is to consistently perform to its design specifications. These questions include:

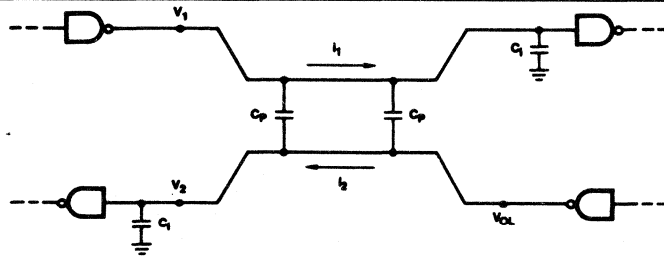
1. What noise voltages can the system's logic and memory devices tolerate?
2. What are the sources of system noise?
3. What can be done to control and minimize this noise?

The first question is answered relatively easily. The magnitude of noise which can be tolerated relates directly to the worst case noise immunity specified for the logic family. Noise immunity is simply the difference between the worst case output levels ( $V_{OH}$  and  $V_{OL}$ ) of the driving circuit and the worst case input voltage requirements ( $V_{IH}$  and  $V_{IL}$ , respectively) of the receiving circuit. For TTL devices the worst case noise immunity is typically 400mV for both the high and low logic levels.

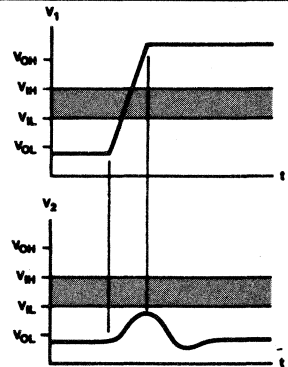
If "system noise" is defined as the sum of things which subtract from this noise immunity, several sources can be identified. A few of the most important sources found in a digital, TTL system are listed below:

- **Cross-Talk:** The desire to pack system components as tightly as possible inevitably causes signal wires or PC board traces to be placed in close proximity. The lead-to-lead capacitance and mutual inductance thus created (see Figure 1) causes "noise" voltages to appear when adjacent signal paths switch.
- **Transmission Line Reflections:** Like it or not, every signal path in the system has transmission line characteristics. TTL signal paths are usually not designed as transmission lines, with predictable and uniform characteristic impedances. This is partly because of the higher costs implied for multilayer PC boards with internal ground planes, termination resistors, etc. It is also the result of TTL logic's limited ability to drive the low impedance lines provided by current PC board technologies. Hence, TTL signal paths do exhibit the ringing and reflection problems associated with improperly terminated transmission lines. These reflections subtract from the available noise immunity as shown in Figure 2.

## Testing High-Performance Bipolar Memory

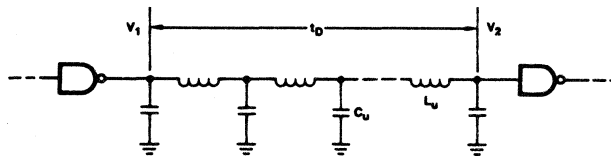


As  $V_1$  switches,  $I_1$  flows to charge the input capacitance  $C_i$ .  $I_2$  flows as a result of mutual inductance. The  $V_1$  voltage change is also coupled directly to  $V_2$  through the parasitic line-to-line capacitances,  $C_p$ .

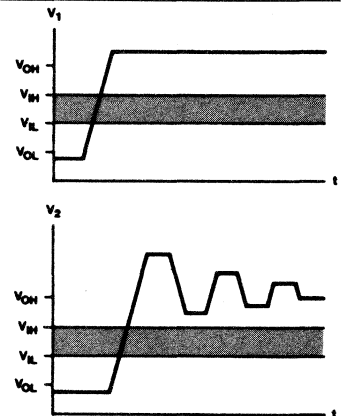


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Figure 1. An Example of Cross-Talk

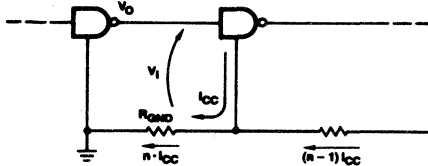


The unit length capacitance and inductance ( $C_u$  and  $L_u$ ) give each system connection transmission line characteristics. Without a matched termination, switching at  $V_1$  causes reflection voltages to appear at  $V_2$ , reducing noise immunity.



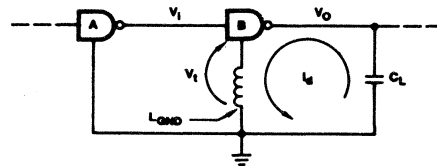
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Figure 2. Line Reflections



$$V_i = V_0 - (n \cdot I_{CC}) R_{GND}$$

a) DC Ground "Noise"



DG000030

When  $V_i$  goes HIGH,  $V_0$  goes LOW discharging  $C_L$ . The discharge current  $I_d$  flows through the ground inductance  $L_{GND}$ , creating a transient voltage  $V_t$ . The input voltage seen by gate B is actually  $V_i - V_t$ .

b) Transient Ground Noise

Figure 3.

● **Ground Network Noise:** Most high-performance systems employ large numbers of high-performance ICs. These devices typically draw large  $I_{CC}$  currents from the power supply. Cumulatively, these currents can reach several amperes per board. Such currents, flowing in the ground network, cause non-negligible DC voltage drops to occur; not all device ground pins are at zero volts. Since the output

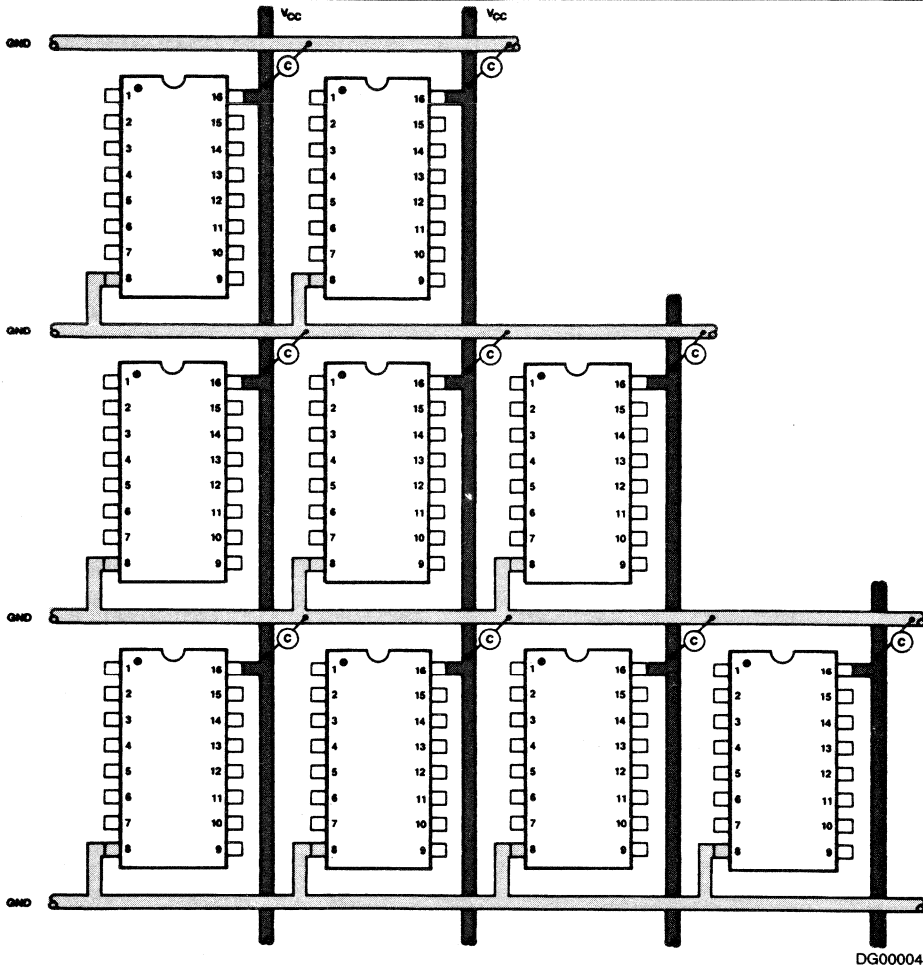
levels and the input thresholds of each TTL device reference the local ground (Figure 3a), these drops also subtract from the available noise immunity. Additional noise margin losses occur each time the device outputs switch. This occurs because large currents must flow to rapidly charge and discharge the interconnect and input capacitances which load each output. These charging currents flow in a loop



(Figure 3b) through the ground network which is normally a simple interconnection of wires, each with some value of resistance and inductance per unit length. Some additional resistive drops occur. But, the rapid changes in these currents (large  $di/dt$ ), occurring as charging starts and stops, mean a transient ground noise voltage is also generated. This voltage obeys the law of  $v = L(di/dt)$  where  $L$  is the ground circuit inductance and  $di/dt$  is the rate of change of the charging currents. Notice that adding local bypass capacitors can only reduce this voltage by paralleling the

ground inductance with the  $V_{CC}$  network inductance. Bypassing cannot eliminate this problem because these capacitors shunt the devices and not the ground and  $V_{CC}$  network inductances where the noise is generated.

Controlling and minimizing noise in a digital system becomes more challenging as the system performance requirements increase. These requirements demand devices capable of short propagation delays, e.g., ultra-fast memories with excellent drive characteristics to minimize fully loaded access times.



DG000040

Note: Transient ground current flow in four directions from each device ground: right and left on the ground bus; up and down the  $V_{CC}$  bus after passing through the local bypass capacitor, C. Equivalent ground inductance is very low.

Figure 4. Example of an AC Ground Mesh

Since noise margin violations result in system malfunctions, the system designer must define a set of rules governing the physical construction techniques to be used within the system. These rules address a host of considerations including power distribution, AC grounding, lead placement, line termination requirements, logic loading (fan in and fan out) and interconnect delays. Specifying these rules is a complex process of making appropriate cost-performance tradeoffs.

For a medium to high performance system, these rules might specify arranging devices in an array with  $V_{CC}$  power traces running vertically up the columns while ground metal running horizontally between the rows. Inserting bypass capacitors at each grid intersection forms an AC ground mesh (Figure 4), limiting the amount of ground inductance at each array site. If limits are also placed on the total capacitance each device may drive (cumulative interconnect and input capacitance on

## Testing High-Performance Bipolar Memory

all outputs), the total charging currents may be controlled thus limiting the noise immunity eroded by ground circuit noise. Similarly, the distance between adjacent traces and the maximum length of unterminated lines may be specified to control noise immunity losses caused by cross-talk and termination mismatches. Ultra-high performance systems may require additional measures; e.g., multilayer boards with true

### THE MEMORY TEST ENVIRONMENT

Ideally the test system hardware and fixtures would be designed to even more stringent rules than those used for the system. This is reasonable as the tester is the standard employed for accepting or rejecting components used in the system. Because a collection of additional objectives constrain the test environment, designing test hardware to equally or more stringent rules is usually impractical.

Memory testers must test many types of components under a variety of conditions. Tests performed include DC parametric tests, functional and AC tests with complex test patterns and margin tests to assure device operation at the extremes of applied conditions and supply voltage. To accomplish this, connections to sets of programmable input drivers and output receivers (comparators), multiple device bias and power supplies, relays to permit connection of the DC parametric test unit, and special load circuits must all converge at the test site.

To provide flexibility and facilitate repair, test hardware must be modular. This requirement dictates placing the hardware (drivers, receivers, etc.) on many small PC boards which then must talk to the DUT (device under test) through additional wiring and connectors.

Frequently the quantity of parts tested necessitates mating an automatic device handler to the tester. Handlers also provide capabilities for testing at temperature extremes when needed. The DUT must be tested inside this equipment, requiring still more wiring between the test head and the actual test site.

ground planes or increased usage of line drivers and receivers. Though the preceding descriptions have been simplified, it should be clear that distances between driving and receiving devices, the quantity and distribution of load capacitance, as well as the AC ground network integrity are all essential elements of the system design.

Ideally, all test hardware would be located immediately adjacent to the test site to minimize cross-talk, reflections and ground noise. However, this objective must be compromised to address the other objectives and constraints outlined above. Techniques commonly employed in making this compromise are illustrated in Figure 5. Notice that DUT drivers are remote from the test site, driving signal to the DUT through "series terminated" transmission lines. Similarly the receivers are some distance from the test site, receiving signals from the DUT through a series of connectors and wires which can degrade the signal. Most annoying of all, the test site ground connection has been compromised. This signal path must carry heavy transient and DC currents during test and should provide a very solid, low impedance reference against which all AC and DC tests are made. Accumulating resistance and inductance in this path jeopardizes the integrity of all test results.

Hence, the electrical environment provided at the test site is generally inferior to the actual system environment where the memory component will be used.

### TEST RELATED PROBLEMS AND SOLUTIONS

Accurately measuring or verifying memory performance in the test system environment requires a recognition of its inherent limitations. Outlined below are five problem areas commonly encountered when testing high-performance bipolar memories. Methods of identifying and alleviating these problems are indicated.

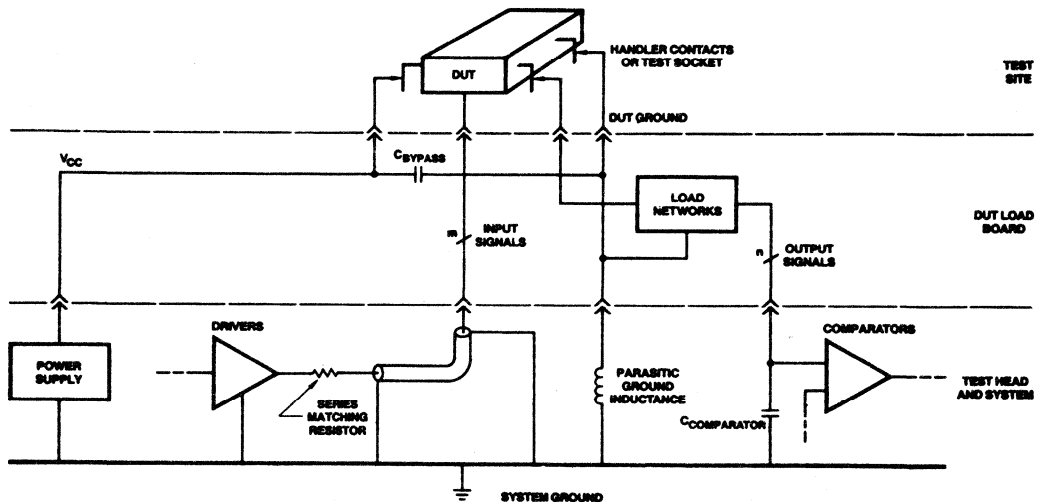


Figure 5. The Test System Environment

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● **Contending with Ground Noise:** Ground noise is one of the most common and troublesome test problems. As defined above, ground noise is caused by switching currents flowing through the ground network impedance. Whereas the sys-

tem environment (Figure 4) may provide multiple low inductance ground paths into a ground mesh or plane, the tester provides one long, higher inductance path back to the test system ground (Figure 5). This path includes handler con-

## Testing High-Performance Bipolar Memory

tacts, connectors and the DUT load board, all of which increase ground inductance and resistance. Transient currents which result when the DUT switches can be enormous. Consider the case of a byte wide (8 output) memory functional test. At some point in the test sequence, all memory outputs will switch from high to low ( $V_{OH}$  to  $V_{OL}$ ) at the same instant, discharging all eight load capacitances simultaneously. If the input capacitance of the receiver is 40pF and the interconnect capacitance of the test fixture is 10pF, the total load capacitance driven by all device outputs would be 400pF. A fast memory device could discharge this load at a 1V/ns rate. The relationship  $i = C(dv/dt)$  implies peak charging currents of 400mA must flow through ground. As Figure 6 illustrates, this charging current does not build to its full value instantaneously. For a fast device the time required to go from zero to full charging current would approximate 2ns. A resultant ground current  $di/dt$  of 200mA/ns is implied. If the ground inductance is 1 nanohen-

ry (approximate inductance of 1 inch of straight, small gauge wire), then  $v = L(di/dt)$  predicts AC ground noise of 200mV. As you have probably guessed, the typical test site ground inductance exceeds 1nh. The path is longer and it is usually not a straight line connection. Actual tester ground noise of up to 800mV is common when testing high-performance byte wide memories. This noise can be measured easily with a high bandwidth oscilloscope by attaching the scope ground to the actual test system ground and monitoring the DUT ground pin with one channel.

Excessive ground noise creates several problems: First, this noise is capacitively coupled to the input drive signals through the DUT input capacitances; if large enough, DC coupling through the DUT input clamp diodes can occur (Figure 7). The DUT output levels are, of course, referenced to the DUT ground potential whereas the receiver board is referenced to test system ground, introducing inaccuracy in access time measurements, etc.

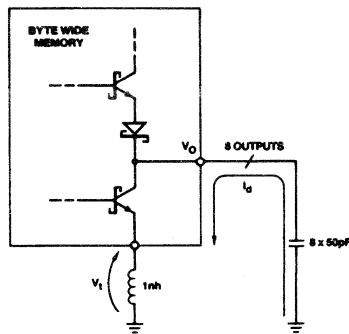
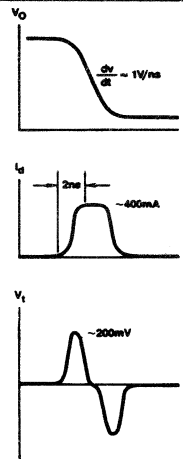


Figure 6. Byte Wide Memory Ground Transients



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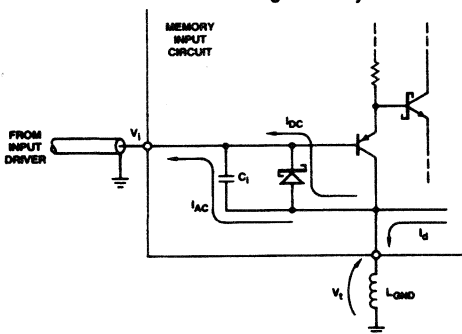
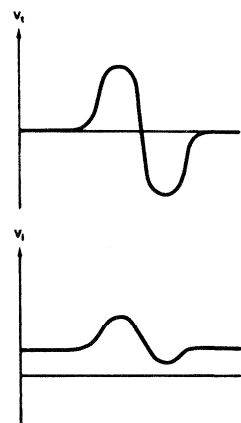


Figure 7. Ground Noise Coupling to the Inputs

For small magnitudes of noise,  $V_t$  noise is AC coupled to the inputs through the input capacitance,  $C_i$ . If  $V_i$  is low, large

positive values of  $V_t$  may momentarily forward bias the input clamp diode, creating a DC coupling.



DG000070

## Testing High-Performance Bipolar Memory

Worst of all, severe ground noise can make functional testing at or near the guaranteed input levels ( $V_{IH}$  and  $V_{IL}$ ) impossible. To demonstrate, assume the device ground noise reaches a positive 0.8V with respect to test system ground during output switching. Assume the input driver high level is programmed to 2.0V, minimum  $V_{IH}$  for most TTL devices. The actual voltage between a "high" DUT input and its ground is only 1.2V. The typical room temperature threshold voltage of a TTL device is 1.5V, and the device interprets 1.2V as a logic "low." This causes the memory to access a new memory location momentarily. The resultant momentary change in output data interferes with access time measurements. In severe cases, this momentary switching of output data creates additional ground noise which also feeds back to the inputs resulting in sustained oscillations. This noise interaction can also be viewed with a dual trace oscilloscope as shown in Figure 8. Channel A of the scope is connected to the address input while channel B monitors the DUT ground pin. The input voltage, as seen by the DUT, can be viewed directly by putting the scope in "A - B," algebraic subtract mode. Note the scope ground is connected to test system ground as before. Attaching scope ground to the DUT pin ground should be avoided as this creates a "ground loop." If connected this way, large noise currents flow in the alternate ground path provided by the scope back to earth ground; this interferes with the scope's ability to measure high-speed events and modifies the condition which is to be observed.

Several techniques can be employed to reduce ground noise problems:

- Keep the ground path as short as possible; use large diameter wire and "straight line" wiring techniques.
- Minimize the number of series connections in the DUT ground path; provide as many parallel ground connections as possible through each remaining connector.

- If the system uses a Kelvin (force - sense) ground system, terminate the system by shorting force to sense on the DUT load board. Kelvin systems provide DC accuracy, but their response times are much too slow to aid in the suppression of ground noise at the test site. Terminating Kelvin early sacrifices a little DC accuracy, but the ability to use the previous sense line as second, low impedance ground path usually improves the overall test accuracy.

- Provide multiple high frequency bypass capacitors as close as possible to the DUT, and again on the DUT load board. This allows the  $V_{CC}$  wiring to serve as an extra AC ground path for high frequency ground noise.

- Reduce the DUT load capacitance (receiver and interconnect capacitance) as much as possible; avoid using low values of load resistors. Both techniques reduce the transient currents, thus improving test accuracy. When necessary, DUT output drive capability can usually be verified with DC tests.

- If  $V_{IL}$  and  $V_{IH}$  tests are necessary, measure the maximum amount of ground noise that the specific device type to be tested generates in the actual test site. Set the input drive levels no tighter than " $V_{IH}$  plus the maximum noise" and " $V_{IL}$  minus the maximum noise." Using tighter limits over tests the device!

- Alternatively, use DC bench tests on a sample basis to verify that input margins are acceptable. This is a sound practice as the input thresholds of bipolar devices are extremely insensitive to fabrication process variations. Virtually any process variation or defect which would result in a threshold failure would also result in the catastrophic failure of other tests.

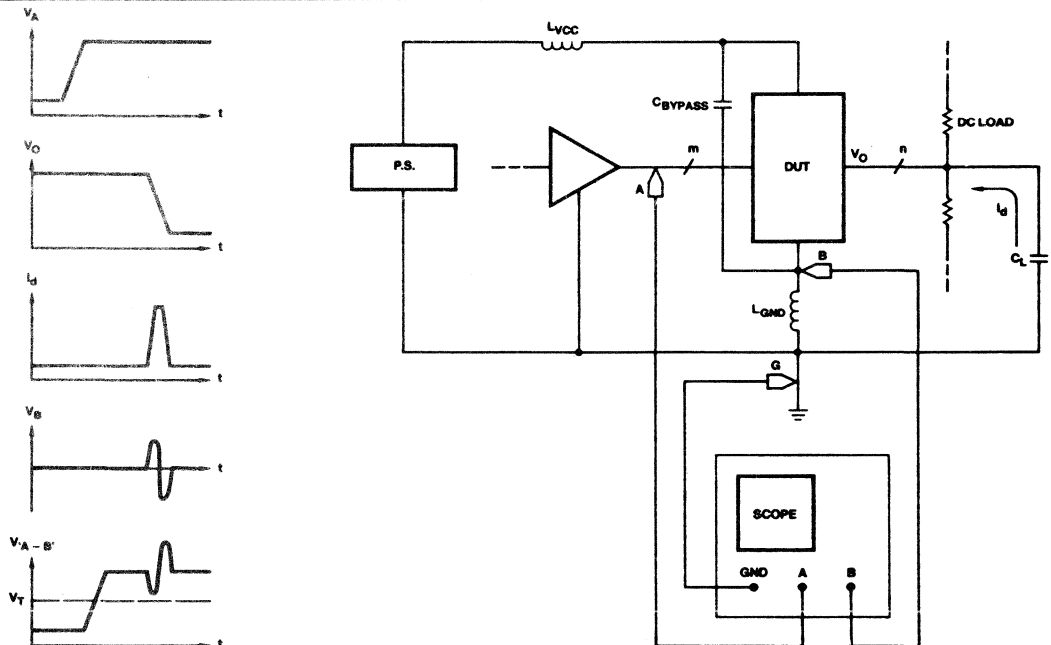


Figure 8. Monitoring Ground Noise

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## Testing High-Performance Bipolar Memory

– DC verification of  $V_{IL}$  and  $V_{IH}$  can also be performed on the test system, but care must be exercised to insure that input voltages NEVER cross through the 0.8V to 2.0V window; voltages residing in this window can cause the DUT to switch, triggering sustained oscillations.

- The Output "Tank Circuit": A second common problem encountered is resonance in the circuitry which connects the DUT outputs to the output comparators or receivers. This resonance occurs because the wire connecting the DUT outputs to the receivers is actually an inductor connected in series with the comparator input capacitance, forming a series resonant tank circuit (Figure 9). This load circuit is quite different from the typical loading situation found in a system environment. Notice that the capacitance in the tester tends to be a single large value of capacitance, lumped at the end of the DUT output drive line. The load capacitance in the system is generally smaller and it is distributed along the drive line; this configuration looks much more like a transmission line, with per unit length values of inductance and capacitance, than it does a resonant tank. The resonant frequencies found at the test site vary with wire length and capacitive load, but tend to be in the 100–500MHz range. The input voltage sensed by the receiver is actually the voltage at the center connection within the tank circuit, which can ring violently when the outputs switch; measurement errors of 5ns or more can occur. A good evaluation technique for this problem is to compare the waveforms observed at the output of the device with a "shmoo plot" of the output. Assuming a simple pattern is used, differences in these results may indicate a resonance problem.

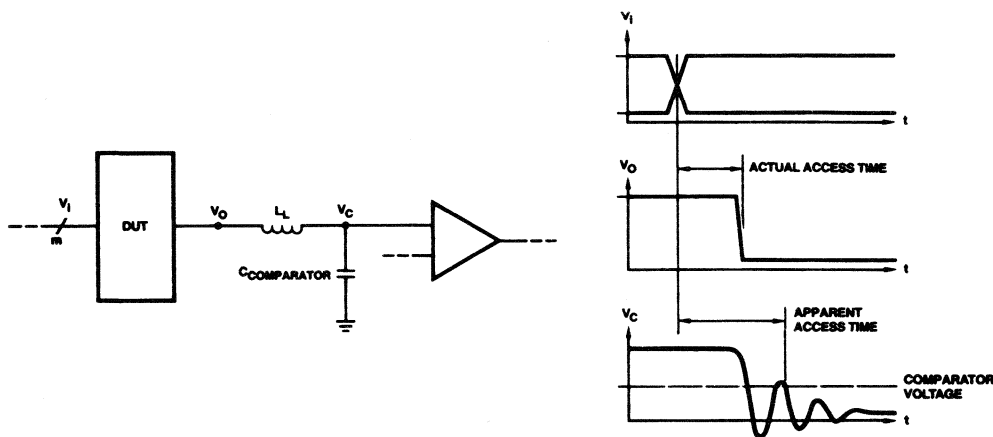
Corrective action for this problem includes:

- Use short, low inductance connections from the DUT output to the receiver; minimize comparator and intercon-

nect capacitance. Both techniques raise the resonant frequency of the tank circuit which limits the time measurement error and reduces the DUT's ability to stimulate ringing in the tank.

- Use twisted pair wiring techniques to connect DUT outputs to the receivers. Though this raises the capacitance slightly, it reduces the purely inductive character of the interconnect, usually tending to reduce ringing.
- Minimizing Cross-Talk: Cross-talk between the input and output lines of the DUT is also a common problem. Obviously, the greater the number of paths which must be packed into a given area, the greater the problem. The signal coupling that occurs adds noise to both the input lines, making  $V_{IH}$  and  $V_{IL}$  testing difficult, and output lines, reducing the accuracy of timing measurements. Techniques which tend to reduce cross-talk include the following:
  - Keep wires as short as possible and avoid laying wires on top of each other.
  - Reduce output loading to minimize the magnitude of current transients which could be coupled into adjacent lines.
  - Use twisted pair or coaxial cable wherever possible; take care to tie all grounds from these transmission lines together at both ends.
  - Use ground plane or ground mesh techniques in the load board and the handler interface if possible. A true ground plane permits the use "strip" transmission lines which not only minimize cross-talk, but also reduce ground noise.

Though expensive, ground plane techniques offer the test engineer a consistent reference voltage which can be used to identify and segregate the various components and sources of noise.



$L_L$ , the interconnect inductance and  $C_{COMPARATOR}$  form a series resonant tank circuit which can cause time measurement errors.

Figure 9. Resonance of the Outputs

### Conclusion

Advanced Micro Devices has invested significantly in the development of advanced, high-performance bipolar memory technologies and products. As the preceding discussion demonstrates, the memory tester presents a very different environment to the memory device than does the system. The

additional constraints placed on the tester virtually guarantee that devices which function in this "worst case" environment will perform satisfactorily in the system. However, this worst case environment may also selectively reject the best performing devices; i.e., those with the fastest access times and best drive characteristics. This occurs because high-perfor-

## Testing High-Performance Bipolar Memory

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mance devices magnify the problems found in the tester environment. The information presented here should aid the component engineer in recognizing and resolving these special test environment problems. Attention to these details will

reward the bipolar memory user by assuring acceptance of the best and broadest range of bipolar memories currently available.



ADVANCED MICRO DEVICES BIPOLAR PROMS

This report describes the technology used to manufacture AMD's family of Bipolar PROMs. This includes Standard PROMs from the 256 bit through the 128K level, Registered PROMs, and AMD's newest family — Diagnostic PROMs with Serial Shadow Register. Included is a discussion of the wafer fabrication in which an advanced, highly reliable platinum silicide fuse is utilized. A description of the major circuit elements and their testing is discussed as well as reliability testing and results.

AMD's families of Bipolar PROMs are manufactured in two highly advanced wafer fabrication areas located in San Antonio, Texas. One area manufactures PROMs on 5 inch diameter wafers which is very advanced for the industry. The other area is the world's first 6 inch bipolar wafer line. These two wafer fabrication areas will provide for the growing demand for Bipolar PROMs at very competitive costs for many years. In fact, AMD's commitment is to continue to be the leading supplier of Bipolar PROMs in both technology and service. Two distinct wafer fabrication processes are used — IMOX II and IMOX III. IMOX II is an advanced junction isolated process utilizing walled emitter transistors for very high speed circuits. Most circuits currently in production use the IMOX II process and it provides extremely high performance circuits with good yields. The IMOX III or "Slot" process utilizes a very narrow and deep silicon etch to create a slot in the silicon to isolate active component areas. This is the most advanced bipolar process available and will provide density and performance advantages unmatched by any other semiconductor technology available today or in the near future. Depending on density and performance requirements, most new Bipolar PROM products will be designed using the IMOX III process. The circuit design concepts are similar on each of the PROM products with the result that the products can be programmed using the same hardware. Only the socket adaptor required for

the PROM configuration and pin count is different. The same programming algorithm is used for all devices. The programming algorithm is also chosen to minimize programming time. The PROMs utilize a platinum Schottky diode structure with barrier metal. Dual layer metal is employed to maximize speed and minimize chip area. This applies to both the IMOX II and IMOX III process. All Advanced Micro Devices' circuits are screened to MIL-STD-883, Method 5004 class B or better, with burn-in as an option. Nearly all PROM products are on AMD's APL (approved product list) which means they meet all standard military requirements including package dimensions. AMD has also announced a new quality program called INTERNATIONAL STANDARD 500. While it is the objective to build quality into all PROM products toward an objective of zero defects, INT-STD-500 guarantees that lots shipped will not exceed a defect level of 500 parts per million.

The Process Technology

The IMOX™ II Process

THE IMOX II process is the next evolutionary step beyond the conventional bipolar Schottky process. This process utilizes platinum silicide fuses, ion implanted bases and emitters, oxide walled emitter structures, and dual layer metal. Platinum silicide continues to be the fuse material for several reasons. First, it has been demonstrated to be an extremely reliable fuse material. It does not exhibit the growback phenomenon common to nichrome technologies; it is not moisture sensitive in freeze-out tests; it is less fragile than nichrome and it does not have mass transport problems associated with moderate current densities. Second, the manufacturing process is easily controlled with regard to reliability factors and fusing currents. Third, the fuses are quite easy to form during the manufacturing process without a substantial number of additional processing steps.

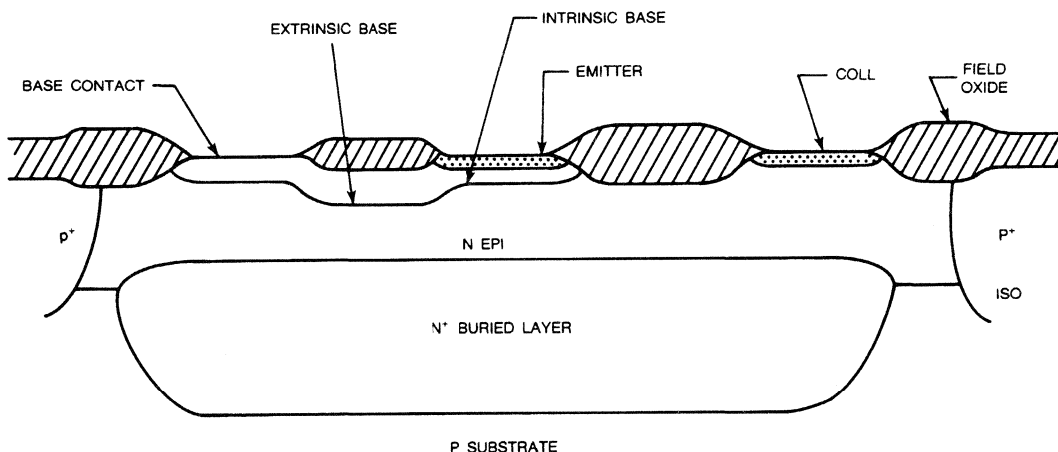


Figure 1  
IMOX-II TECHNOLOGY

DF006080

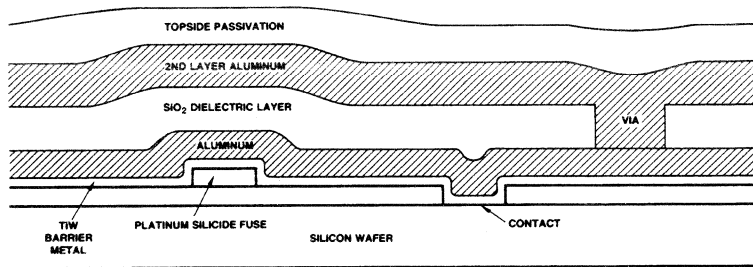


Figure 1 is a cross section of an IMOX II transistor. A heavily doped buried layer diffusion is first performed to allow for the fabrication of NPN transistors with low saturation resistances. A thin epitaxial layer is grown. The isolation and base regions are effectively self-aligned using a composite masking approach. The combined use of localized oxidations and ion implanting result in a transistor structure where the vertical side of the emitter is walled by oxide and does not come in contact with the base. This feature greatly reduces the emitter base capacitance and significantly improves the switching speed of the transistor. A short series of steps results in the definition of polycrystalline silicon in the shape of the fuse.

Following the formation of the emitter, platinum is sputtered over the entire wafer. Since all contacts, Schottkies, and fuses are exposed at this point, an alloying operation allows platinum silicide to form. The residual platinum is etched off the wafer leaving the silicide contacts, Schottkies, and fuses. After this step, the semiconductor elements of the circuit have been completely formed, and all that remains is the interconnect metallization. To form the interconnects, aluminum is used as

the primary conducting element. Aluminum has a very strong affinity for silicon, including that in platinum silicide. To retain the advantages of the very stable platinum silicide Schottky devices, it is necessary to sputter an inactive metal—tungsten—with a small amount of titanium as a bonding agent over the surface of the wafers to serve as a barrier to the diffusion or microalloying of the aluminum. Aluminum is now evaporated over the surface of the wafers and the aluminum interconnections are defined. Figure 3 shows the structure of the metal layer.

To complete the dual layer metallization structure, silicon dioxide is deposited on the wafer and etched with interlayer metal connect openings (vias). A second layer of aluminum is then placed on top of the dielectric. This layer has a thickness greater than the first one and is especially suited for power busses and output lines. To complete the circuit, a layer of nitride is deposited over the top of the wafers and etched at the appropriate locations to allow for bonding pads (see figure 2).



RF000090

Figure 2  
2-Layer Metallization Structure

### The IMOX™ III (Slot) Process

Figure 3 shows a cross section of the IMOX III process. This process will be used on most new and advanced bipolar PROM products. It will provide performance and manufacturing advantages unmatched by any other semiconductor technology. The method of isolating active component areas is what makes this process different from the IMOX II process previously discussed. A reactive ion etch creates deep vertical slots in the silicon surface. These slots extend through the epi region into the substrate. A P<sup>+</sup> channel stopping implant is placed at the bottom of the slot. An oxide is thermally grown

and the slot is filled with insulating polysilicon. The surface is then planarized to provide superior metal step coverage. The remaining processing steps are very similar to the IMOX II process. This technique of isolation reduces substantially the collector to isolation spacing compared to conventional junction isolation techniques. The result is a much smaller chip size for a given memory size and greatly improved switching speeds. The lateral platinum silicide fuse design is retained because of its proven reliability and ease of manufacturing.

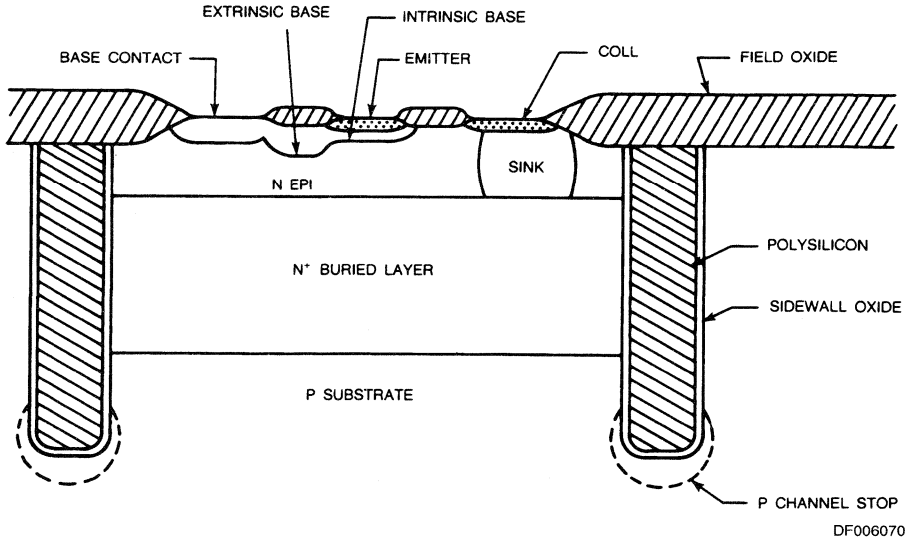


Figure 3  
IMOX™ III (SLOT) TECHNOLOGY

PROGRAMMABLE READ-ONLY MEMORY CIRCUITRY

Advanced Micro Devices' bipolar PROM designs have the general configuration shown in Figure 4. Although the figure is

for that of the Am27S20, the circuit techniques are the same for the entire generic family of PROMs.

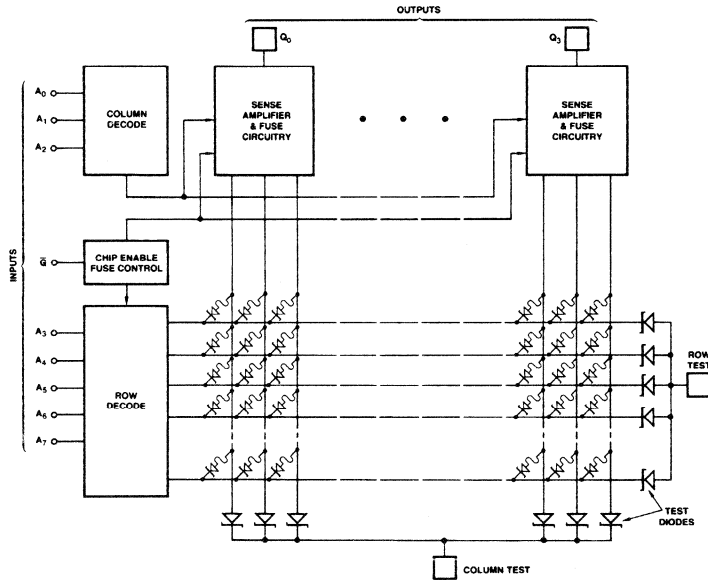


Figure 4. PROM Circuitry Block Diagram

**Input, Memory & Output Circuitry**

Two groups of input buffers and decoders called "X" and "Y" are used to drive word lines and columns respectively. The X-decode addresses ( $A_3 - A_7$ ) have Schottky clamp diode protected, PNP inputs for minimum loading. (Figure 5). The X-input buffers ( $A_3 - A_7$ ) provide A and  $\bar{A}$  outputs to a Schottky decode matrix which selects one of 64 word drivers. The word line drivers are very fast high current, high voltage, non-saturating buffers providing voltage pull down to the selected word line.

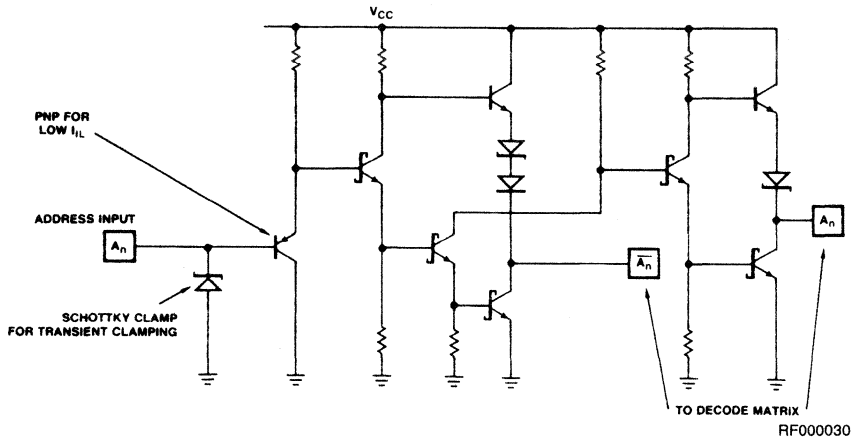
The Y-decode address buffers ( $A_0 - A_2$ ) are also Schottky diode clamped, PNP inputs driving a Schottky diode matrix. However, this diode matrix selects one of eight columns on each of the four output bits. The selected column line drives the sense amplifier input to a high level in the case of a blown fuse, or current is shunted through an unblown fuse through the selected word driver to ground resulting in a "low" input to the sense amplifier.

The sense amplifier is a proprietary fast level shifter-inverter with temperature and voltage threshold sensitivities compensated for the driving circuitry. Each of the four sense amplifiers in this circuit provides active drive to an output buffer.

Each output buffer also contains a disable input, which is driven from the chip-enable buffer. The chip-enable buffer input is a Schottky diode clamped PNP buffered design with an active pull up and pull down to drive the output buffer. Additionally, the chip-enable gate contains circuitry to provide fuse control as described below.

**Fusing Circuitry**

Platinum silicide fuses as implemented in Advanced Micro Devices' PROMs have extremely high fuse current to sense current ratios. Sensing normally requires that only a few hundred microamps flow through the fuse, whereas absolute minimum requirements for opening the fuse are approximately 100 times that amount. This provides a significant safety margin for transient protection and long-term reliability.



**Figure 5. Input Buffer Schematic**

## Bipolar Generic PROM Series

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High-yield fusing of platinum silicide fuses requires that a substantial current be delivered to each fuse. This current is sourced from the output terminals through darlington transistors which can drive the column lines when enabled. These darlington transistors are driven directly from the output and are selected by the Y-decode column select circuitry. Current during fusing flows from the output through the darlington directly to the fuse through the selected array Schottky and finally through the row-driver output transistor to ground. This path is designed for a very large fusing current safety margin.

The control circuitry works as follows: After  $V_{CC}$  is applied, the appropriate address is selected and the  $\bar{G}$  input is taken to a logic high, the programmer applies 20 volts to the bit output to be programmed. The application of the 20 volts simultaneously deselects the output buffer to prevent destructive current flow, and powers down internal circuitry unneeded during fusing to minimize chip heating.

It also enables the darlington base drive circuitry, makes power available to the darlington from the output and enables the fusing control circuitry. At this point, the PROM is ready for the control line at the chip-enable pin to release the selected row driver to allow current flow through the fuse. This technique is particularly advantageous because the control signal does not supply the large fusing currents. They are supplied through the darlington from the output power supply. Some care must be taken to avoid excessive line inductance on the output line. Reasonable and normal amounts of care will reward the user with high-programming yields.

### Special Test Circuitry

All Advanced Micro Devices PROMs include high-threshold voltage gates paralleling several address lines to allow the selection of special test words and the deselection of the columns to allow for more complete testing of the devices. Additionally, special test pads accessible prior to assembly allow for testing of some key attributes of the devices. The function of these special circuits will be described in more detail in the section, "Testing", later in this report.

There are several advantages to this technique. First, the two high current power sources,  $V_{CC}$  and the voltage applied to the output do not have critical timing requirements. The low current chip select pin gates the fusing current into the circuit. Since it is generally desirable to gate the fusing current into the chip at relatively fast rates, the use of the chip select for this purpose avoids the speed trade-off which would exist

using the output voltage as the control. The output voltage must not be raised too quickly to avoid breakdown and latchback conditions which might occur with sub-microsecond rise times on the output.

The second major advantage of this technique is that in the event that the fuse does not open during the first attempt to blow it, a near DC condition may be safely applied to it with no danger of developing a reliability problem such as that which occurs with nichrome fuses. This will be discussed in more detail later. The algorithm can therefore be designed first to minimize the time required to program the PROM, i.e. with a fast first pulse, and second, to maximize the probability that any circuit will program. Most PROMs do, of course, fuse satisfactorily with all short pulses. However, it is impossible for any manufacturer to guarantee absolutely that all fuses in all circuits receive 100 percent of the rated fusing current during programming.

Circuit defects which may be resistant to pre-programming testing prevent such a guarantee. It is, therefore, quite important to have a fuse material insensitive to marginal conditions. Even the application of single, short pulses does not guarantee that no fuse received marginal amounts of current during fusing. The silicide fuse provides this safety margin and allows the programmer to maximize the possibility of fusing by applying near DC condition to the fuses.

### Fuse Characteristics

When a fast (less than 500ns rise time) current pulse is applied to a fuse, the fuse voltage rises abruptly to a value approaching the level anticipated from calculations of the room temperature resistance. However, it quickly falls to a value of approximately two volts. This value is nearly independent of the applied current. During this period of time, typically, the fuse is molten. Very abruptly, the fuse current drops to zero indicating the separation of the platinum silicide into two distinct sections. Scanning Electron Microscope photographs of the resulting fuses (see Figure 6) indicate that the typical case is a sharp, clean separation in excess of a micron. This separation occurs in the center of the fuse because the bow-tie structure (see Figure 7) concentrates the energy density in the center away from the aluminum lines. The energy density in the center of the fuse is capable of creating temperatures substantially greater than required to melt the silicide. The very abrupt, high power applied to the fuse melts the fuse center and results in a wicking of material on either side due to surface tension.

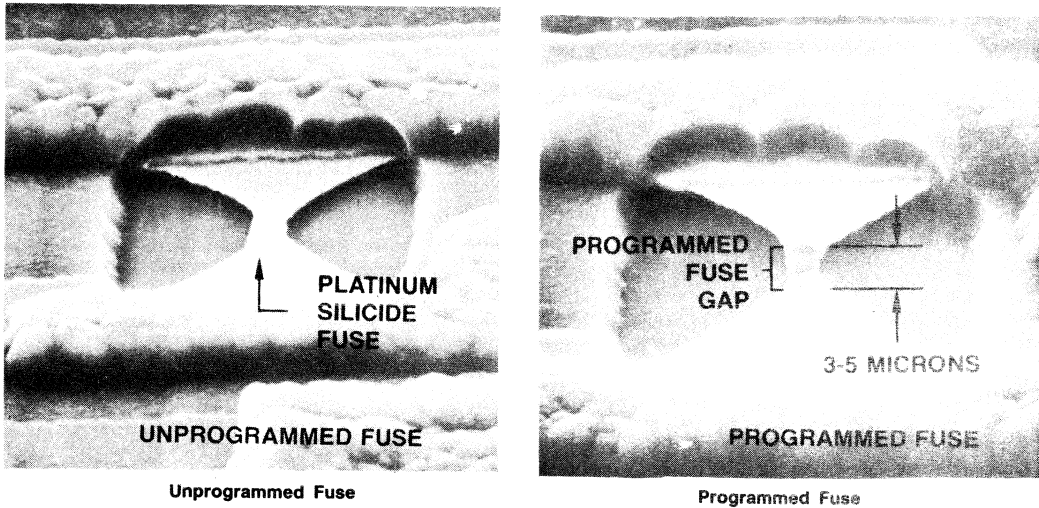


Figure 6.

**FINAL TESTING OF ADVANCED MICRO DEVICES' MEMORIES**

**Wafer Level Tests**

In addition to all the standard DC tests, Advanced Micro Devices performs a series of special tests to conform to the screening of criteria of MIL-STD-883, Method 5004 3.3 and the 0.05% AQL INT-STD-500. Also, AMD performs special tests to increase the confidence level of unique address selection and to demonstrate fusing capability on all columns and word drivers. To accomplish this, diodes are connected from the column lines and the word lines to special test pads which are accessible only during wafer probing. (See Figure 4). Using these diodes, Advanced Micro Devices confirms that each word driver is capable of sinking sufficient current to blow fuses, has appropriate saturation characteristics for AC performance, and has sufficient voltage breakdown to withstand fusing voltages. In addition, using special software, a sequence of tests dramatically increases the confidence of unique address selection on the address decoding. All darlingtontons are checked to confirm that sufficient current drive is available to blow fuses from any column. Schottky diode array leakage is also checked to affirm that it is sufficiently low so as not to overload the pull down circuitry during the high-voltage application of fusing. Finally, high voltages are applied to the inputs and outputs to remove potentially weak devices before the PROM's are assembled.

**Test Fusing**

Each PROM has two additional word drivers connected to special test fuses. These test words are valuable in demonstrating beyond reasonable doubt that the device is capable of opening fuses in all columns. They also increase the confidence level in unique addressing. Furthermore, the test words

serve as correlatable measures of the access times that the user can expect from his devices after he has placed his own program in the memory. These test words are not visible to the user unless he applies special voltages to certain address pins. Figure 8 is a diagram of this input circuit. One hundred percent of the PROM devices shipped from Advanced Micro Devices have had AC testing for access and enable times at high-and low-power supply voltages to affirm their AC characteristics.

The result of this extensive testing at both the wafer and finished device level is a product with very high-programming yields and virtually guaranteed AC performance after the user places his program in the parts. Additionally, the high voltage tests provide an additional level of confidence that the oxide and junction integrity is excellent in each circuit and that the devices will be relatively insensitive to small transients common to programming equipment.

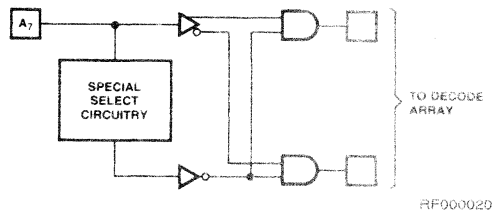


Figure 8. Special Input Circuit Used for Array Deselection and Test Word Check.

## Bipolar Generic PROM Series

### Reliability Testing

All new AMD products must pass strict reliability requirements prior to production release. Following qualification, the long term reliability of AMD's products is routinely assessed in AMD's Reliability Monitor Program (AMD 15-015). The monitor program in effect ensures monthly requalification of product to

AMD's reliability standards & goals. Product is tested by generic groupings, all key elements of the qualification test matrix are repeated monthly, and performance to standards is reviewed by the Executive Quality Board For Bipolar PROMs, over fifty billion fuse hours have been completed with no fuse related failures.

### RELIABILITY MONITOR PROGRAM FOR DEVICES IN MOLDED PACKAGES

TEST	CONDITIONS	TEST METHOD	SAMPLE SIZE	TARGET MAX FAIL RATE	ALERT LEVEL FAIL RATE
1. Infant Mortality	160 hours at 125°C or 85°C ambient (Tj < 150°C nominal) Initial and end-point electrical-QA tape	06-108	300	0.15% @ 85°C 0.20% @ 125°C	0.4% @ 85°C 0.6% @ 125°C
2. Operating Life	1000 hrs (1160 total) @ 125°C or 85°C ambient (Tj < 150°C, nominal) Initial & end-point Electrical - QA tape	06-108	120	0.2%/1k hr at 85°C 0.3%/1k hr at 125°C	1.0%/1k hr at 85°C 1.0%/1k hr at 125°C
3. Long Term Life	5,000 hrs cum @ 125°C or 85°C (Tj < 150°C, nominal) Selected from Test 2 above. Test Tape Interim point at 2k hours	06-108	120	0.2%/1k hr at 85°C 0.3%/1k hr at 125°C	1.0%/1k hr at 85°C 1.0%/1k hr at 125°C
4. Temperature and Humidity	85°C/85% RH/low power bias, 500 hours and  1000 hrs  Initial, Interim and end-point electrical QA tape	06-119	50	0.5% at 500 hrs 1.0% at 1000 hrs	2% at 500 hrs 4.0% at 1000 hrs
5. Temperature Cycle	A. 1000 cycles: -65°C to 150°C, 30 minutes/ cycle. High temperature (75°C min) Functional End-point Electrical Test	06-109	50	1.3%	4.0%
6. Pressure Cooker	121°C 15psi, 160 hours, unbiased. Initial end-point electrical	06-120	50	1.0	4.0%

RELIABILITY MONITOR PROGRAM FOR DEVICES IN HERMETIC PACKAGES

TEST	CONDITIONS	TEST METHOD	SAMPLE SIZE	TARGET MAX FAIL RATE	ALERT LEVEL FAIL RATE
1. Infant Mortality	160 hours at 125°C ambient Initial and end-point electrical test – QA tape	06 – 108	300	0.2%	0.4%
2. Operating Life	1000 hrs (1160 total) at 125°C ambient Initial and end-point electrical test – QA tape	06 – 108	120	0.2%/1k hr	1.0%/1k hr
3. Long Term Life	5,000 hrs cum, Selected Test 2 groups, same conditions and test tapes Interim point at 2k hours	06 – 108	120	0.2%/1k hr	1.0%/1k hr
4. Temperature Cycle	1000 cycles, (–65° to 150°C), 30 min/cycle end-point-hermeticity and electrical test QA tape	06 – 109	50	0.7%	2%
5. 150°C Operating Life	1000 hours at 150°C ambient Initial and end-point electrical – QA tape	06 – 108	50	0.6%/1k hr	3.0%/1k hr

## Bipolar PROMs as Programmable Logic Products

Selection Guide					
PART NUMBER	INPUTS	OUTPUTS	PRODUCT TERMS	REGISTERED OUTPUTS	$t_{PD}/I_{CC}$ $t_{SU}/t_{CP-O}/I_{CC}$ COM'L (MAX)
Am27S19A	5	8	32		25ns/115mA
Am27S19SA	5	8	32		15ns/115mA
Am27S21A	8	4	256		30ns/130mA
Am27S13A	9	4	512		30ns/130mA
Am27S29A	9	8	512		35ns/160mA
Am27S25A	9	8	512	8	30ns/20ns/185mA
Am27S25SA	9	8	512	8	25ns/12ns/185mA
Am27S33A	10	4	1024		35ns/140mA
Am27S65*	10	4	1024	4	30ns/15ns/165mA
Am27S65A*	10	4	1024	4	23ns/10ns/165mA
Am27S281A	10	8	1024		35ns/185mA
Am27S35A	10	8	1024	8	35ns/20ns/185mA
Am27S37A	10	8	1024	8	35ns/20ns/185mA
Am27S185A	11	4	2048		35ns/150mA
Am27S75*	11	4	2048	4	30ns/15ns/175mA
Am27S75A*	11	4	2048	4	25ns/12ns/175mA
Am27S291A	11	8	2048		35ns/185mA
Am27LS291	11	8	2048		30ns/90mA
Am27S291SA	11	8	2048		20ns/185mA
Am27S45A	11	8	1024	8	40ns/20ns/185mA
Am27S45SA	11	8	1024	8	25ns/10ns/185mA
Am27S47A	11	8	1024	8	40ns/20ns/185mA
Am27S47SA	11	8	1024	8	25ns/10ns/185mA
Am27S41A	12	4	4096		35ns/185mA
Am27S85*	12	4	4096	4	35ns/15ns/185mA
Am27S85A*	12	4	4096	4	27ns/12ns/185mA

\*These devices contain SSR™ on chip diagnostics



**GENERIC PROGRAMMING INFORMATION**

Advanced Micro Devices Bipolar PROMs are members of a generic series incorporating common programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable platinum-silicide fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields and produce excellent parametric correlation.

Platinum-silicide was selected as the fuse link material to achieve a well-controlled melt rate resulting in large non-conductive gaps that ensure very stable long term high reliability. Extensive operating testing has proven that this low-field, large gap technology offers the best reliability for fusible link PROMs.

High-yield fusing of the platinum-silicide fuses require that a substantial current be delivered to the decoded and selected fuse. The fusing current path has been designed to provide a large fusing current safety margin. This, however, generates large current transients at the time the fuse enable input goes to  $V_{IH}$ , and a proportional current decrease at the time the fuse opens. The magnitude of this current change may be between 50 and 150 mA with rise and fall times of 2 - 10 ns. Some care must be taken to avoid excessive line inductance in the output lines of the device ( $V_{CCO}$  for ECL devices) as well as the ground line to the device in order to maximize fusing yields.

The PROMs may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device for more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip, including  $V_{CC}$ , should be removed for a period of 5 seconds after which programming may be resumed.

**PROM Programming Equipment Guide\***

Advanced Micro Devices has an ongoing program of evaluation and qualification of PROM programming equipment from various hardware manufacturers. Qualification by AMD implies that the equipment has been evaluated for proper implementation of the programming algorithm presented at the device socket pins. Programming yield analysis on a limited sample size is also evaluated to meet expected, results of AMD.

Manufacturers listed below have been qualified on the particular equipment listed only. Not all manufacturers have implemented AMD's complete product line. Please contact your local AMD sales representative for up-to-date information regarding manufacturers implementation status.

DATA I/O 10525 Willows Road N.E. Redmond, Wa. 98052 (206) 881-6444	Systems 19, 29, & 100 Model 22	UniPak UniPak II UniPak IIB
Digilec, Inc. 1602 Lawrence Avenue Ocean, N.J. 07712 (201) 493-2420	Model UPP-803	FAM-12
Kontron Electronics 630 Price Avenue Redwood City, Ca. 94063 (415) 361-1012	Model EPP-80 Model MPP-80S	MOD 14
Oliver Advanced Engineering 320 W. Arden, Suite 220. Glendale, Ca. 91203 (818) 240-0080	OMNI 64	
Stag Systems, Inc. 528-5 Weddell Drive Sunnyvale, Ca. 94086 (408) 745-1991	Model PPX Model PP17	PM 2000
Valley Data Sciences, Inc. 2426 Charleston Road Mt. View, Ca. 94043 (415) 968-2900	Series 160	

Software support for PROMs as programmable logic products is available from the following companies, please contact the indicated company for the status of their particular product:

Assisted Technology, Inc. (CUPL)  
2381 Zanker Road, Suite 150  
San Jose, Ca. 9513  
(408) 942-8787

DATA I/O (ABEL) (PROMLINK)  
10525 Willows Road N.E.  
Redmond, Wa. 98052  
(206) 881-6444

## TTL PROM Programming Procedure

### Fusing Technique

Advanced Micro Devices' PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer yet allows the circuit to fuse the platinum silicide links quickly and reliably. Specifically, the following sequence of events must take place:

1.  $V_{CC}$  power is applied to the chip;
2. The appropriate address is selected;
3. The chip is deselected;
4. The programming voltage is applied to one output;
5. The fuse enable voltage is raised to enable a high-threshold voltage gate. This action gates the current flow through the proper fuse resulting in an open fuse in a few microseconds;
6. The output voltage is lowered (the programming voltage removed);
7. The device is enabled and the bit sensed to verify that the fuse has blown. In the unusual event that the fuse does not verify as blown, a sequence of much longer pulses is applied to the fuse at a high duty cycle until the fuse verifies as open;

8. The sequence of 2 through 7 must be repeated for each fuse which must be opened.
9. At the conclusion of programming, the device should be verified for correct data at all addresses with two (2)  $V_{CC}$  supply voltages ( $V_{CC} = 5.7\text{ V}$  &  $V_{CC} = 4.4\text{ V}$ ).

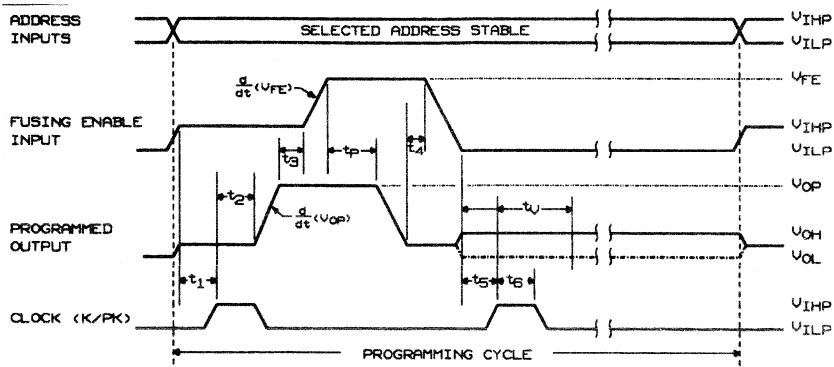
### NOTES ON PROGRAMMING

1. All delays between edges are specified from the completion of the first edge to the beginning of the second edge, not the midpoints.
2. Delays  $t_1$  through  $t_6$  must be greater than 100 ns; maximum delays of 1.5  $\mu\text{s}$  are recommended to minimize heating during programming.
3. During  $t_v$ , the output being programmed is switched to the load R and read to determine if additional programming pulses are required.
4. Outputs not being programmed are connected to  $V_{ONP}$  through resistor R which provides output current limiting.
5. All output enable pins, except the output enable used as the Fusing Enable Input, should be held at  $V_{ILP}$  for  $\bar{G}_n$  inputs and  $V_{IHP}$  for  $G_n$  inputs.

### PROGRAMMING PARAMETERS $T_A = 25^\circ\text{C}$

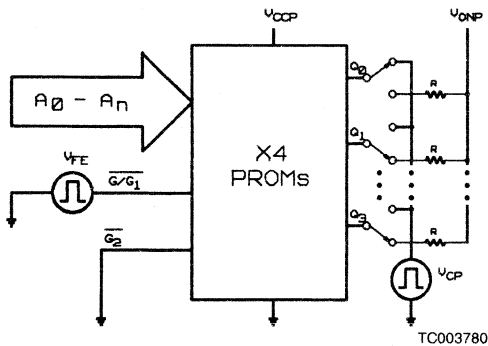
Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
$V_{IHH}$	Control Pin Extra High Level @ 10 – 40 mA	14.5	15	15.5	Volts
$V_{FE}$	Fusing Enable Voltage @ 10 – 40 mA	14.5	15	15.5	Volts
$V_{OP}$	Program Voltage @ 15 – 200 mA	19.5	20	20.5	Volts
$V_{IHP}$	Input High Level During Programming and Verify	2.4	5	5.5	Volts
$V_{ILP}$	Input Low Level During Programming and Verify	0.0	0.3	0.5	Volts
$V_{CCP}$	$V_{CC}$ During Programming @ $I_{CC} = 50 - 200\text{ mA}$	5	5.2	5.5	Volts
$dV_{OP}/dt$	Rate of Output Voltage Change	20		250	V/ $\mu\text{s}$
$dV_{FE}/dt$	Rate of Fusing Enable Voltage Change	20		1000	V/ $\mu\text{s}$
$t_p$	Fusing Time First Attempt	10	50	100	$\mu\text{s}$
	Fusing Time Subsequent Attempts	1	5	10	ms
$t_1 - t_6$	Delays Between Various Level Changes	100		1500	ns
$t_v$	Period During which Output is Sensed for $V_{Blown}$ Level		500		ns
$V_{ONP}$	Pull-Up Voltage On Outputs Not Being Programmed	$V_{CCP} - 0.3$	$V_{CCP}$	$V_{CCP} + 0.3$	Volts
R	Pull-Up Resistor On Outputs Not Being Programmed	0.2	2	5.1	K $\Omega$

PROGRAMMING WAVEFORMS



WF022020

PROGRAMMING 4 Bit WIDE TTL PROMs



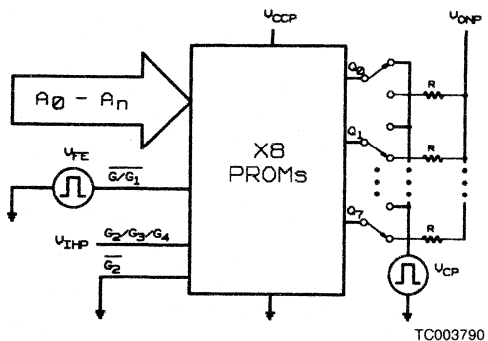
TC003780

SIMPLIFIED PROGRAMMING DIAGRAM

Part Number	Fuse Enable Pin
Am27S20/21	$\overline{G}_1$
Am27S12/13	$\overline{G}$
Am27S32/33	$\overline{G}_1$
Am27S184/185	$\overline{G}$
Am27S40/41	$\overline{G}_1$

5

PROGRAMMING 8 Bit WIDE TTL PROMs



TC003790

SIMPLIFIED PROGRAMMING DIAGRAM

Part Number	Fuse Enable Pin
Am27S15	$\overline{G}_1$
Am27S18/19	$\overline{G}$
Am27S28/29	$\overline{G}$
Am27S280/281	$\overline{G}_1$
Am27S290/291	$\overline{G}_1$
Am27S31	$\overline{G}_1$
Am27S180/181	$\overline{G}_1$
Am27S190/191	$\overline{G}_1$
Am27S43	$\overline{G}_1$
Am27S49	$\overline{G}_1$
Am27S51	$\overline{G}_1$

**PROGRAMMING 4 – WIDE REGISTERED PROMS**

The 4-bit wide Registered PROMs are programmed according to the generic TTL programming algorithm. This algorithm specifies a clock at the beginning of the programming cycle to establish output data states & enable register state. A second clock occurs prior to verification to bring programmed data to the outputs. The fuse enable input is the MODE (M) input. The DK input and all enable inputs ( $\bar{G}$  &  $\bar{G}/\bar{GS}$ ) should be held at a logic LOW throughout programming and verification. On the Am27S95 the  $G_2$  input should be held at a logic HIGH.

In addition to the programmable fusible link array these devices contain two (2) architecture fuses to program the Enable and the Initialize input functionality. Special verification circuitry within the device will permit the architecture word to be presented at the outputs for programming verification. This verification circuitry is enabled by holding the SD input at  $V_{IH}$  throughout programming and verification. The two-bit architecture word will then program the functionality of the respective inputs according to Table 1.

**Table 1**

Architecture Data Word (Hex)	Am27S65, Am27S75, and Am27S95 Input Function		Am27S85 Input Function
	$\bar{G}/\bar{GS}$ Input	$\bar{I}/\bar{IS}$ Input	$\bar{G}/\bar{GS}/\bar{I}/\bar{IS}$ Input
0	Asynchronous $\bar{Enable}$ ( $\bar{G}$ )	Asynchronous $\bar{Initialize}$ ( $\bar{I}$ )	Asynchronous $\bar{Enable}$ ( $\bar{G}$ )
4	Asynchronous $\bar{Enable}$ ( $\bar{G}$ )	Synchronous $\bar{Initialize}$ ( $\bar{IS}$ )	Asynchronous $\bar{Initialize}$ ( $\bar{I}$ )
8	Synchronous $\bar{Enable}$ ( $\bar{GS}$ )	Asynchronous $\bar{Initialize}$ ( $\bar{I}$ )	Synchronous $\bar{Enable}$ ( $\bar{GS}$ )
C	Synchronous $\bar{Enable}$ ( $\bar{GS}$ )	Synchronous $\bar{Initialize}$ ( $\bar{IS}$ )	Synchronous $\bar{Initialize}$ ( $\bar{IS}$ )

These Registered PROMs all have an additional 4-bit word which may be programmed to provide any arbitrary microinstruction for system initialization. The unprogrammed state of this word will initialize the data registers with all outputs LOW.

These parts use the initialize ( $\bar{I}/\bar{IS}$ ) pin as a select control between the array and the architecture & initialize words. Initialize ( $\bar{I}/\bar{IS}$ ) HIGH enables the array for programming and disables the architecture & initialize words. Initialize ( $\bar{I}/\bar{IS}$ )

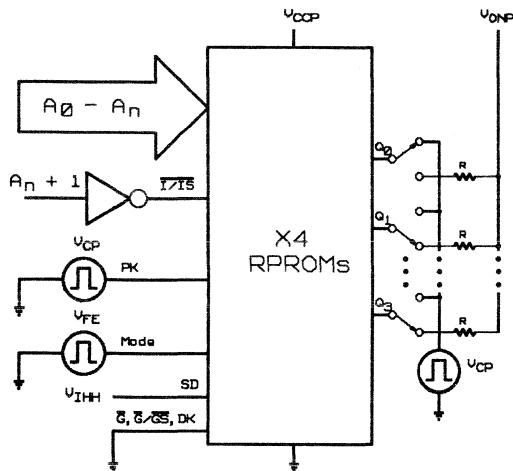
LOW enables the architecture & initialize words for programming and disables the array.

An easy implementation for programming the architecture & initialize words would be to invert the next higher address input ( $A_n + 1$ ) from the PROM programmer and apply this signal to the initialize ( $\bar{I}/\bar{IS}$ ) input pin. The array, architecture, and initialize words could then be programmed over a continuous address field according to Table 2.

**Table 2**

Device	$\bar{I}/\bar{IS}$ Pin	Array Programming Address Field (Hex)	Architecture Word Address (Hex)	Initialize Word Address (Hex)
Am27S65	$\bar{A}_{10}$	000 thru 3FF	400	401
Am27S75	$\bar{A}_{11}$	000 thru 7FF	800	801
Am27S85	$\bar{A}_{12}$	0000 thru 0FFF	1000	1001
Am27S95	$\bar{A}_{13}$	0000 thru 1FFF	2000	2001

**PROGRAMMING 4 Bit WIDE Registered PROMs**



TC003740

**SIMPLIFIED PROGRAMMING DIAGRAM**

Part Number	Fuse Enable Pin
Am27S65	(M) MODE
Am27S75	(M) MODE
Am27S85	(M) MODE
Am27S95	(M) MODE

**PROGRAMMING 8 - WIDE REGISTERED PROMs**

The 8-bit wide registered PROMs, with the exception of the Am27S55, are programmed according to the generic TTL programming algorithm. This algorithm specifies a clock at the beginning of the programming cycle to establish output data states & enable register state. A second clock occurs prior to verification to bring programmed data to the outputs. The fuse enable input is the asynchronous enable ( $\bar{G}$ ) input. The synchronous enable input ( $\bar{GS}$ ) on all parts is held at a logic LOW.

The Am27S35, Am27S37, Am27S45, & Am27S47 all have an additional 8-bit word which may be programmed to provide any arbitrary microinstruction for system initialization. The

unprogrammed state of this word will initialize the data registers with all outputs LOW.

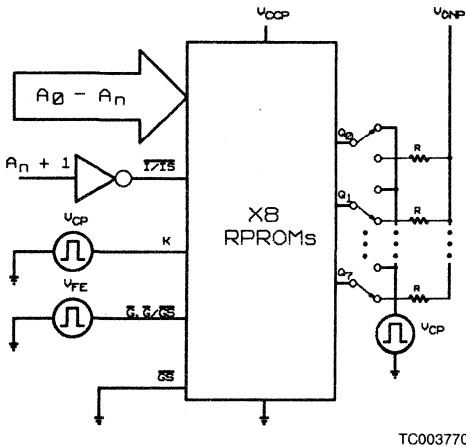
These parts use the initialize ( $\bar{I}/\bar{IS}$ ) pin as a select control between the array and the initialize word. Initialize ( $\bar{I}/\bar{IS}$ ) HIGH enables the array for programming and disables the initialize word. Initialize ( $\bar{I}/\bar{IS}$ ) LOW enables the initialize word for programming and disables the array.

An easy implementation for programming the initialize word would be to invert the next higher address input ( $A_n + 1$ ) from the PROM programmer and apply this signal to the initialize ( $\bar{I}/\bar{IS}$ ) input. The array and initialize word could then be programmed over a continuous address field according to Table 1.

**TABLE 1**

Device	$\bar{I}/\bar{IS}$	Array Programming Address Field (Hex)	Initialize Word Address (Hex)	$\bar{G}/\bar{GS}$ Word Address (Hex)
Am27S35- Am27S37	$\bar{A}_{10}$	000 thru 3FF	400	N/A
Am27S45- Am27S47	$\bar{A}_{11}$	000 thru 7FF	800	801

**PROGRAMMING 8 Bit WIDE Registered PROMs**



Part Number	Fuse Enable Pin
Am27S27	$\overline{G}$
Am27S25	$\overline{GS}$
Am27S35	$\overline{G}$
Am27S45	$\overline{G}/\overline{GS}$

**SIMPLIFIED PROGRAMMING DIAGRAM**

**PROGRAMMING the Am27S55 8 - WIDE REGISTERED PROM**

The Am27S55 is programmed according to a modified TTL programming algorithm. This algorithm specifies a clock at the beginning of the programming cycle which transitions between a TTL LOW level and  $V_{IH}$  to establish output data states & enable register state. A second clock, at normal TTL levels, occurs prior to verification to bring programmed data to the outputs. The fuse enable input is the multifunction ( $\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$ ) input.

In addition to the programmable fusible link array this device contains two (2) architecture fuses to program the  $\overline{Enable}$  or the Initialize input functionality. Special verification circuitry within the device will permit the architecture word to be presented at the outputs for programming verification. This verification circuitry is enabled by holding the  $A_1$  input at  $V_{IH}$  throughout programming and verification of the architecture & initialization fuses. The two-bit architecture word will then program the functionality of the  $\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$  pin to one of the input functions according to Table 1.

**Table 1**

Architecture Data Word (Hex)	Input Function
	$\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$ Input
00	Asynchronous $\overline{Enable}$ ( $\overline{G}$ )
01	Synchronous $\overline{Enable}$ ( $\overline{GS}$ )
02	Asynchronous Initialize ( $\overline{I}$ )
03	Synchronous Initialize ( $\overline{IS}$ )

This product has an additional 8-bit word which may be programmed to provide any arbitrary microinstruction for system initialization. The unprogrammed state of this word will initialize the data registers with all outputs LOW.

This part uses the address input ( $A_1$ ) as a select control between the array and the architecture & initialize words.  $A_1$  at either a TTL LOW or HIGH enables the array for programming and disables the architecture & initialize words.  $A_1$  when taken

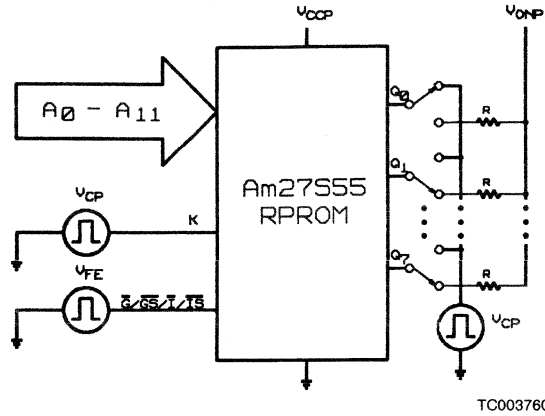
to a  $V_{IH}$  level enables the architecture & initialize words for programming and disables the array.

An easy implementation for programming the architecture & initialize words would be to have the next higher address input ( $A_n + 1$ ).  $A_{12}$  in this case, from the PROM programmer used to enable a  $V_{IH}$  HIGH level for the  $A_1$  input pin. The array, architecture, and initialize words could then be programmed over a continuous address field according to Table 2.

**Table 2**

Device	$A_1$ ( $V_{IH}$ ) Enable Control Pin	Array Programming Address Field (Hex)	Architecture Word Address (Hex)	Initialize Word Address (Hex)
Am27S55	$A_{12}$	0000 thru 0FFF	1000	1001

PROGRAMMING the Am27S55

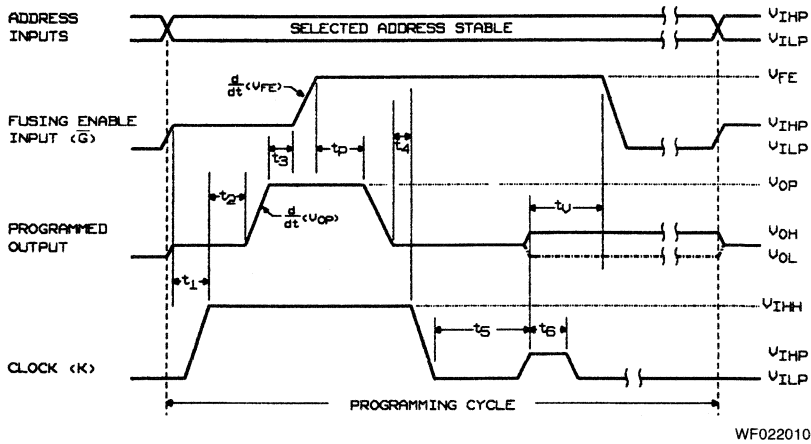


TC003760

Part Number	Fuse Enable Pin
Am27S55	$\bar{G}/GS/I/IS$

SIMPLIFIED PROGRAMMING DIAGRAM

Am27S55 PROGRAMMING WAVEFORMS



WF022010

ECL PROM Programming Procedure

Fusing Technique

Advanced Micro Devices' PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer yet allows the circuit to fuse the platinum silicide links quickly and reliably. Specifically, the following sequence of events must take place:

1.  $V_{CC}$  power is applied to the chip;
2. The appropriate address is selected;
3. The chip is deselected;
4. The programming voltage is applied to  $V_{CCO}$ ;
5. The output to be programmed is raised to  $V_{FE}$ . This action gates the current flow through the proper fuse resulting in an open fuse in a few microseconds;
6. The programming voltage ( $V_{CP}$ ) is lowered and the fuse enable voltage ( $V_{FE}$ ) is removed from the output.
7. The device is enabled and the bit sensed to verify that the fuse has blown. In the unusual event that the fuse does not

- verify as blown, a sequence of much longer pulses is applied to the fuse at a high duty cycle until the fuse verifies as open;
8. The sequence of 2 through 7 must be repeated for each fuse which must be opened.
9. At the conclusion of programming, the device should be verified for correct data at all addresses with two (2)  $V_{EE}$  supply voltages ( $V_{EE} = -4.2$  V, &  $V_{EE} = -5.7$  V.).

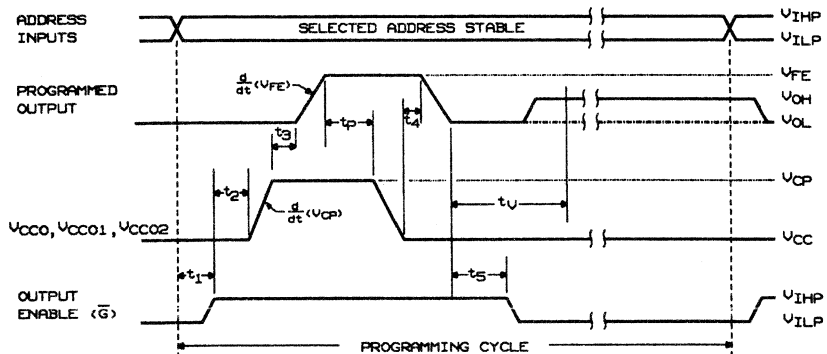
NOTES ON PROGRAMMING

1. All delays between edges are specified from the completion of the first edge to the beginning of the second edge, i.e., not the midpoints.
2. Delays  $t_1$  through  $t_5$  must be greater than 100 ns; maximum delays of 1.5  $\mu$ s are recommended to minimize heating during programming.
3. During  $t_v$ , the output being programmed is switched to the load R and read to determine if additional programming pulses are required.
4. Outputs not being programmed are connected to  $V_{ONP}$  through resistor R which provides output current limiting.

PROGRAMMING PARAMETERS  $T_A = 25^\circ\text{C}$

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
$V_{FE}$	Fusing Enable Voltage (Applied to Outputs) @ 10 mA	1.60	1.80	2.00	Volts
$V_{CP}$	Program Voltage @ 15 - 200 mA	14.5	15	15.5	Volts
$V_{IHP}$	Input High Level During Programming and Verify	-1.2	-1.0	-0.8	Volts
$V_{ILP}$	Input Low Level During Programming and Verify	-1.85	-1.65	-1.45	Volts
$V_{EEP}$	$V_{EE}$ During Programming @ $I_{EE} = 50 - 400$ mA	-5.4	-5.2	-5.0	Volts
$dV_{OP}/dt$	Rate of Program Voltage Change	20		250	V/ $\mu$ s
$dV_{FE}/dt$	Rate of Fusing Enable Voltage Change	20		1000	V/ $\mu$ s
$t_p$	Fusing Time First Attempt	40	50	100	$\mu$ s
	Fusing Time Subsequent Attempts	4	5	10	ms
$t_1 - t_5$	Delays Between Various Level Changes	100		1500	ns
$t_v$	Period During Which Output is Sensed for $V_{Blown}$ Level		500		ns
$V_{ONP}$	Pull-Down Voltage for Outputs (During Programming)	0.0	0.0	0.0	Volts
	Pull-Down Voltage for Outputs (During Verification)	-2.1	-2.0	-1.8	Volts
R	Pull-Down Resistor On Outputs Not Being Programmed	1.8	2.0	2.2	K $\Omega$

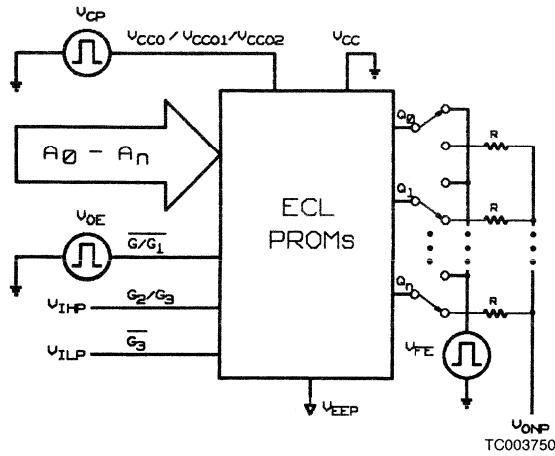
PROGRAMMING WAVEFORMS



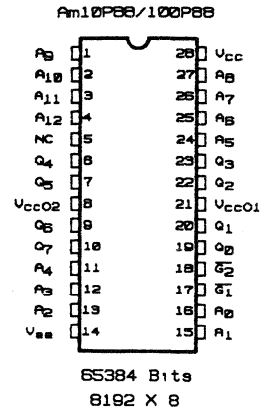
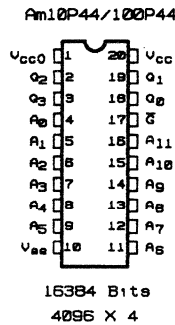
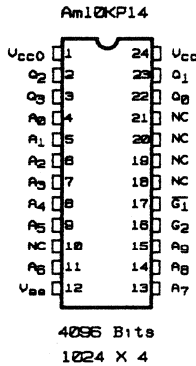
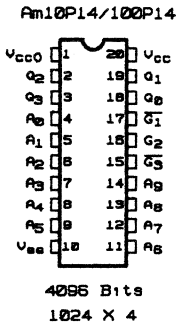
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PROGRAMMING ECL PROMS



SIMPLIFIED PROGRAMMING DIAGRAM



CD009860

# Guide to the Analysis of Programming Problems

by AMD Bipolar Memory Product Engineering



## INTRODUCTION

Advanced Micro Devices' Generic Series of Programmable Read Only Memory (PROM) circuits have been designed to provide extremely high programming yields. Available programming currents are over designed by a factor of four and special circuitry accessible only during testing is incorporated into each product to eliminate ordinarily difficult to detect shorts and opens in the array and decoders. As a result, unique decoding and very large fusing currents are virtually assured to the user. AMD PROMs have test fuses programmed prior to shipment as a further guarantee. The results of such extensive testing and design considerations are programming yields consistently in the 98% to 99.5% range.

Key to the achievement of such yields is a programmer properly calibrated to the AMD specification with good contactors, "clean" electrical wave forms and properly functioning subcircuits. In the event that your programming yields fall below 98%, you should investigate the characteristics of the failed devices to find a prominent failure mode, then use the attached information as a guide to resolving the problem. Simple problems can be very costly if not detected and corrected.

Should you continue to have trouble optimizing your programming yield, contact your AMD representative or local programmer manufacturer representative.

## Guide to the Analysis of Programming Problems

Primary Symptom	Secondary Symptom	Possible Causes
I) Units fail to program all desired bits	A) Binary blocks of missing data	<ol style="list-style-type: none"> <li>1) Address driver output which remains continuously low or continuously high.</li> <li>2) Address driver with a "low" voltage greater than 0.5V or a "high" voltage less than 2.4V.</li> <li>3) Poor, intermittent or no electrical contact to one or more address input pins.</li> </ol> <p>Any of the above may result in over programming half the array and not programming the other half.</p>
	B) Random bits of missing data	<ol style="list-style-type: none"> <li>1) Address driver with a "low" voltage greater than 0.5V or a "high" voltage less than 2.4V.</li> <li>2) Poor electrical contact to address, chip enable and output pins.</li> <li>3) Excessive transient noise on V<sub>CC</sub>, output pin (&gt; 20.5V), or ground pins. Check with a high speed storage oscilloscope for peak values during programming. Use transient suppression networks where appropriate.</li> <li>4) Programmer does not comply with AMD Programming Specification. (See Programming Parameters.) Examples:               <ul style="list-style-type: none"> <li>— Output voltage during programming less than 19.5V</li> <li>— V<sub>CC</sub> during programming less than 5.0V</li> <li>— <math>\bar{G}</math> voltage during programming less than 14.5V</li> </ul> </li> </ol>
C) All data associated with a single output missing	D) No data change	<ol style="list-style-type: none"> <li>1) Poor or no electrical contact to that output pin.</li> <li>2) Defective current switch in programmer.</li> </ol>
		<ol style="list-style-type: none"> <li>1) Wrong device or programming socket.</li> <li>2) Programmer does not comply with AMD's Programming Specifications. (See Programming Parameters.) Examples:               <ul style="list-style-type: none"> <li>— Output voltage during programming less than 19.5V</li> <li>— V<sub>CC</sub> during programming less than 5.0V</li> <li>— <math>\bar{G}</math> voltage during programming less than 14.5V</li> </ul> </li> </ol>

## Guide to the Analysis of Programming Problems

Primary Symptom	Secondary Symptom	Possible Causes
II) Over-Programmed Devices	A) One output continuously at a Logic "1"	1) Programmer does not comply with AMD's Programming Specifications. (See Programming Parameters.) Examples: — Output voltage during programming greater than 20.5V — Programmer timing incorrect 2) Open outputs can appear to be programmed to Logic "1" with the presence of a pullup resistor even though the device has not actually been programmed. 3) Excessive voltage transients on output lines during programming. Be sure appropriate transient suppression networks are placed on the outputs.
	B) All outputs continuously at a Logic "1"	1) No V <sub>CC</sub> applied to device. 2) No ground applied to device. 3) Incorrect device type. 4) Incorrect programming socket. 5) Excessive voltage transients on output lines. Use transient suppression network shown in Figure 1.

### DEFINITIONS

#### Fuse

— Conductive Platinum-Silicide link used as a memory element in Advanced Micro Devices' PROM circuits.

#### Unprogrammed Bit

— A conductive fuse.

#### Programmed Bit

— A nonconductive fuse, that is one which has been opened.

#### Output Low (Logic "0")

— An output condition created by an unprogrammed bit.

#### Output High (Logic "1")

— An output condition created by a programmed bit.

#### Failure to Program

— A device failure in which a fuse selected to be opened failed to open during the fusing operation.

#### Over Programmed

— A device failure in which a fuse which was not selected to open nevertheless opened during the fusing operation.

#### Address Driver

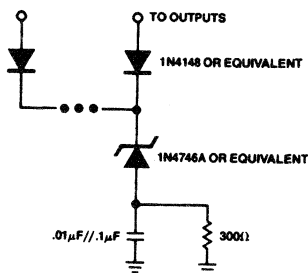
— The voltage source which drives an individual address pin in the PROM. This source is part of the programmer and drives the address pin with "0"s (0V to .45V) and "1"s (2.4V to 5.5V) depending on instructions from the programmer control circuitry. There is a separate address driver for every PROM address pin.

#### Programmer

— A system capable of providing the appropriate array of signals to a PROM circuit to cause certain user controlled bits to be programmed (i.e., fuses opened) in the device. As a minimum it consists of a memory containing the pattern to be programmed, control circuitry to sequence the addressing and fusing control pulses, power supplies, and address drivers.

5

### TRANSIENT SUPPRESSION NETWORK



AF000250

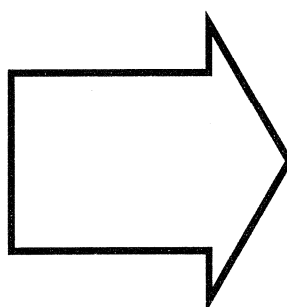
- Notes:
1. Clamp diodes should be connected to each output as close as physically possible to the device pin.
  2. V<sub>CC</sub> should be decoupled at the device pin using .01μF/.1μF capacitors.
  3. AMD recommends that all address pins be decoupled using .001μF capacitors.

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Advanced  
Micro  
Devices



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### Packaging

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## Abstract

Determination of the Thermal Resistance of Packaged Devices is of concern to the designer of new devices and to AMD customers. The Advanced Package and Material Development group has undertaken the task of characterizing current AMD products and quantifying package-related influences on Thermal Resistance. This report describes some of these effects and the technique used to measure Thermal Resistance.

## Definition of Thermal Resistance

The reliability of an integrated circuit is largely dependent on the maximum temperature which the device will attain during operation. Because the stability of a semiconductor junction declines with increasing temperature, knowledge of the thermal properties of the packaged device becomes an important factor during device design. In order to increase the operating lifetime of a given device, the junction temperatures must be minimized. This demands knowledge of the thermal resistance of the completed assembly and specification of the conditions in which the device will function properly. As devices become both smaller and more complex and the requirement for high speed operation becomes more important, heat dissipation will become an ever more critical parameter.

Thermal resistance is defined as the temperature rise per unit power dissipation above some referenced condition. The unit of measure is typically °C/watt. The relationship between junction temperature and thermal resistance is given by:

$$T_J = T_X + P_D \theta_{JX} \quad (1)$$

where:  $T_J$  = junction temperature  
 $T_X$  = reference temperature  
 $P_D$  = power dissipation  
 $\theta_{JX}$  = thermal resistance  
 $X$  = some defined test condition

In general, one of three conditions is defined for measurement of thermal resistance:

- $\theta_{JC}$  – thermal resistance measured with reference to the temperature at some specified point on the package surface.
- $\theta_{JA}$  (still air) – thermal resistance measured with respect to the temperature of a specified volume of still air.
- $\theta_{JA}$  (moving air) – thermal resistance measured with respect to the temperature of air moving at a specified velocity.

The relationship between  $\theta_{JC}$  and  $\theta_{JA}$  is

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

where  $\theta_{CA}$  is a measure of the heat dissipation due to natural convection (still air) or forced convection (moving air) and the effect of heat radiation and mounting techniques.  $\theta_{JC}$  is dependent solely on material properties and package geometry;  $\theta_{JA}$  includes the influence of the surface area of the package and environmental conditions. Each of these definitions of thermal resistance is an attempt to simulate some manner in which the package device may be used.

The thermal resistance of a packaged device, however measured, is a summation of the thermal resistances of the individual components of the assembly. These in turn are functions of the thermal conductivity of the component materials and the geometry of the heat flow paths. Like other material properties, thermal conductivity is usually temperature dependent. For alumina and silicon, two common package materials, this dependence can amount to a 30% variation in thermal conductivity over the operating temperature range of the device. The thermal resistance of a component is given by

$$\theta = \frac{L}{K(T)A} \quad (2)$$

where:  $L$  = length of the heat flow path  
 $A$  = cross sectional area of the heat flow path  
 $K(T)$  = thermal conductivity as a function of temperature

and the overall thermal resistance of the assembly (discounting convective effects) will be:

$$\theta = \sum \theta_n = \sum \frac{L_n}{K_n A_n}$$

but since the heat flow path through a component is influenced by the materials surrounding it, determination of  $L$  and  $A$  is not always straightforward.

A second factor that affects the thermal resistance of a packaged device is the power dissipation level and, more particularly, the relationship between power level and die geometry, i.e., power distribution and power density. By rearrangement of equation 1 to

$$P_d = \frac{1}{\theta_{JX}} (T_J - T_X) = \frac{1}{\sum \theta_n} (T_J - T_X) \quad (3)$$

the relationship between  $P_d$  and  $T_J$  can be more clearly seen. Thus, to dissipate a greater quantity of heat for a given geometry,  $T_J$  must increase and, since the individual  $\theta_n$  will also increase with temperature, the increase in  $T_J$  will not be a linear function of increasing power levels.

A third factor of concern is the quality of the material interfaces. In terms of package construction, this relates

specifically to the die attach bond, and for those packages having a heatsink, the heatsink attach bond. The quality of the die attach bond will most severely influence the package thermal resistance as this is the area which first impedes the transfer of heat out of the silicon die. Indeed, it seems likely that the initial thermal response of a powered device can be directly related to the quality of the die attach bond.

## Experimental Method

The technique for measurement of thermal resistance involves the identification of a temperature-sensitive parameter on the device and monitoring this parameter while the device is powered. For bipolar integrated circuits the forward voltage of the substrate isolation diode provides a convenient parameter to measure and has the advantage of a linear dependence on temperature. MOS devices which do not have an accessible substrate diode present greater measurement difficulties and may require simulation through use of a specially designed thermal test die. Choice of the parameter to be measured must be made with some care to ensure that the results of the measurement are truly representative of the thermal state of the device being investigated. Thus measurement of the substrate isolation diode which is generally diffused across the area of the die yields a weighted average of the condition of the individual junctions across the die surface. Measurement of a more local source would yield a less generalized result.

For MOS devices, simulation is accomplished using the thermal test die. The basis for this test die is a 25 mil square cell containing an isolated diode and a 1 KΩ resistor. The resistors are interconnected from cell to cell on the wafer before it is cut into multiple arrays of the basic unit cell. In use the device is powered via the resistors with voltage or current adjusted for the proper level and the voltage drop of the individual diodes is monitored as in the case of actual devices.

Prior to the thermal resistance test, the diode voltage/temperature calibration must be determined. This is done by measuring the forward voltage at 1 mA current level at two different temperatures. The diode calibration factor is then:

$$K_1 = \frac{T_2 - T_1}{V_2 - V_1} = \frac{\Delta T}{\Delta V} \quad (4)$$

in units of °C/mV. For most diodes used for this test the voltage/temperature relationship is linear and these two measurement points are sufficient to determine the calibration.

The actual thermal resistance measurement has two alternating phases: measurement and power on. The device under test is pulse powered with an ON duty cycle of 99% and a repetition rate of < 100 Hz. During the brief OFF states the device is reverse-biased with a 1 mA current and the voltage drop is measured. The series of voltage readings are averaged over short periods and compared to the voltage reading obtained before the device was first powered ON. The thermal resistance is then computed as:

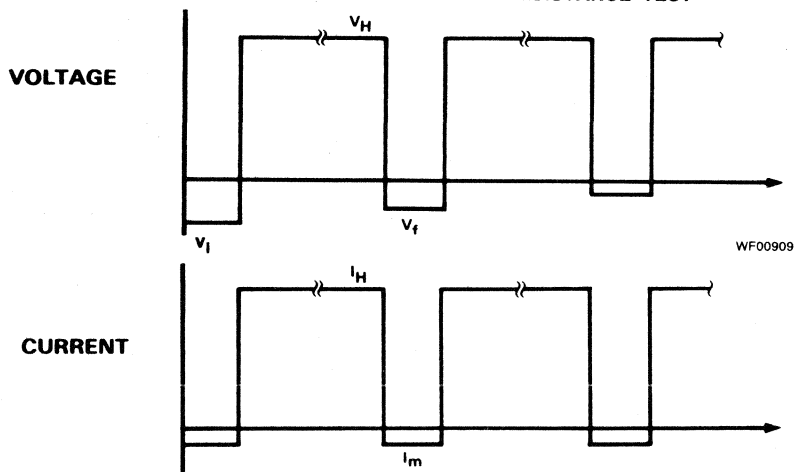
$$\theta_{jk} = \frac{K_f(V_F - V_i)}{V_{H/I_H}} = \frac{K_f \Delta V}{P_D} \quad (5)$$

where:  $K_f$  = calibration factor  
 $V_i$  = initial forward voltage value  
 $V_F$  = current forward voltage value  
 $V_H$  = heating voltage  
 $I_H$  = heating current

The pulsing measurement is continued until the device has reached thermal equilibrium and the final value measured is the equilibrium thermal resistance of the device under test.

When the end result desired is  $\theta_{JA}$  (still air), the device and the test fixture (typically a standard burn-in socket) are enclosed in a box containing approximately 1 cubic foot of air. For  $\theta_{JC}$  measurements the device is attached to a large metal heatsink. This ensures that the reference point on the device surface is maintained at a constant temperature. The requirements for measurement of  $\theta_{JA}$  (moving air) are rather more complex and involve the use of a small wind tunnel with capability for monitoring air pressure, temperature and velocity in the area immediately surrounding the device tested. Standardization of this last test requires much careful attention.

WAVEFORMS FOR PULSED THERMAL RESISTANCE TEST





## Experimental Results

The thermal resistance data included in the attached table was extrapolated from data collected using the procedure outlined in the preceding section. This data has resulted from an ongoing program undertaken by members of the Material Technology Development group.

Updated data will replace the data in this table as each device is measured or revised data becomes available.

## Thermal Resistance of AMD Products

(Notes 1, 2 and 3)

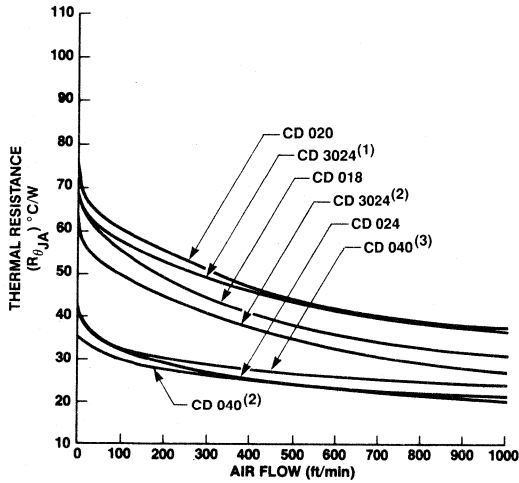
PIN COUNT	PACKAGE TYPE (Note 4)	$\theta_{JA}$	$\theta_{JC}$
20	Ceramic DIP	60	11
	Plastic DIP	61	30
	Ceramic Flatpack	56	CR
	Ceramic LCC	61	CR
	Plastic LCC*	CR	CR
24	Ceramic DIP	57	15
	Plastic DIP	60	CR
	Ceramic Flatpack	85	9
28	Ceramic LCC	CR	CR
	Plastic LCC*	58	CR

Notes:

1. Representative values for each package type — for information only.
2. Any given device may differ from these values. Consult local AMD sales office for specific-device information.
3. CR = Consult local AMD Representative.
4. DIP = Dual-In-Line Package  
LCC = Leadless Chip Carrier  
LCC\* = Leaded Chip Carrier

Table 1.

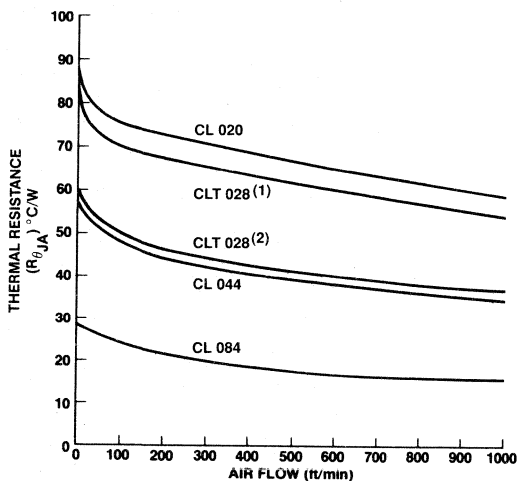
## Cerdip (CD) Packages



Package	Die Size (mils) <sup>2</sup>	$R_{\theta,JC}^*$ (°C/Watt)
CD 018	22,500	6
CD 020	5,625	14
CD 3024 <sup>(1)</sup>	5,625	16
CD 3024 <sup>(2)</sup>	11,250	9
CD 024	50,625	3
CD 040 <sup>(3)</sup>	22,500	4
CD 040 <sup>(2)</sup>	50,625	2

\* These are typical values for the given die size.  
Other die size values to be supplied in the future.  
Most Advanced Micro Devices' products will be slightly lower.

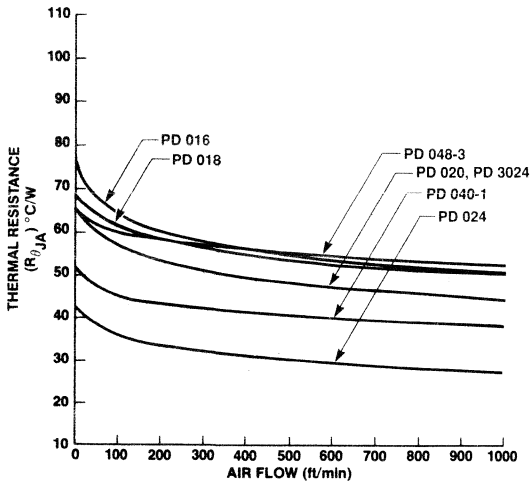
## Leadless Chip Carriers (CL) Packages



Package	Die Size (mils) <sup>2</sup>	$R_{\theta,JC}^*$ (°C/Watt)
CL 020	5,625	16
CLT 028 <sup>(1)</sup>	5,625	20
CLT 028 <sup>(2)</sup>	22,500	9
CL 044	22,500	4
CL 084	50,625	4

\* These are typical values for the given die size.  
Other die size values to be supplied in the future.  
Most Advanced Micro Devices' products will be slightly lower.

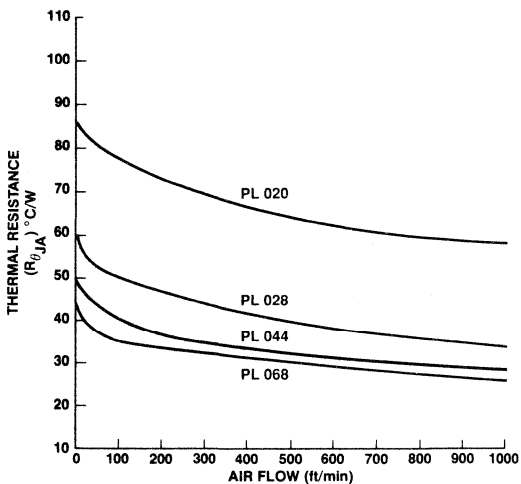
## Molded Dip (PD) Packages



Package	Die Size (mils) <sup>2</sup>	$R_{\theta JC}^*$ ( $^{\circ}\text{C/Watt}$ )
PD 016	5,625	29
PD 018	5,625	30
PD 020	5,625	23
PD 024	50,625	10
PD 3024	5,625	22
PD 040-1	22,500	16
PD 040-3	5,625	23

\* These are typical values for the given die size.  
Other die size values to be supplied in the future.  
Most Advanced Micro Devices' products will be slightly lower.

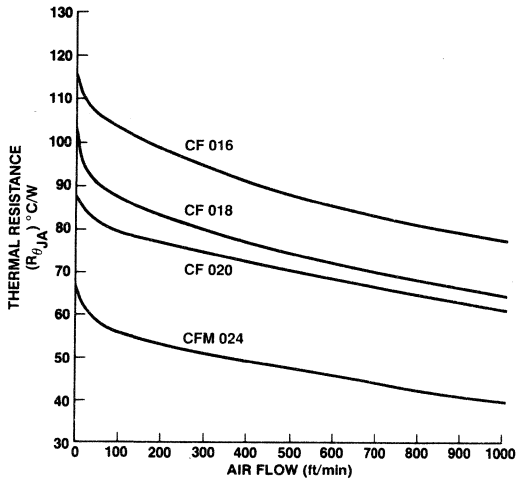
## Plastic Leaded Chip Carrier (PL) Packages



Package	Die Size (mils) <sup>2</sup>	$R_{\theta JC}^*$ ( $^{\circ}\text{C/Watt}$ )
PL 020	5,625	35
PL 028	22,500	16
PL 044	22,500	13
PL 068	50,625	8

\* These are typical values for the given die size.  
Other die size values to be supplied in the future.  
Most Advanced Micro Devices' products will be slightly lower.

## Cerpack (CF) Packages

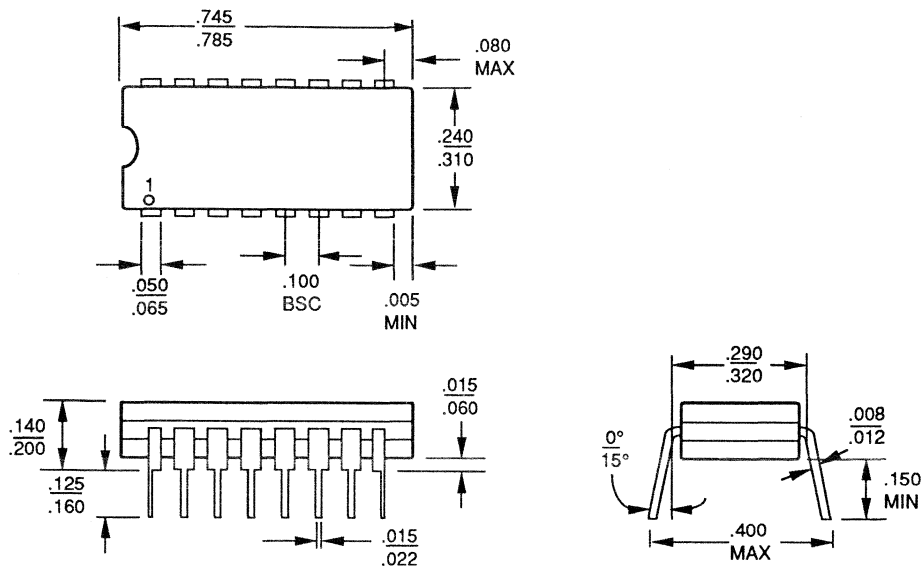


Package	Die Size (mils) <sup>2</sup>	$R^*_{\theta_{JC}}$ ( $^{\circ}\text{C/Watt}$ )
CF 016	5,625	21
CF 018	5,625	17
CF 020	5,625	15
CFM 024	22,500	4

\* These are typical values for the given die size.  
 Other die size values to be supplied in the future.  
 Most Advanced Micro Devices' products will be slightly lower.

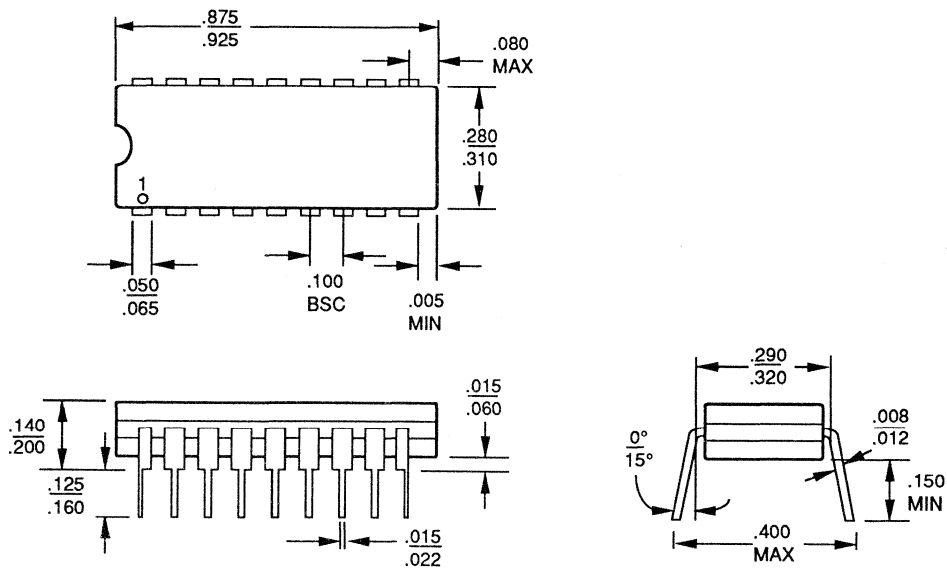
# Physical Dimensions

## CD 016



07319B

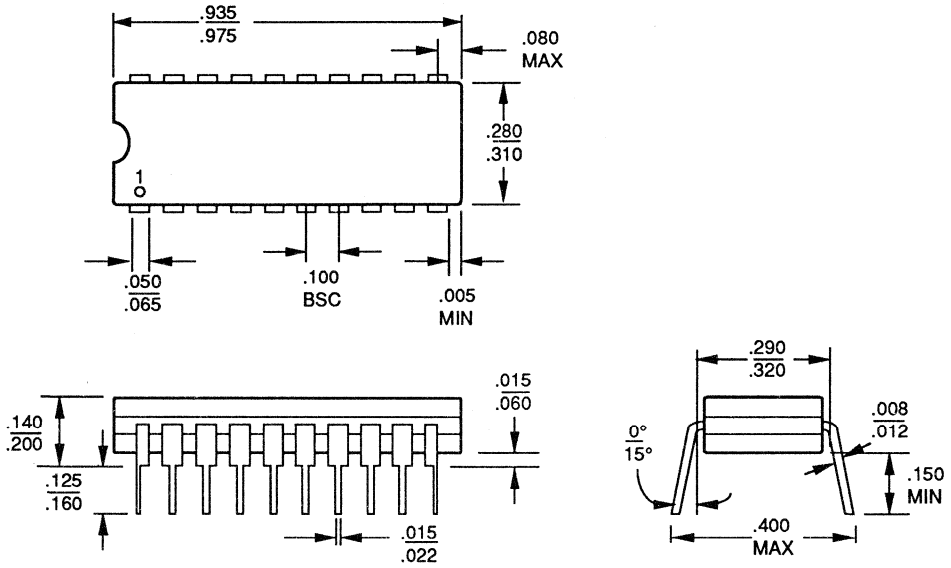
## CD 018



07803C

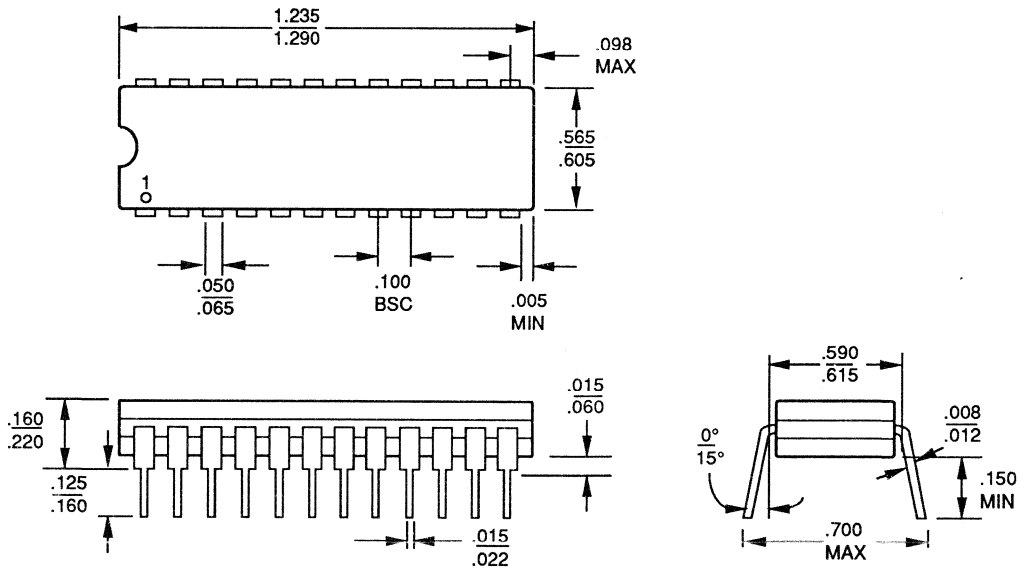
Physical Dimensions are for reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.

CD 020



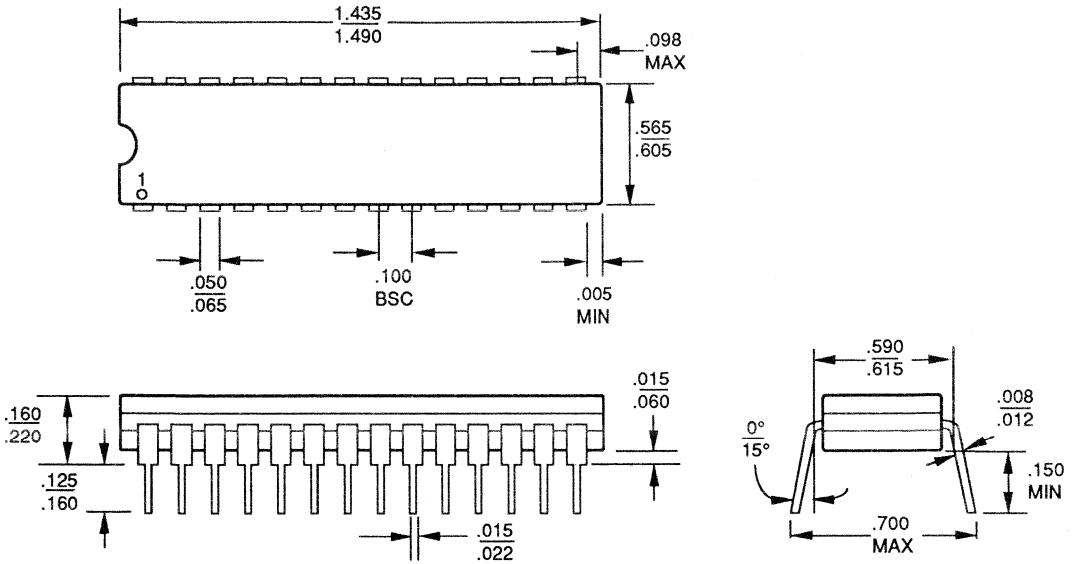
07553B

CD 024



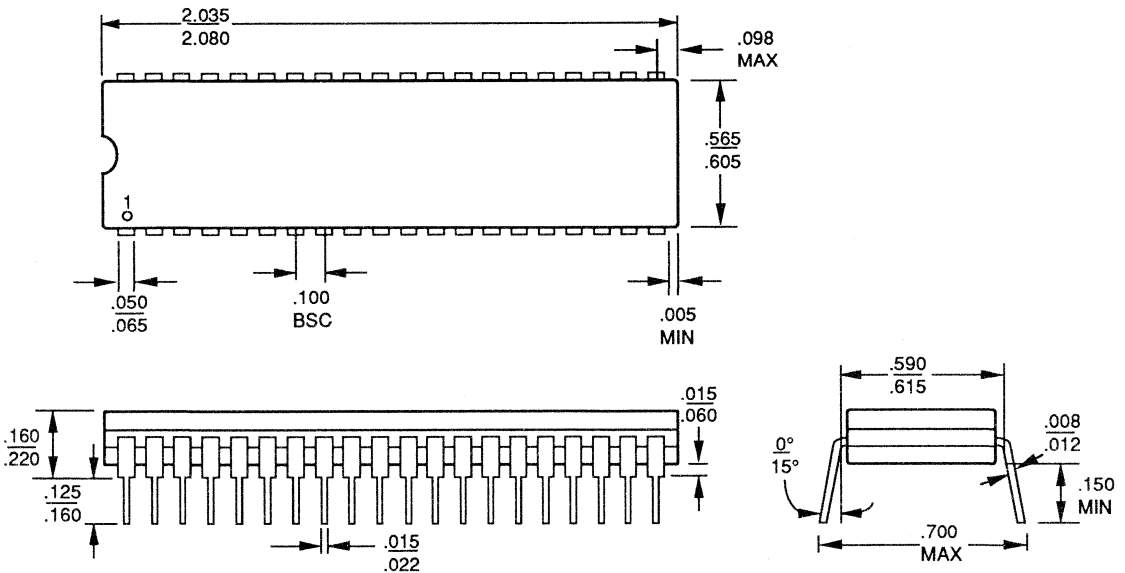
07156B

CD 028



06837C

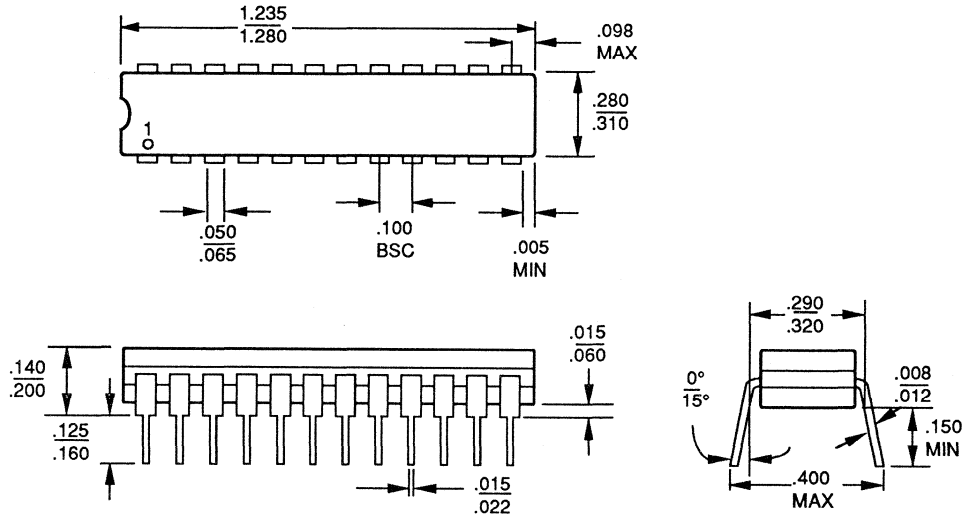
CD 040



06824C

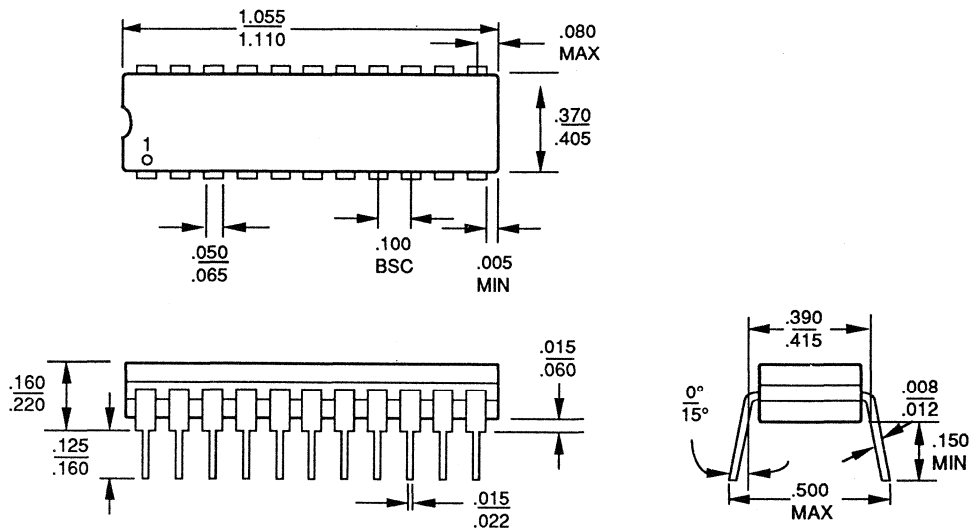
6

CD 3024



06850C

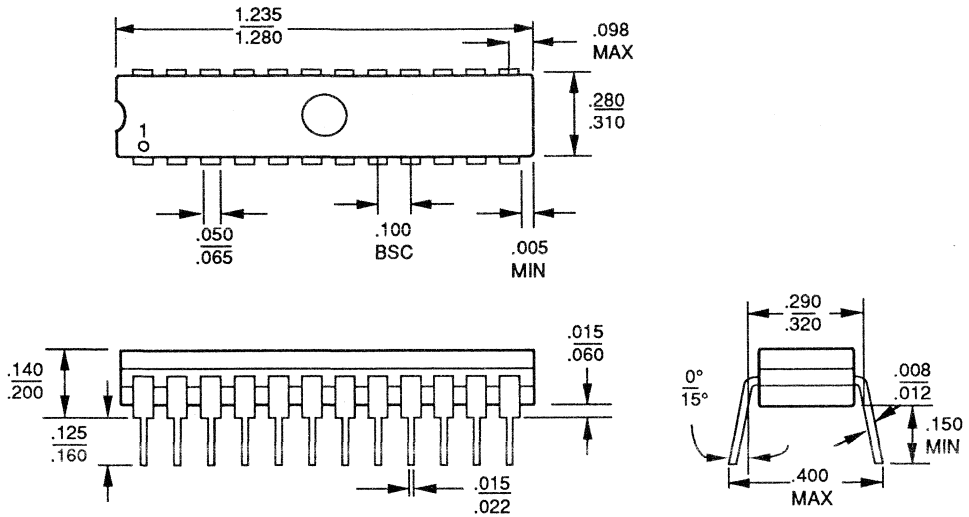
CD 4022



08244B

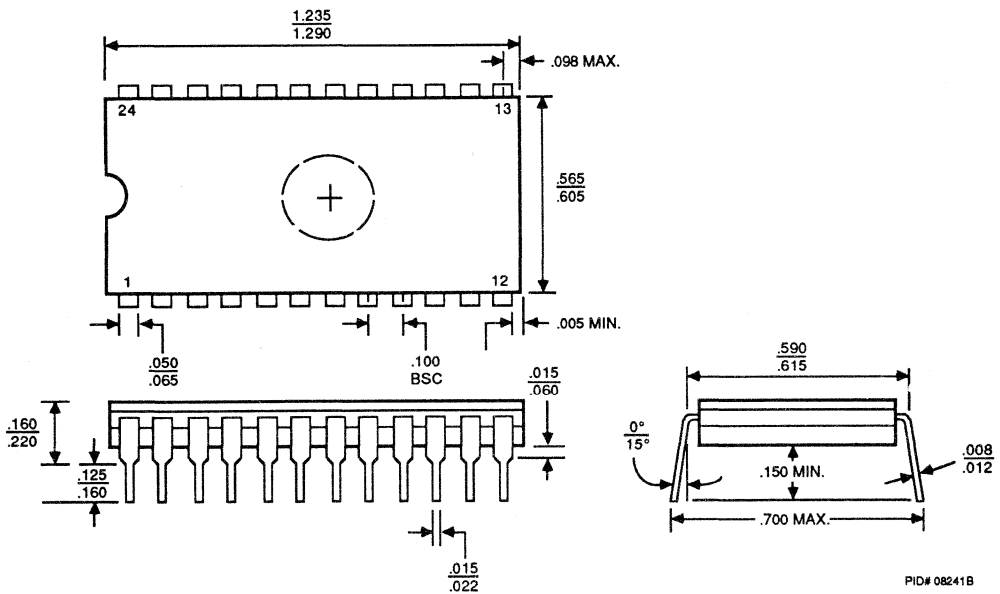


CDE 024



12189A

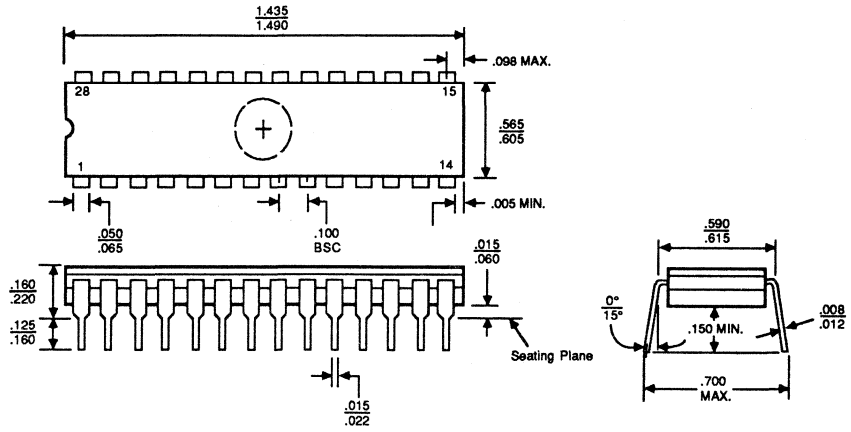
CDV 024



PID# 08241B

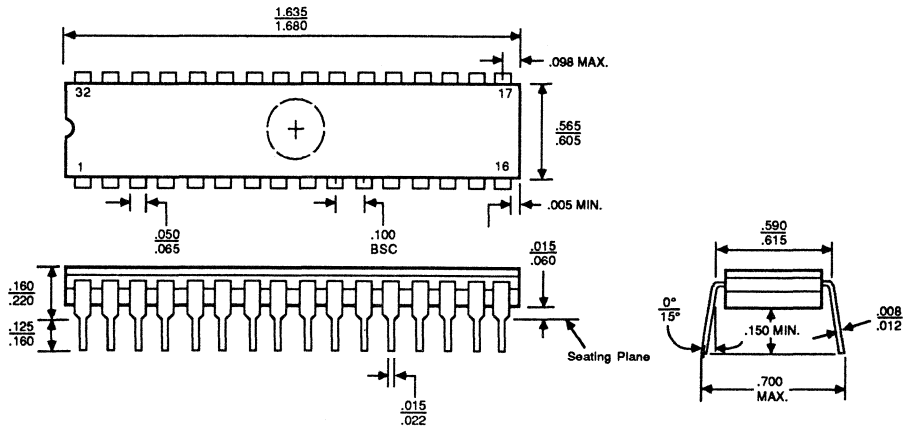
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### CDV 028



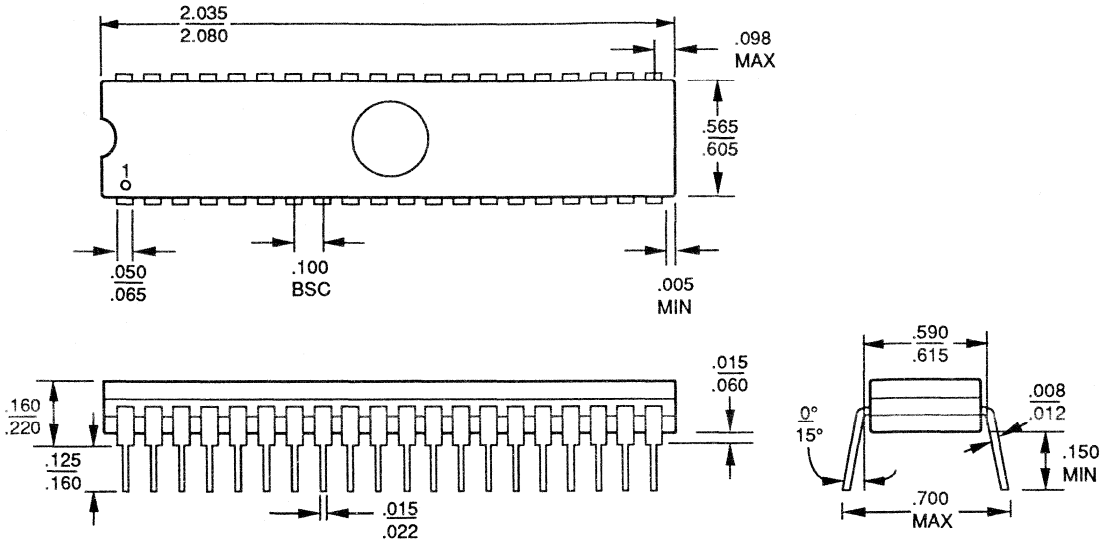
PID# 06267B

### CDV 032



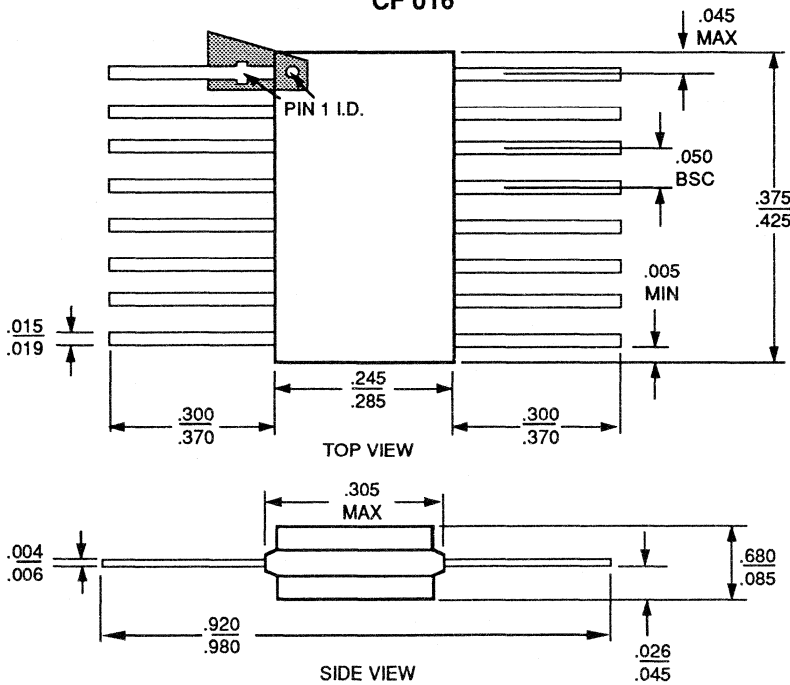
PID# 11092A

CDV 040



07880C

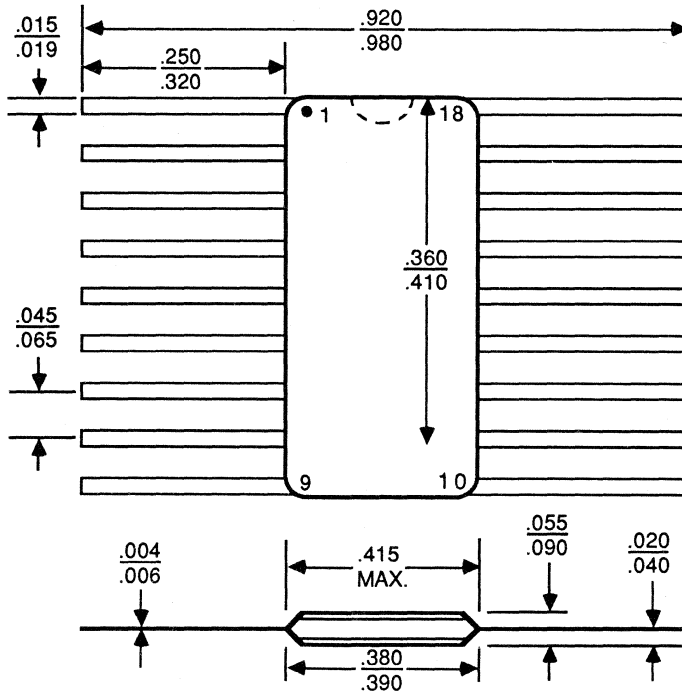
CF 016



07320B

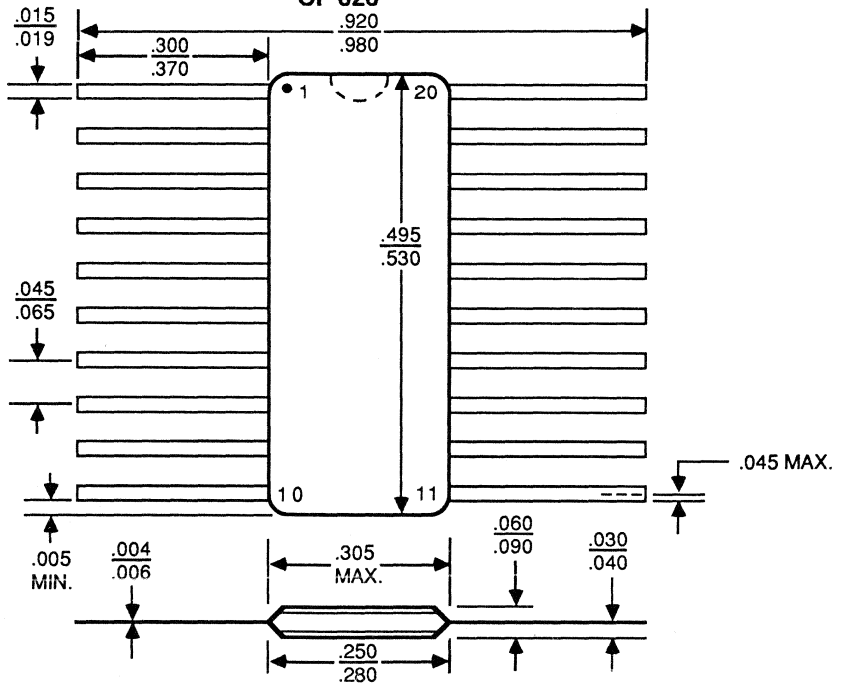
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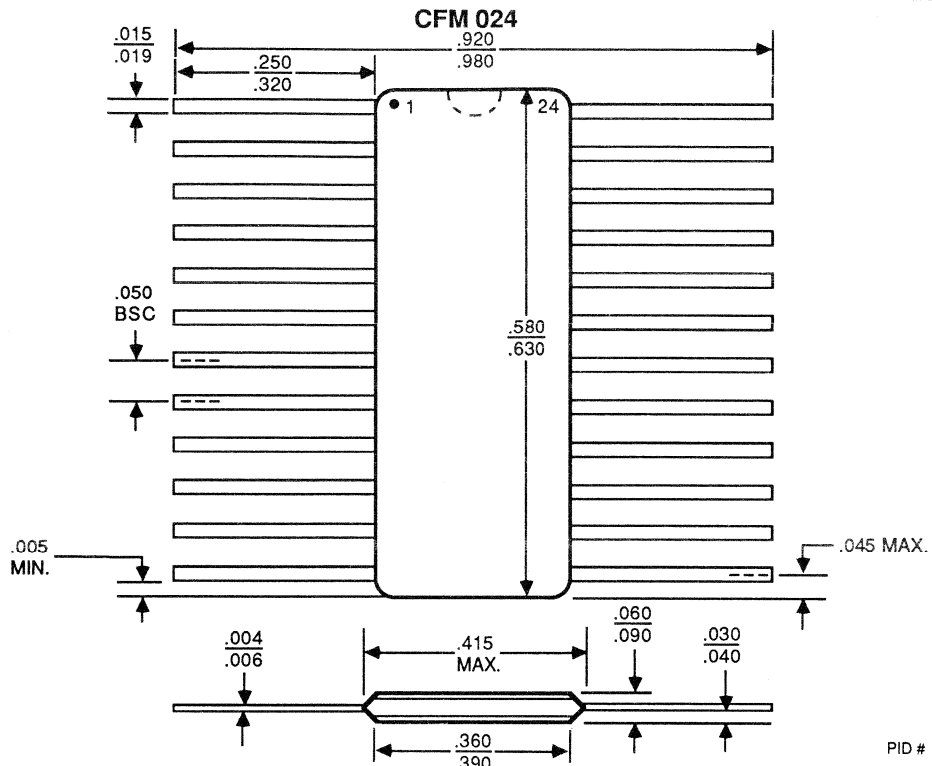
**CF 018**



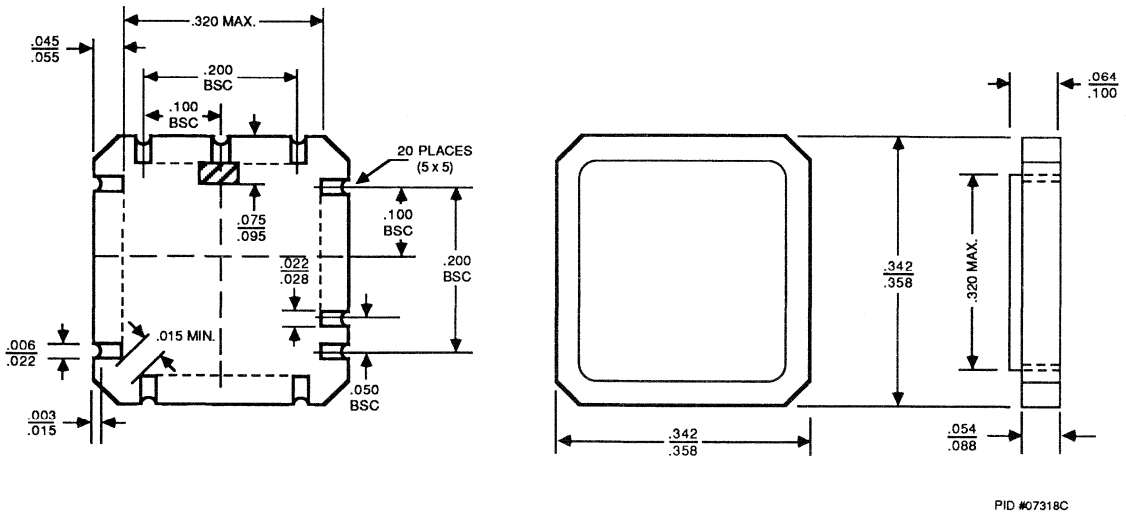
08256A

**CF 020**



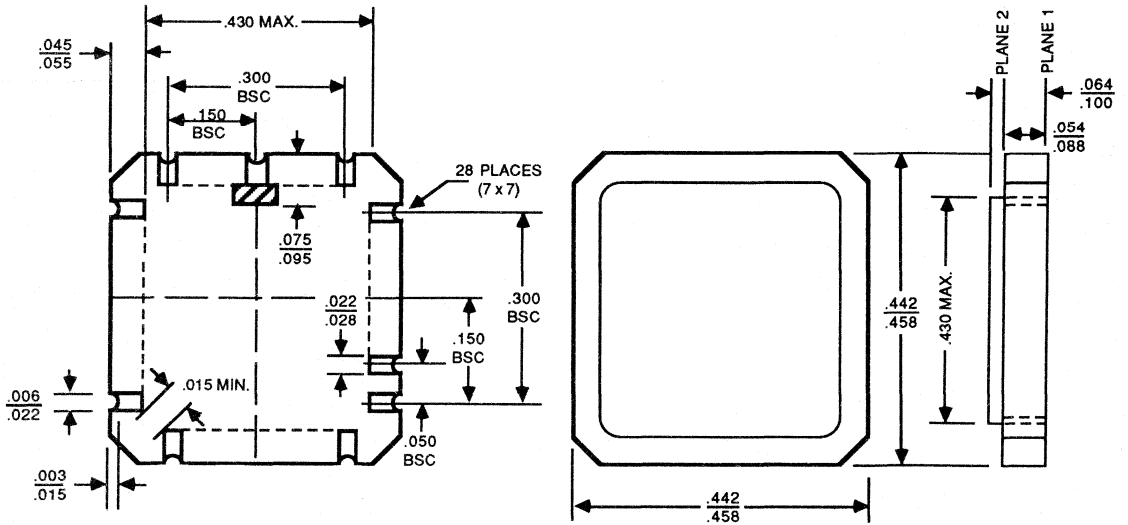


**CL 020**



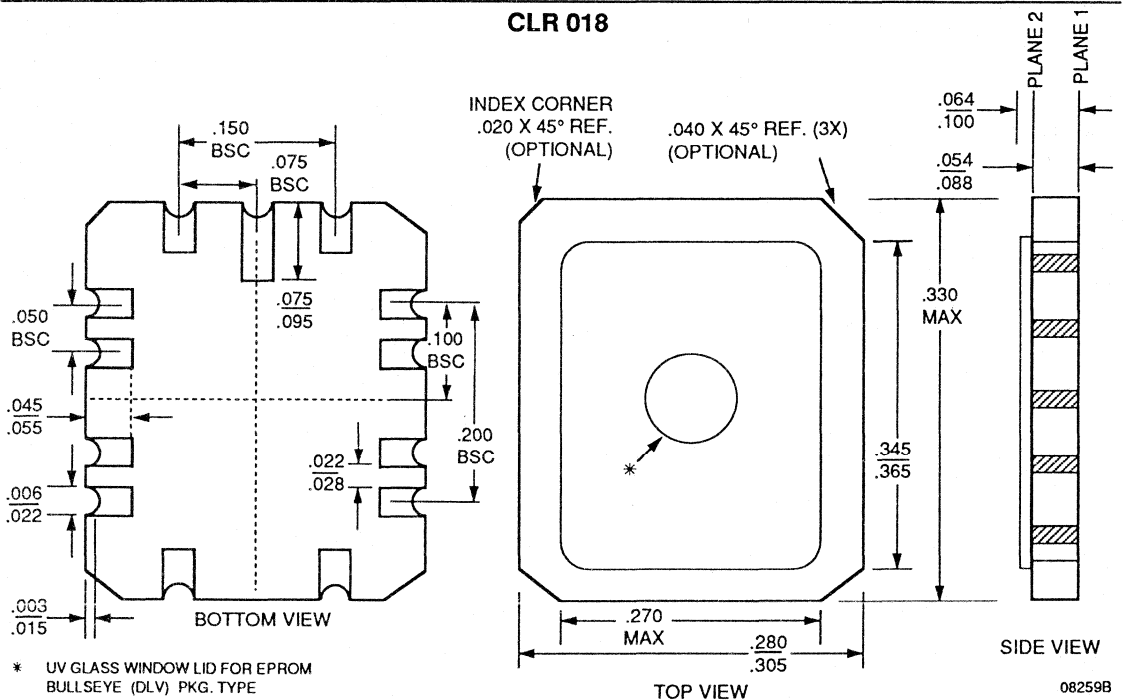
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CL 028



PID #06595F

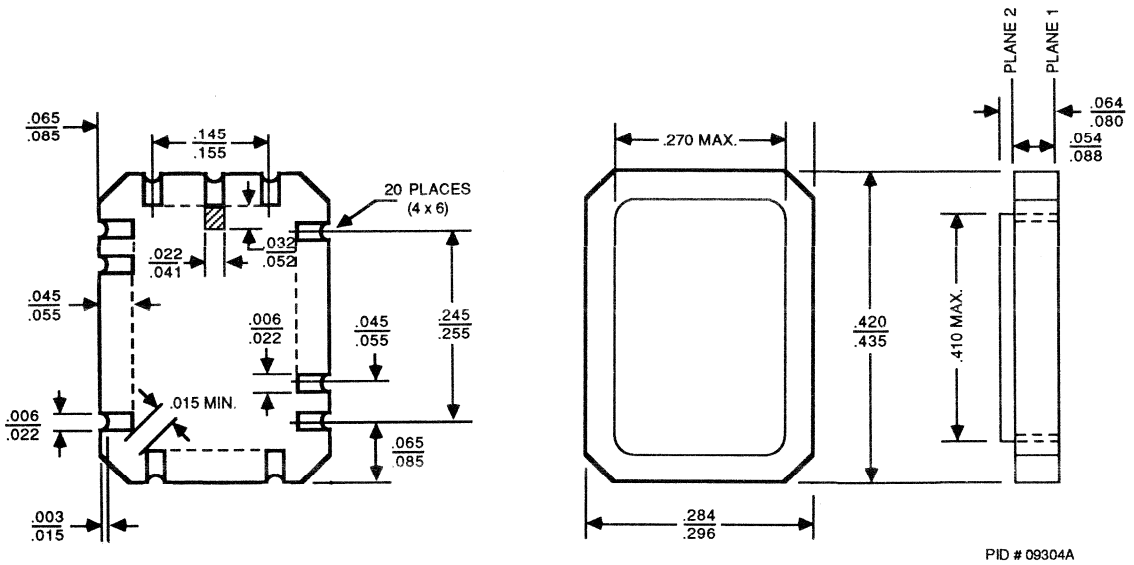
CLR 018



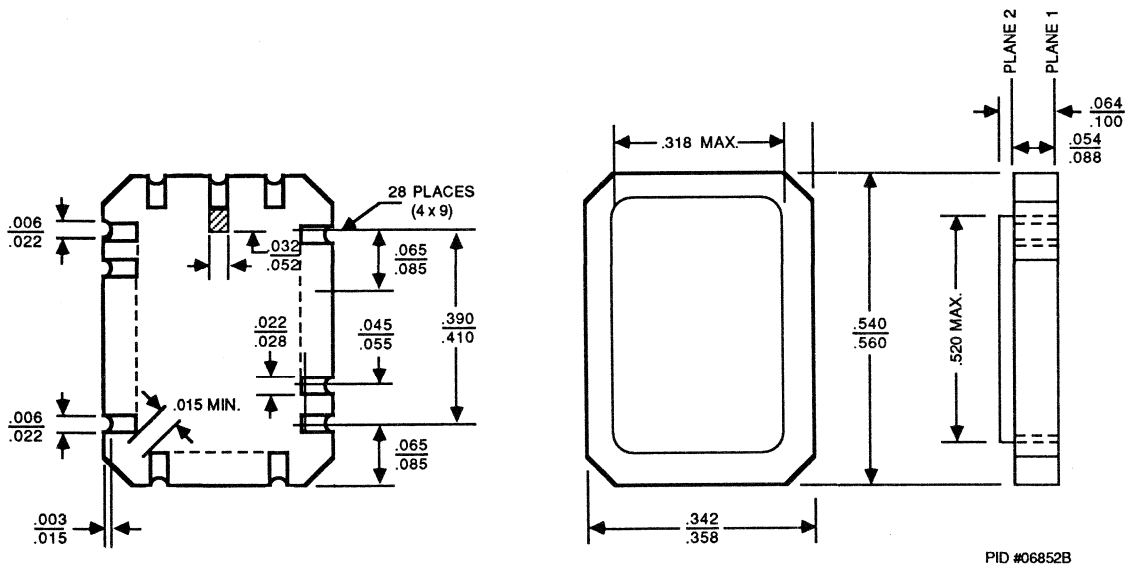
\* UV GLASS WINDOW LID FOR EPROM BULLSEYE (DLV) PKG. TYPE

08259B

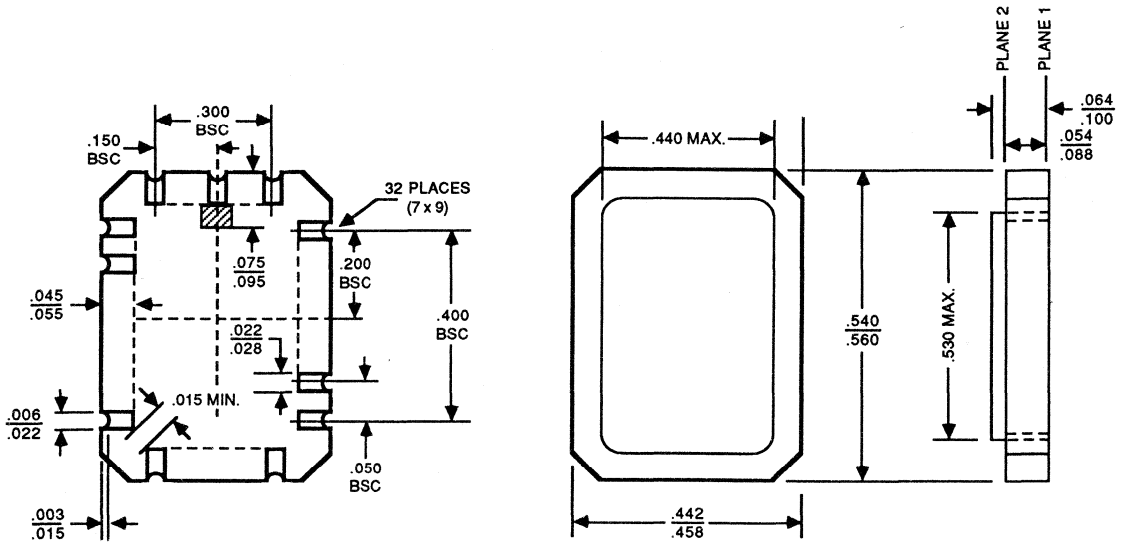
CLR 020



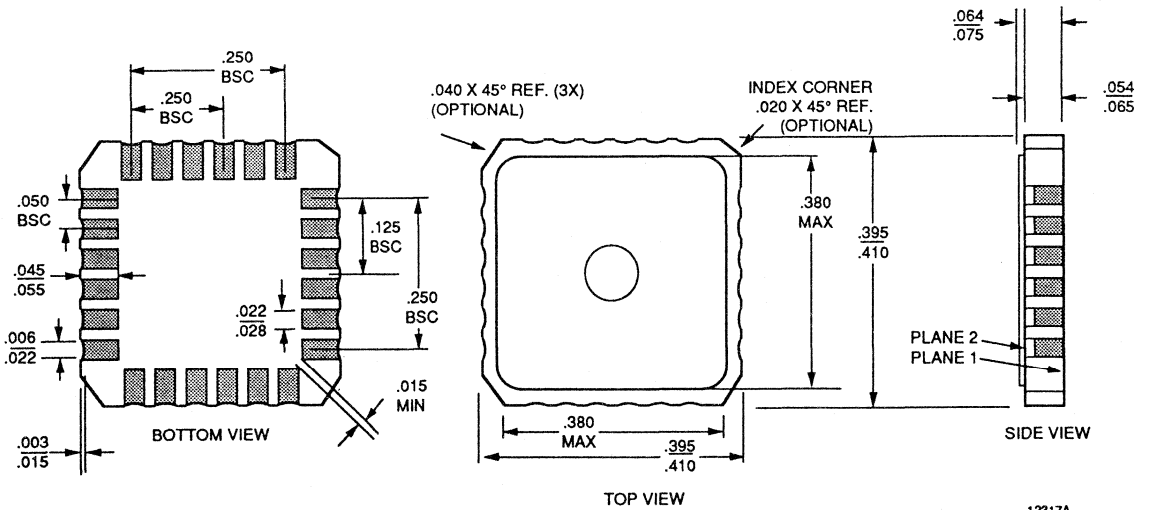
CLR 028



CLR 032



CLT 024

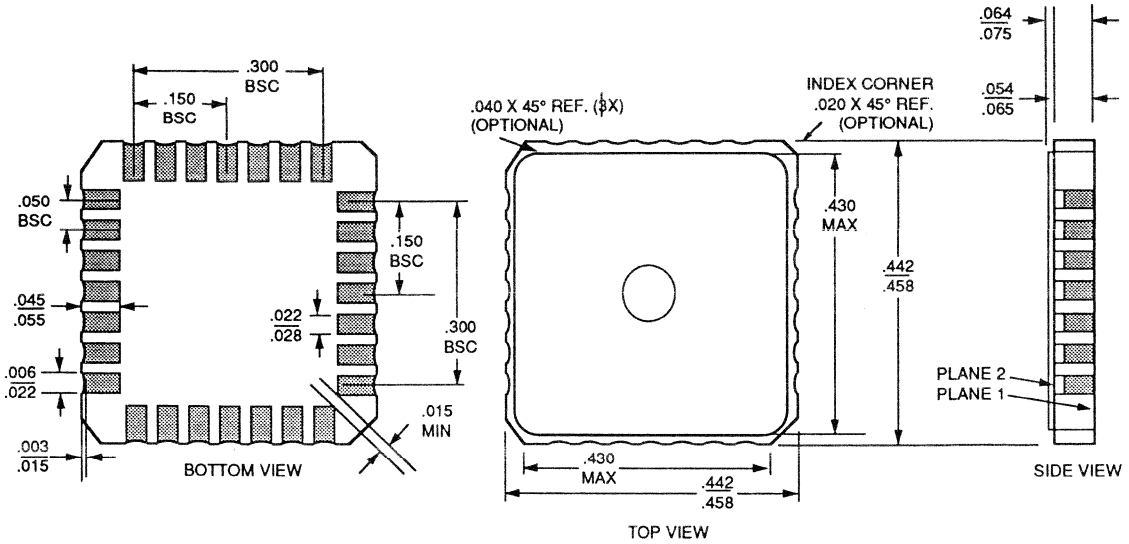


12317A

12317A

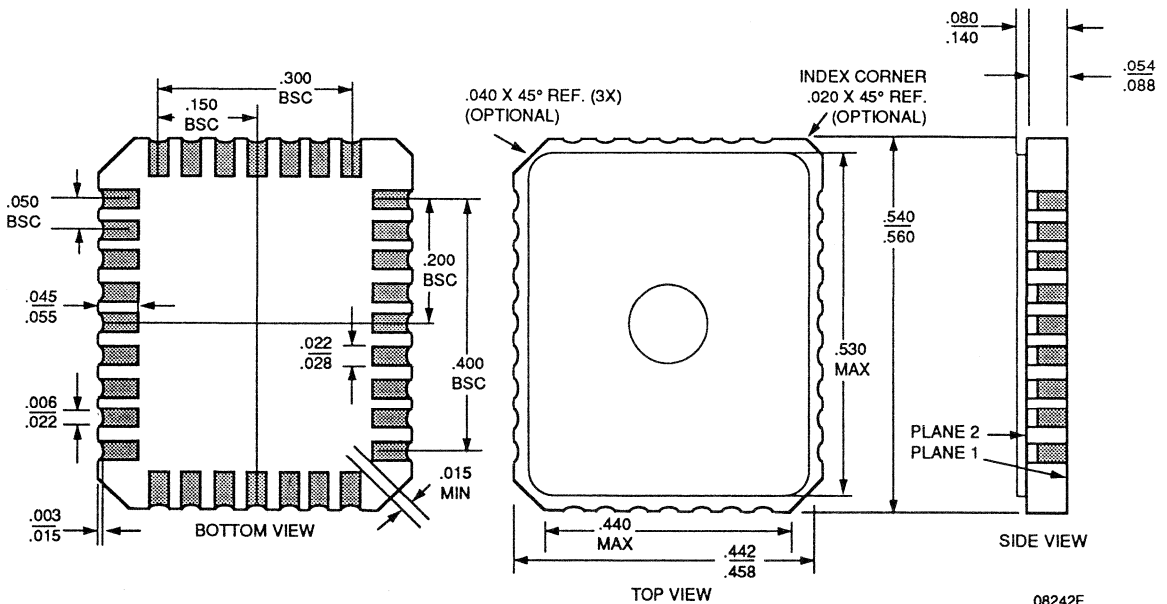


CLT 028



07703C

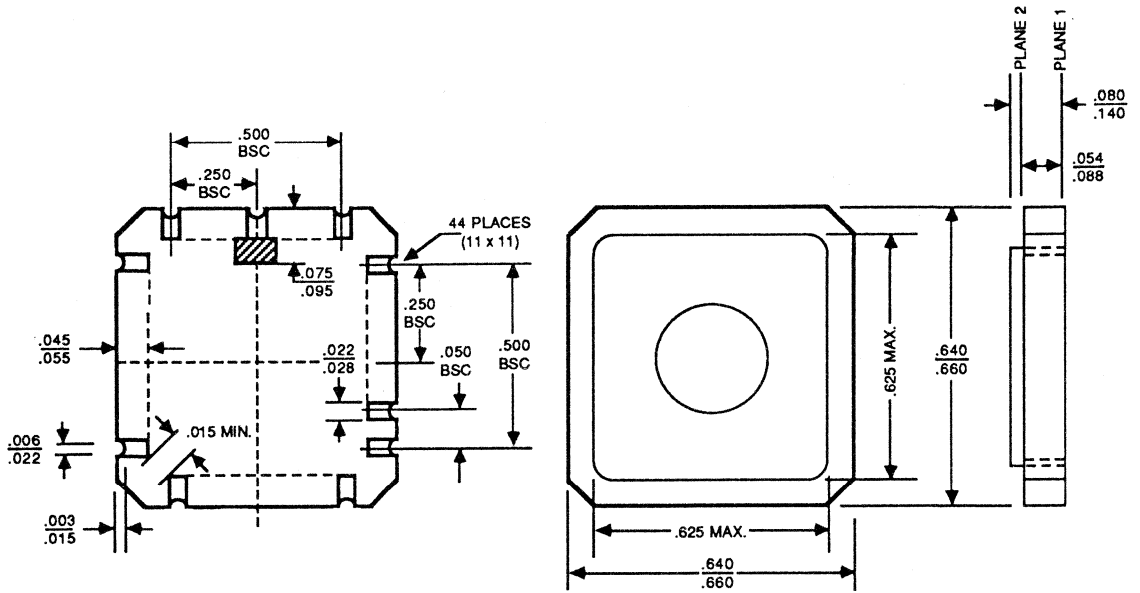
CLV 032



08242F

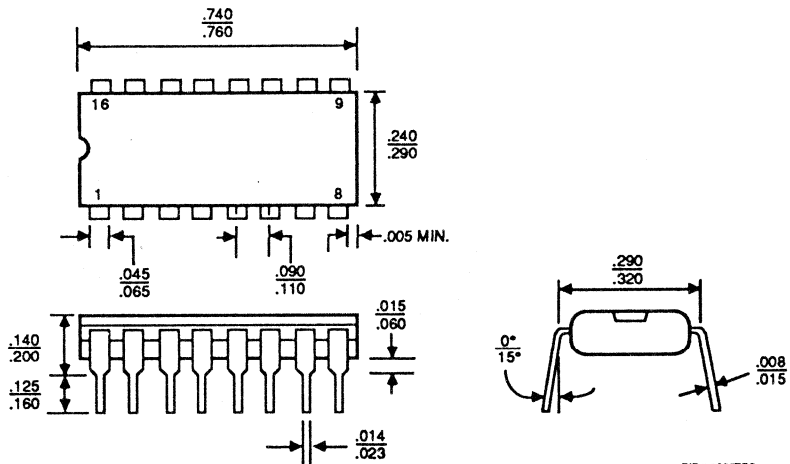
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CLV 044



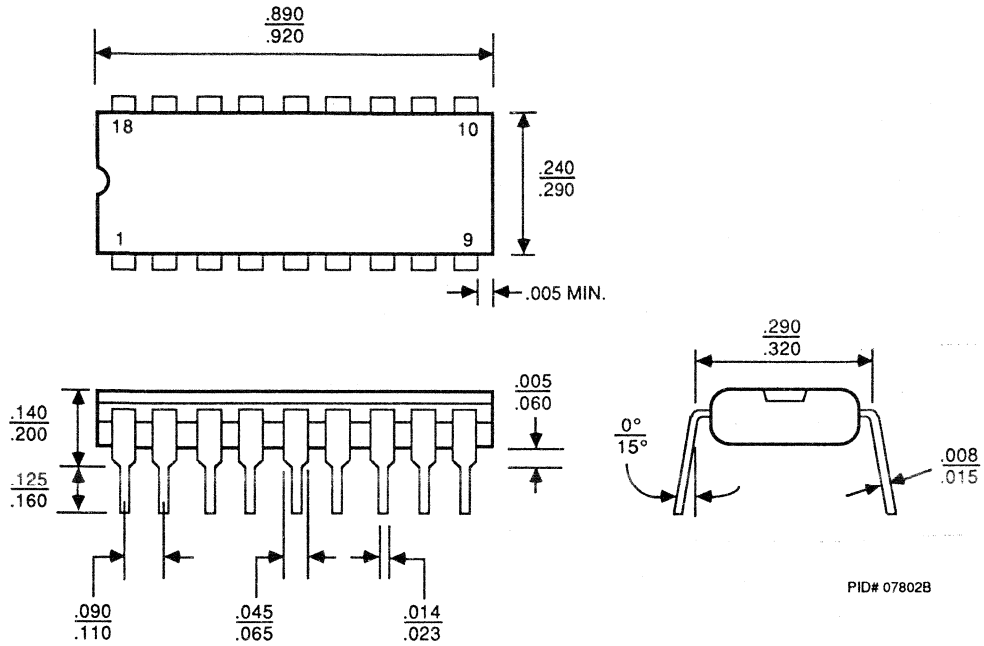
PID #09703C

PD 016

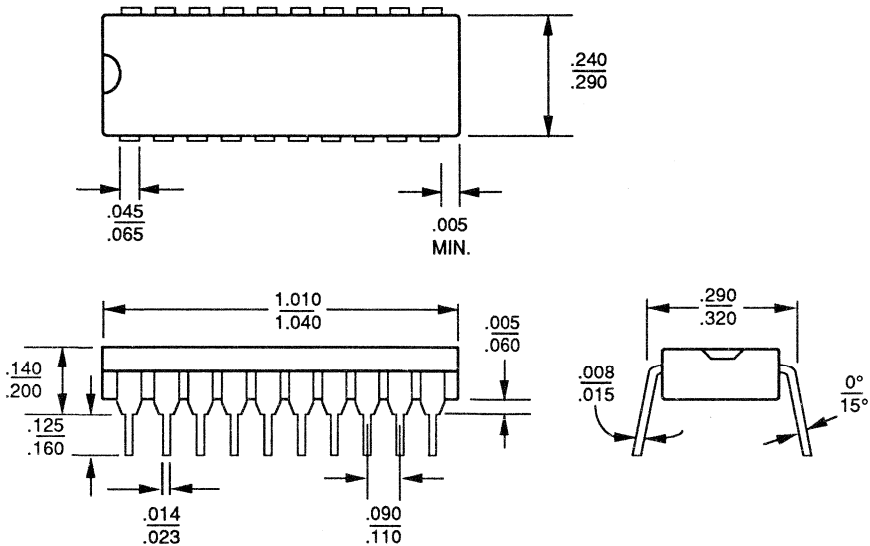


PID# 06967B7

PD 018

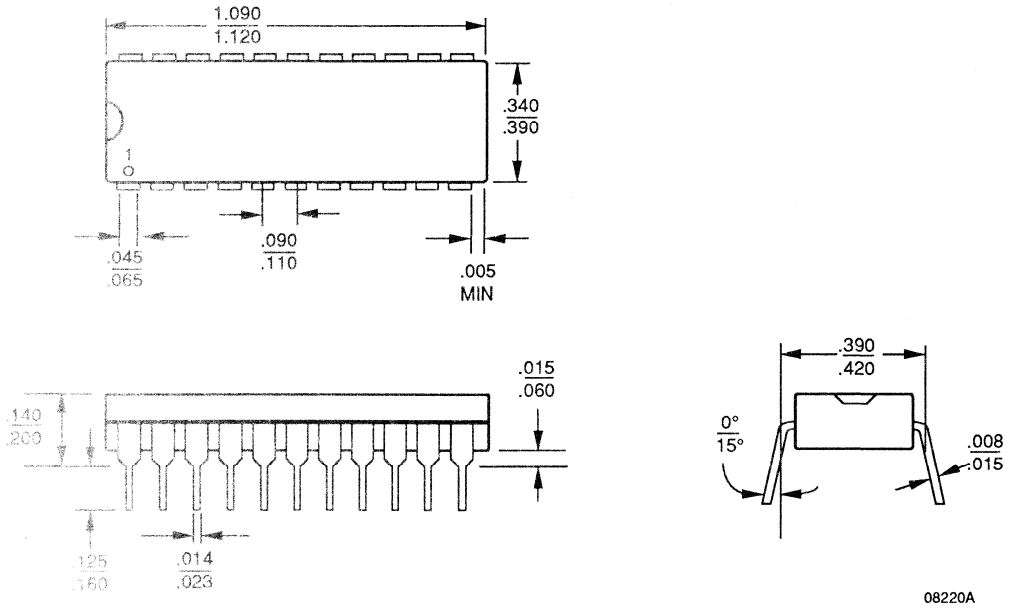


PD 020

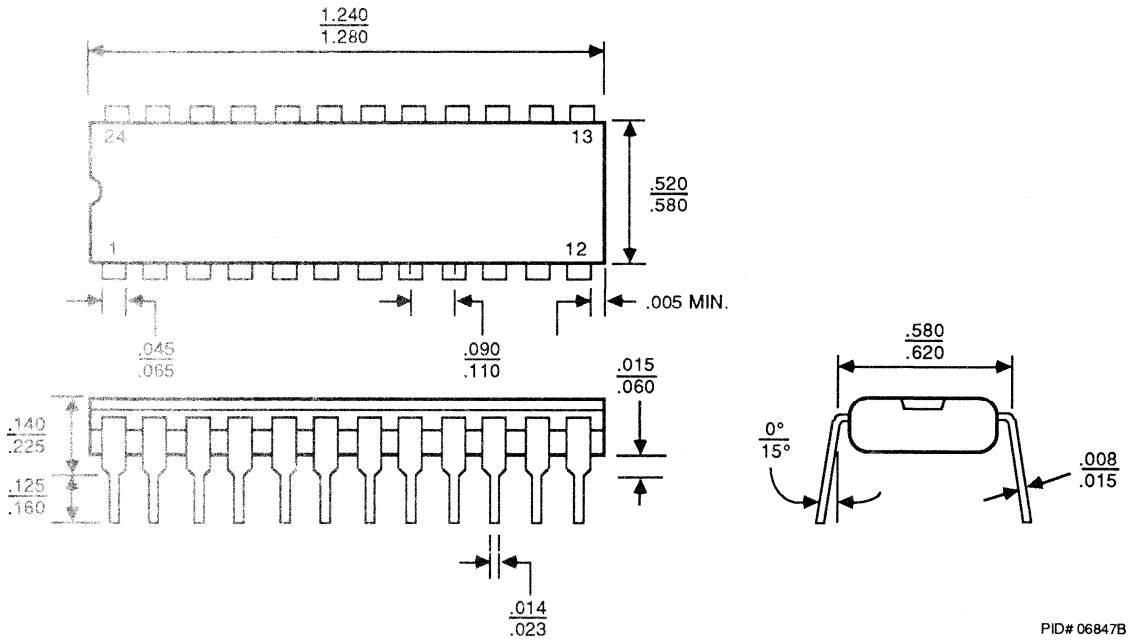


07552A

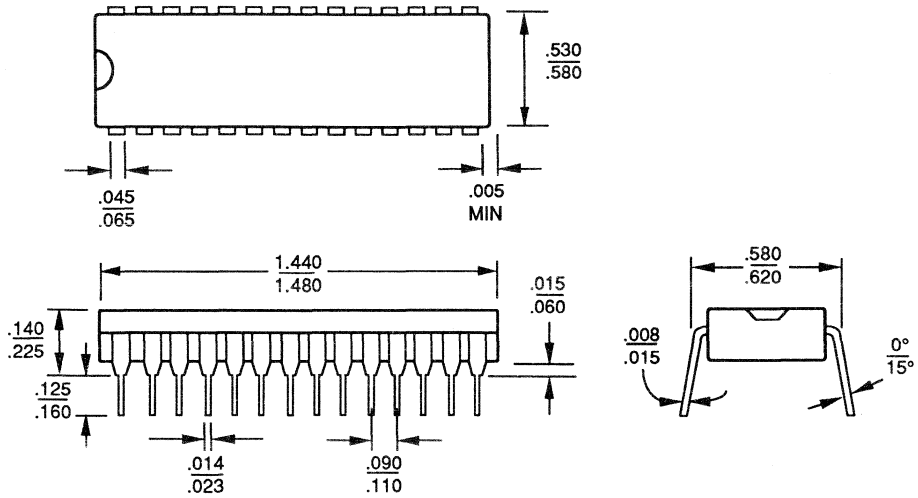
PD 022



PD 024

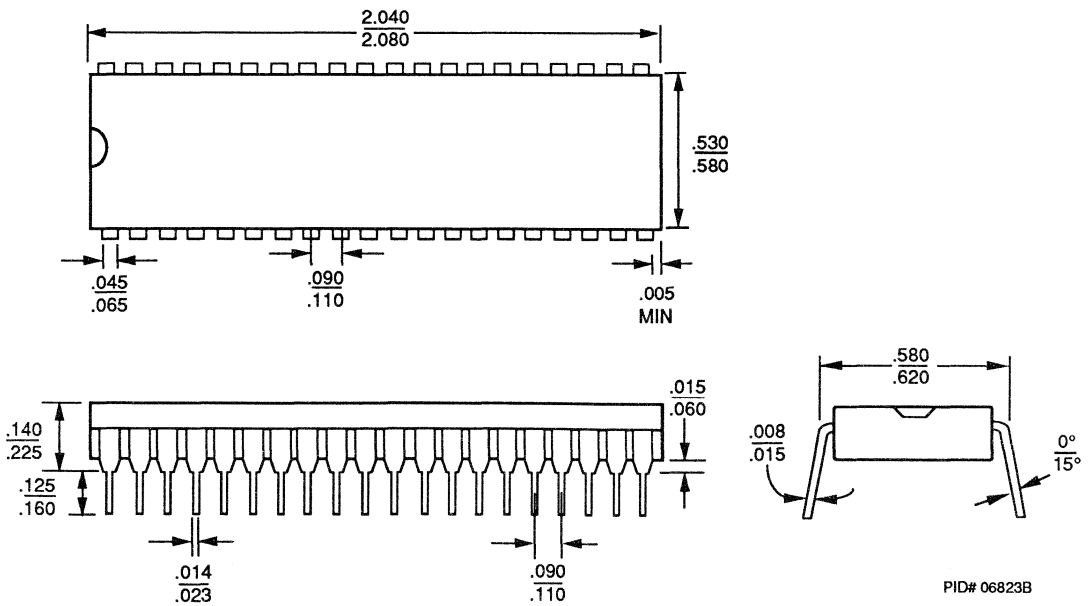


PD 028



06842B

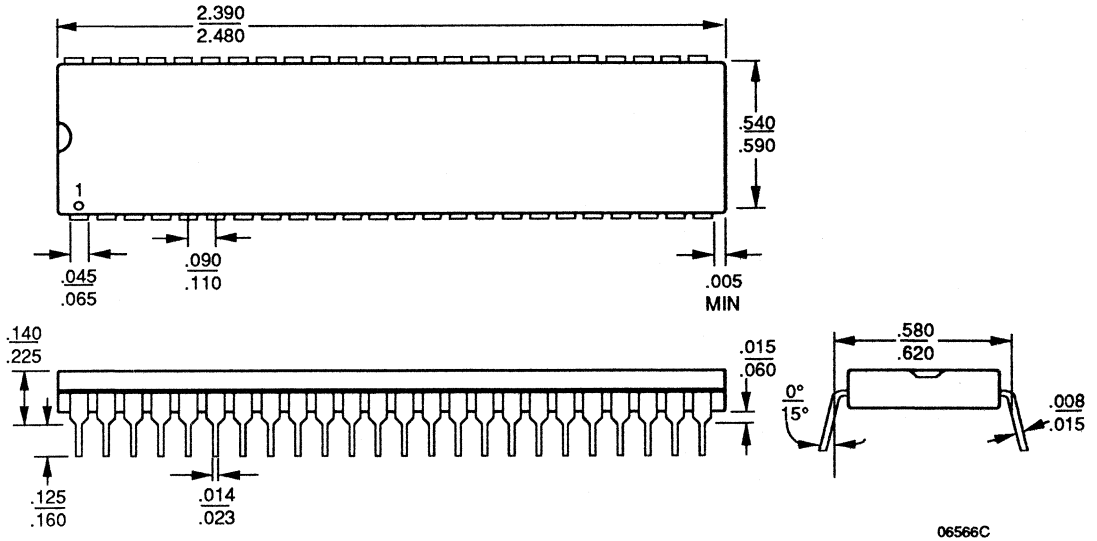
PD 040



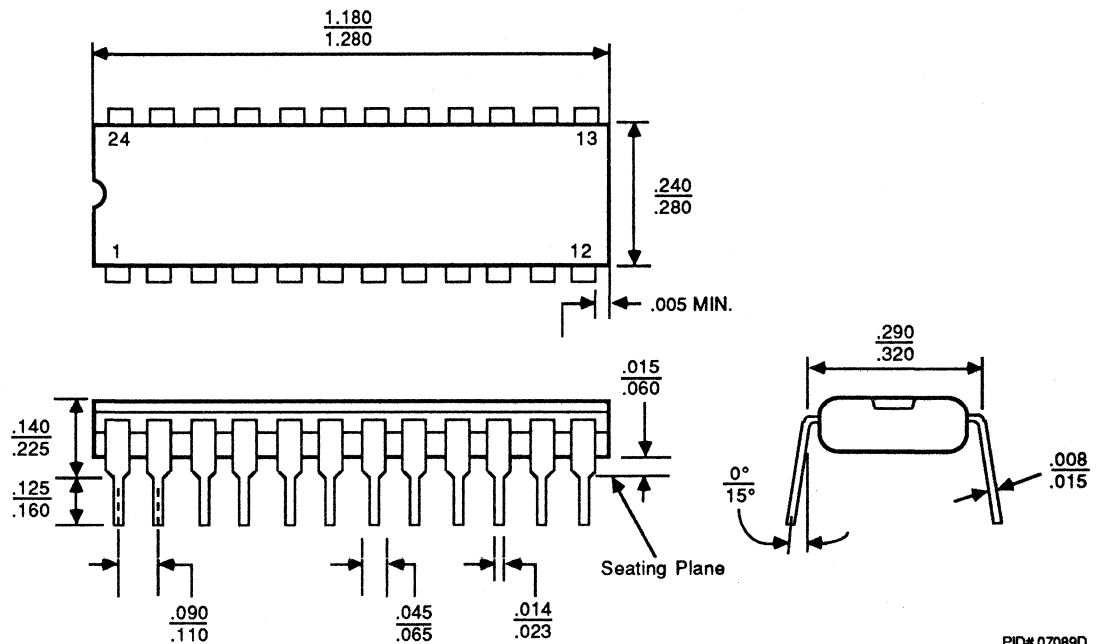
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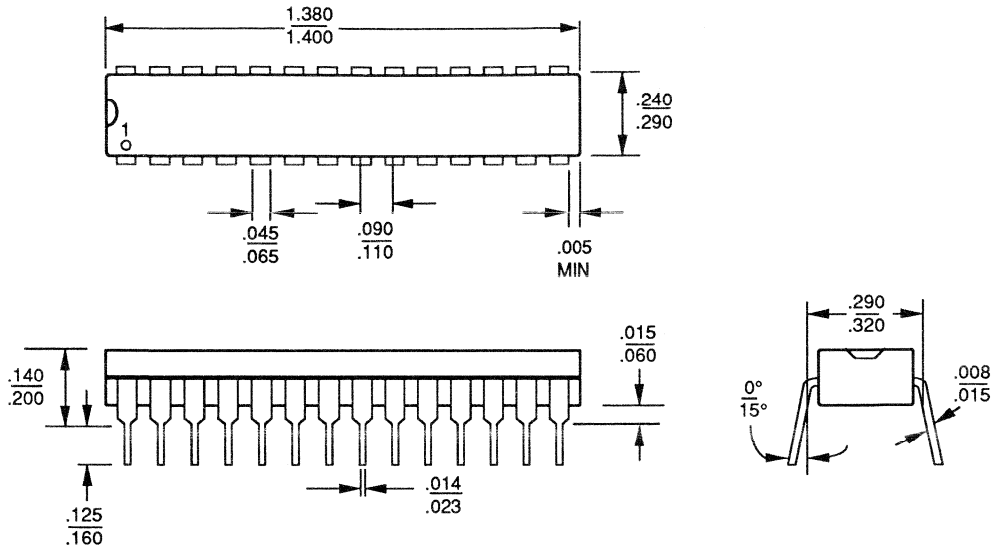
PD 048



PD 3024

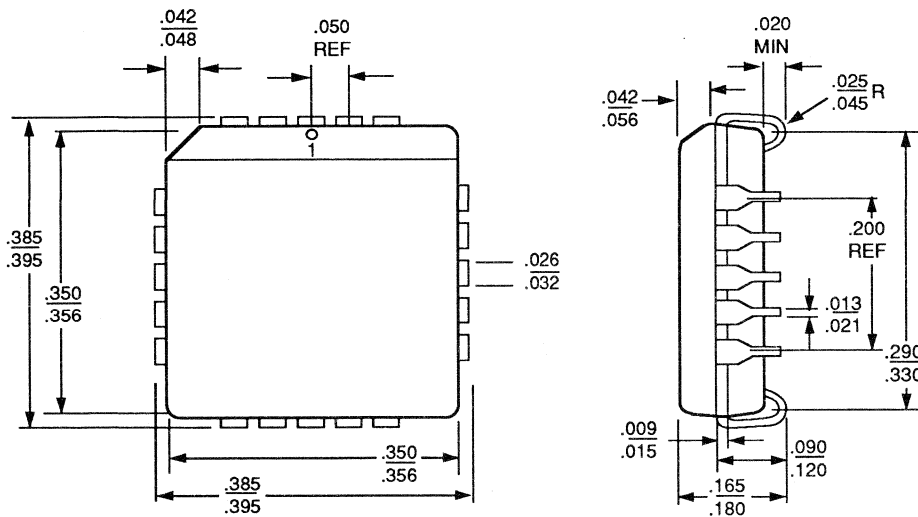


PD 3028



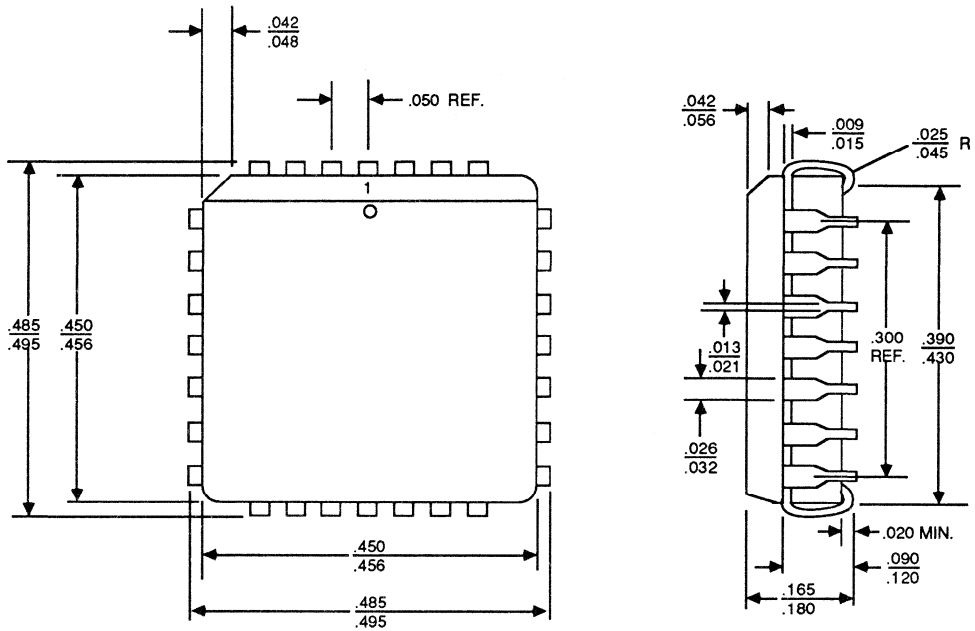
11427A

PL 020



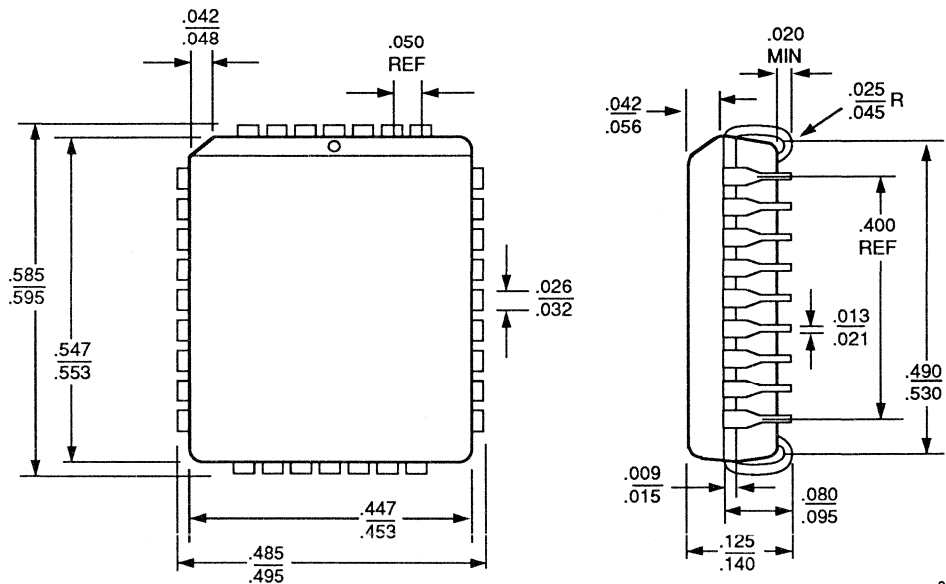
06970D

PL 028



PID # 06751E

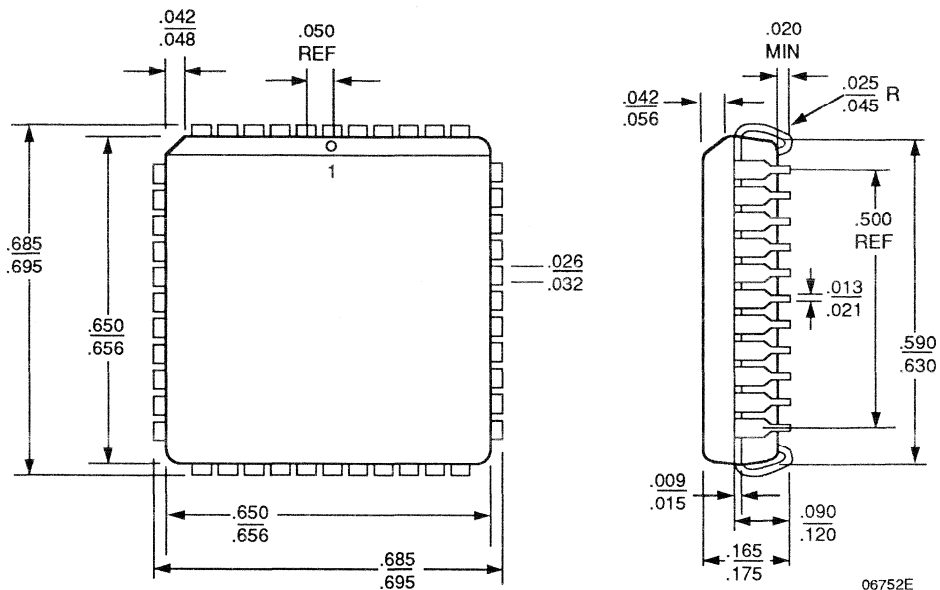
PL 032



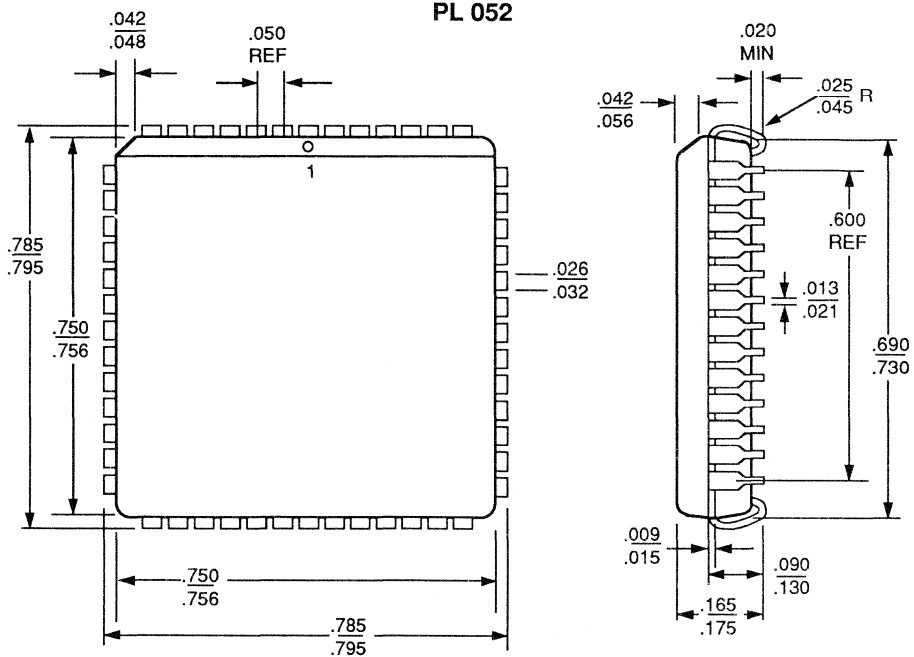
06971C



PL 044

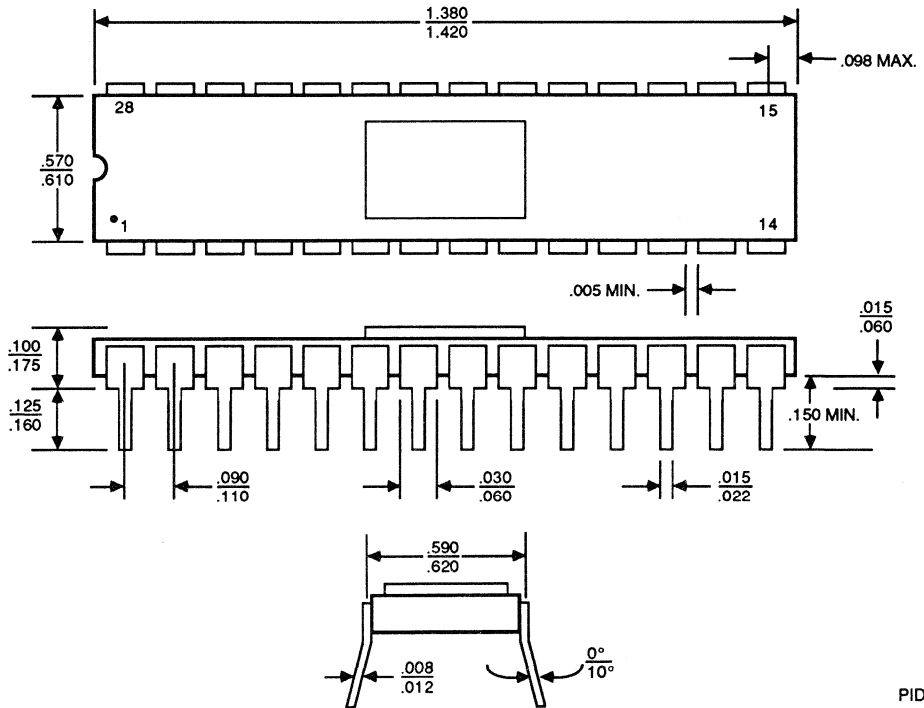


PL 052



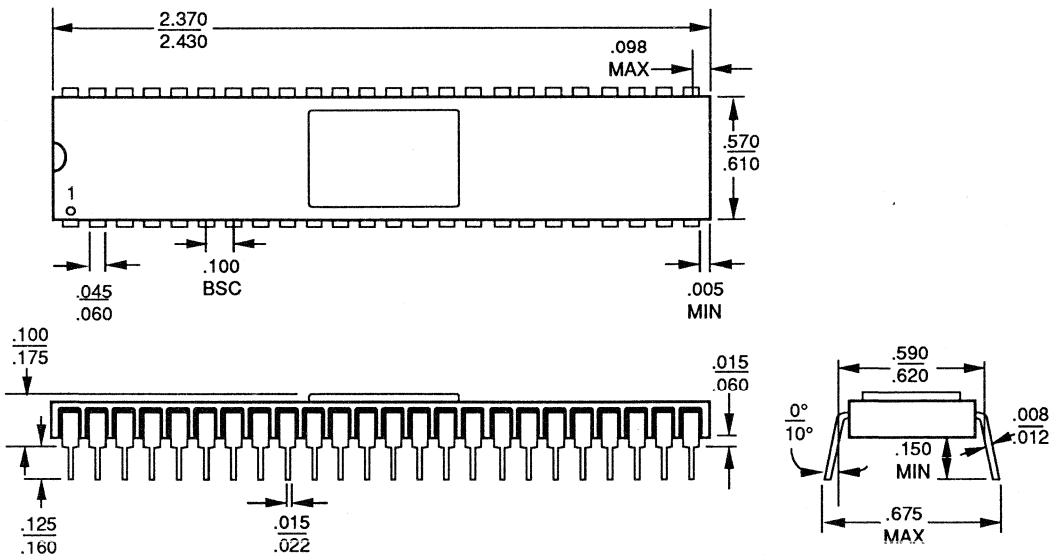
6

### SD 028



PID #07430A

### SD 048



07644B

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 4/10/89  
 B-104M-5/89-0 Printed in USA



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